FOUR CHANNEL DIGITAL AUDIO LIP-SYNC DELAY WITH I²C CONTROL

FEATURES

- **Digital Audio Format: 16-24-bit I²S, Right-Justified, Left-Justified**
- **I²C Bus Controlled**
- **Dual Serial Input Ports**
- **Delay Time: 85 ms/ch at fs = 48 kHz**
- **Delay Resolution: One Sample**
- **Delay Memory Cleared on Power-Up or After Delay Changes**
  - **Eliminates Erroneous Data on Output**
- **3.3 V Operation With 5 V Tolerant I/O and I²C Control**
- **Supports Audio Bit Clock Rates of 32 to 64 fs with fs = 32 kHz–192 kHz**
- **No External Crystal or Oscillator Required**
  - **All Internal Clocks Generated From the Audio Clock**
- **Independent Clocks for Each Audio Input**
- **Surface Mount 4mm × 4mm, 16-pin QFN Package**

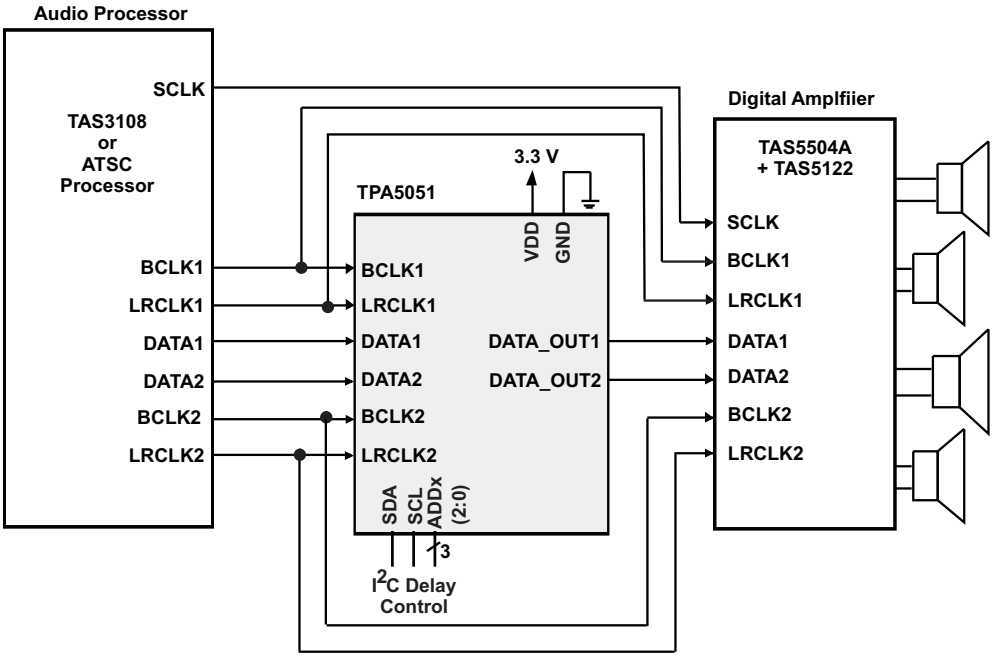
APPLICATIONS

- **High Definition Lip-Sync Delay**
- **Flat Panel TV Lip-Sync Delay**
- **Home Theater Rear Channel Effects**
- **Wireless Speaker Front-Channel Synchronization**

DESCRIPTION

The TPA5051 accepts two serial audio inputs, buffers the data for a selectable period of time, and outputs the delayed audio data on two serial outputs. One device allows delay of up to 85 ms/ch (fs = 48 kHz) to synchronize the audio stream to the video stream in systems with complex video processing algorithms. If more delay is needed, the devices can be connected in series. Independent clocks can be used for each audio input.

SIMPLIFIED APPLICATION DIAGRAM



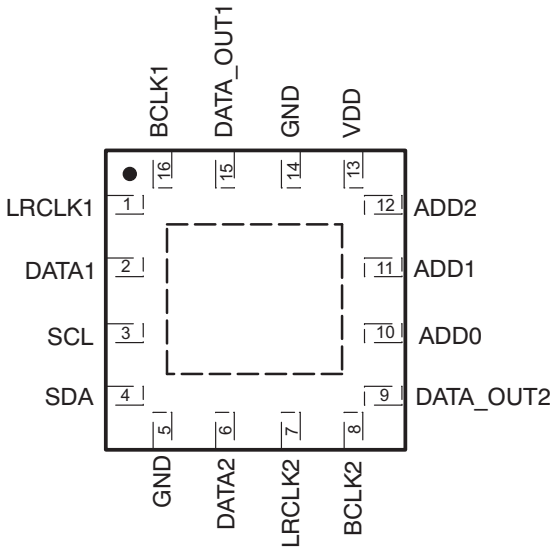
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PIN DESCRIPTIONS

RSA (QFN) PACKAGE
(TOP VIEW)

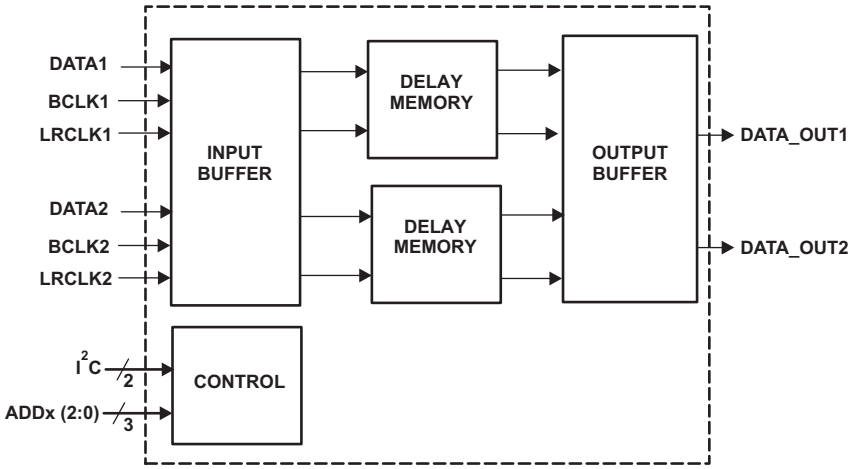


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ADD0	10	I	I^2C address select pin – LSB. 5V tolerant input.
ADD1	11	I	I^2C address select pin. 5V tolerant input.
ADD2	12	I	I^2C address select pin – MSB. 5V tolerant input.
BCLK1 (1)	16	I	Audio data bit clock input for serial input 1. 5V tolerant input.
BCLK2 (1)	8	I	Audio data bit clock input for serial input 2. 5V tolerant input.
DATA1	2	I	Audio serial data input for serial input 1. 5V tolerant input.
DATA2	6	I	Audio serial data input for serial input 2. 5V tolerant input.
DATA_OUT1	15	O	Delayed audio serial data output for channel 1.
DATA_OUT2	9	O	Delayed audio serial data output for channel 2.
GND	5, 14	P	Ground – All ground terminals must be tied to GND for proper operation
LRCLK1 (1)	1	I	Channel 1 left and right serial audio sampling rate clock (fs). 5V tolerant input.
LRCLK2 (1)	7	I	Channel 2 left and right serial audio sampling rate clock (fs). 5V tolerant input.
SCL	3	I	I^2C communication bus clock input. 5V tolerant input.
SDA	4	I/O	I^2C communication bus data input. 5V tolerant input.
VDD	13	P	Power supply interface.
Thermal Pad		-	Connect to ground. Must be soldered down in all applications to properly secure device on the PCB.

(1) Left and right channels may use different BCLK frequencies as well as different LRCLK (fs) frequencies.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted) (1)

			VALUE	UNIT
V_{DD}	Supply voltage		–0.3 to 3.6	V
V_I	Input voltage	DATA, LRCLK, BCLK, SCL, SDA, ADD[2:0]	–0.3 to 5.5	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_A	Operating free-air temperature range		–40 to 85	°C
T_J	Operating junction temperature range		–40 to 125	°C
T_{stg}	Storage temperature range		–65 to 125	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RSA	2.5 W	25 mW/°C	1.375 W	1.0 W

(1) This data was taken using 1 oz trace copper and copper pad that is soldered directly to a JEDEC standard high-k PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI technical briefs SCBA01D and SLUA271 for more information about using the QFN thermal pad.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage	VDD	3	3.6	V
V_{IH}	High-level input voltage	DATA1, DATA2, LRCLK1, LRCLK2, BCLK1, BCLK2, SCL, SDA, ADD[2:0]	2		V
V_{IL}	Low-level input voltage	DATA1, DATA2, LRCLK1, LRCLK2, BCLK1, BCLK2, SCL, SDA, ADD[2:0]		0.8	V
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 3.3 V, fs = 48 kHz, BCLK = 32 × fs		1.8	3	mA
I_{OH}	High-level output current	DATA_OUT1 = DATA_OUT2 = 2.6 V	5		13	mA
I_{OL}	Low-level output current	DATA_OUT1 = DATA_OUT2 = 0.4 V	5		13	mA
I_{IH}	High-level input current	DATA1, DATA2, LRCLK1, LRCLK2, BCLK1, BCLK2, SCL, SDA, Vi = 5.5V, VDD = 3V			20	µA
		ADD[2:0], Vi = 3.6V, VDD = 3.6V			5	µA
I_{IL}	Low-level input current	DATA1, DATA2, LRCLK1, LRCLK2, BCLK1, BCLK2, SCL, SDA, ADD[2:0], Vi = 0V, VDD = 3.6V			1	µA

TIMING CHARACTERISTICS(1)(2)

For I²C Interface Signals Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Frequency, SCL	No wait states			400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6			µs
$t_{w(L)}$	Pulse duration, SCL low		1.3			µs
t_{su1}	Setup time, SDA to SCL		100			ns
t_{h1}	Hold time, SCL to SDA		10			ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3			µs
t_{su2}	Setup time, SCL to start condition		0.6			µs
t_{h2}	Hold time, start condition to SCL		0.6			µs
t_{su3}	Setup time, SCL to stop condition		0.6			µs

(1) $V_{Pull\text{-}up} = V_{DD}$
(2) A pull-up resistor ≤2 kΩ is required for a 5 V I²C bus voltage.

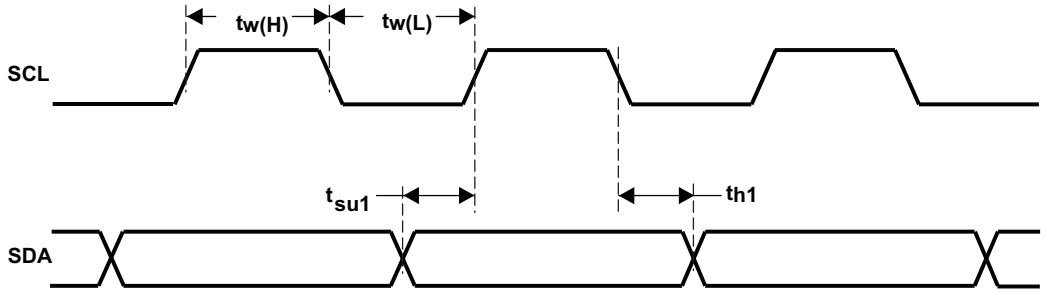


Figure 1. SCL and SDA Timing

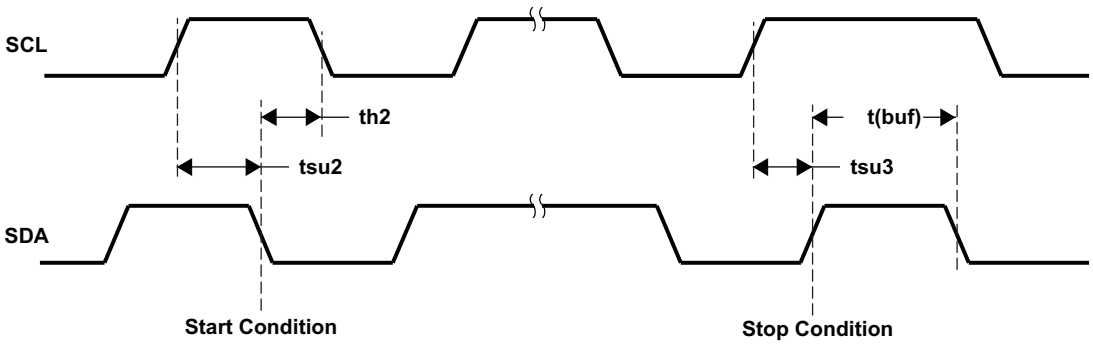


Figure 2. Start and Stop Conditions Timing

Serial Audio Input Ports

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLKIN}	Frequency, BCLK 32 × fs, 48 × fs, 64 × fs		1.024		12.288	MHz
t_{su1}	Setup time, LRCLK to BCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from BCLK rising edge		10			ns
t_{su2}	Setup time, DATA to BCLK rising edge		10			ns
t_{h2}	Hold time, DATA from BCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	BCLK duty cycle			50%		
	LRCLK duty cycle			50%		
	BCLK rising edges between LRCLK rising edges	LRCLK duty cycle = 50%	32		64	BCLK edges

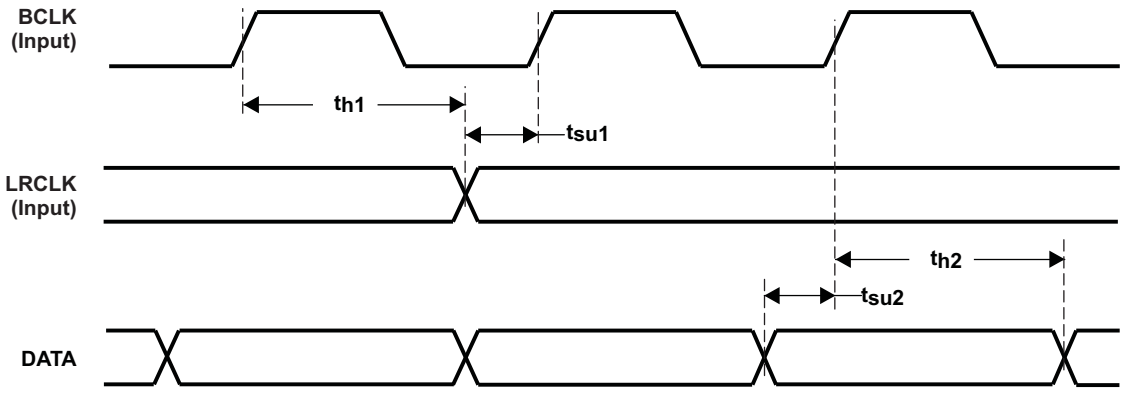


Figure 3. Serial Data Interface Timing

APPLICATION INFORMATION

AUDIO SERIAL INTERFACE

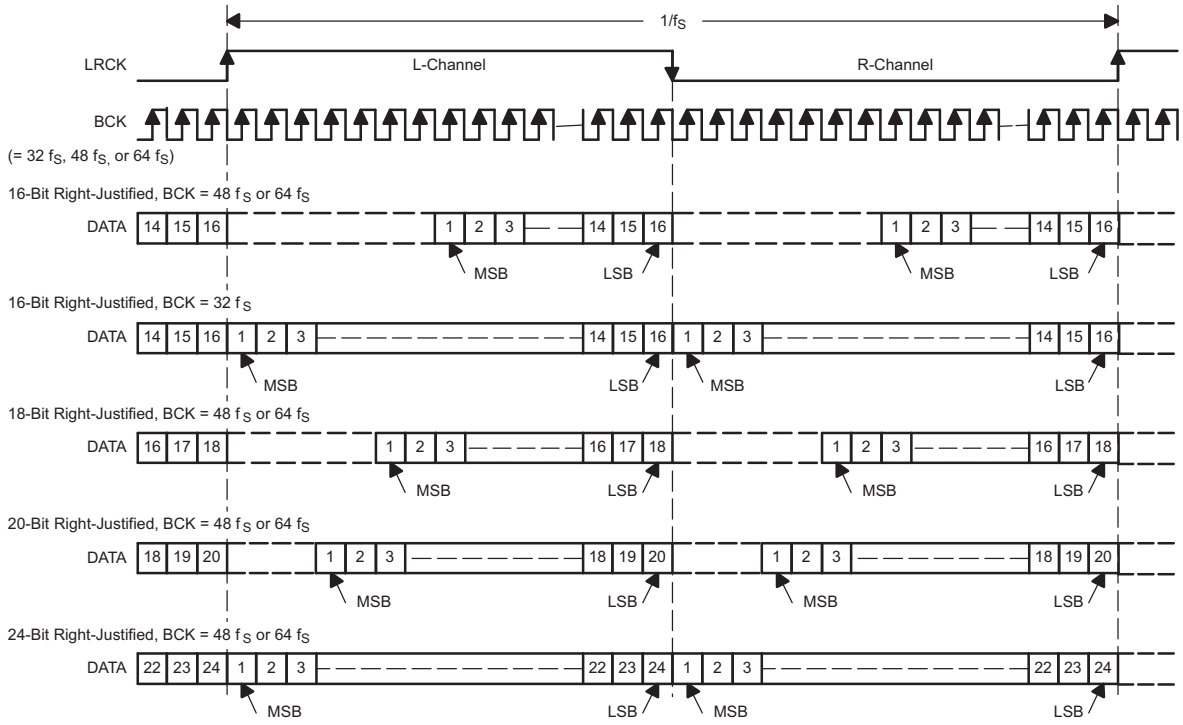
The audio serial interface for the TPA5051 consists of two 3-wire synchronous serial ports. Each includes an LRCLK, BCLK, and DATA. BCLK is the serial audio bit clock, and it is used to clock the serial data present on the DATA line into the serial shift register of the audio interface. Serial data is clocked into the TPA5051 on the rising edge of BCLK. LRCLK is the serial audio left/right word clock, operated at the sampling frequency, fs. It is used to latch serial data into the internal registers of the serial audio interface. BCLK can be operated at 32 to 64 times the sampling frequency for right-justified, left-justified, and I^2S formats. Generally, both LRCLK and BCLK should be synchronous to the system clock. However, the TPA5051 does not have a system clock, so the only synchonization necessary is between BCLK and LRCLK.

AUDIO DATA FORMATS AND TIMING

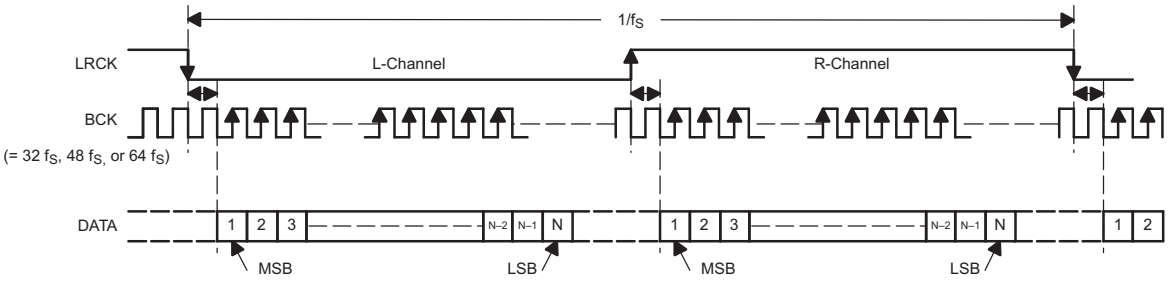
The TPA5051 supports industry-standard audio data formats, including right-justified, I^2S, and left-justified. The data formats are shown in Figure 4. Data formats are selected using the I^2C interface and register map (see Table 1).

APPLICATION INFORMATION (continued)

(1) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

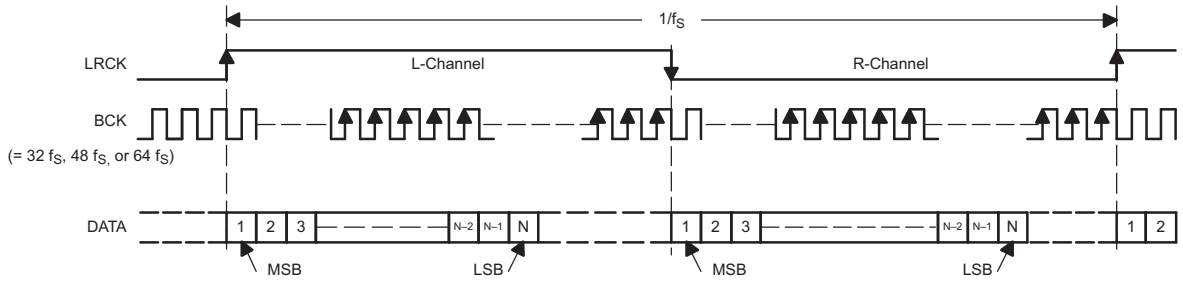


Figure 4. Audio Data Formats

APPLICATION INFORMATION (continued)

GENERAL I²C OPERATION

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 5. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TPA5051 holds SDA low during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection.

An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. When the bus level is 5 V, pull-up resistors between 1 kΩ and 2 kΩ in value must be used. For a bus level of 3.3 V, higher resistor values, such as 10 kΩ, may be used.

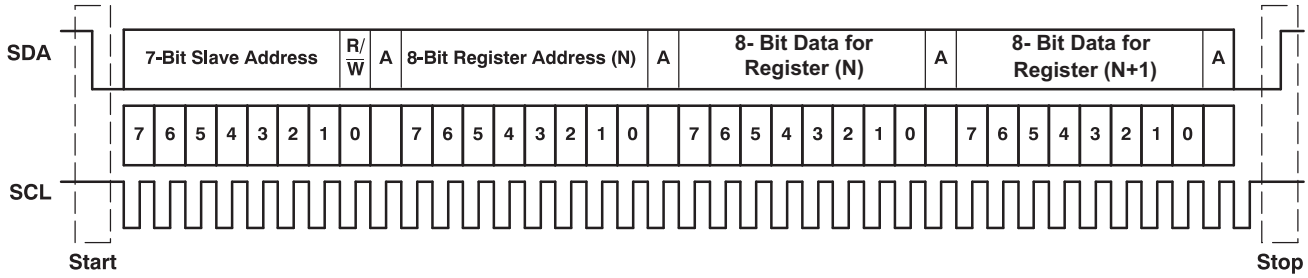


Figure 5. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 5.

The 7-bit address for the TPA5051 is selectable using the 3 address pins (ADD0, ADD1, ADD2). Table 1 lists the 8 possible slave addresses.

Table 1. I²C Slave Address

FIXED ADDRESS (4 MSB bits)	SELECTABLE ADDRESS BITS		
	ADD2	ADD1	ADD0
1101	0	0	0
1101	0	0	1
1101	0	1	0
1101	0	1	1
1101	1	0	0
1101	1	0	1
1101	1	1	0
1101	1	1	1

SINGLE-AND MULTIPLE-BYTE TRANSFERS

The serial control interface supports both single-byte and multi-byte read/write operations for all registers.

During multiple-byte read operations, the TPA5051 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TPA5051 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

SINGLE-BYTE WRITE

As shown is Figure 6, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TPA5051 responds with an acknowledge bit. Next, the master transmits the register byte corresponding to the TPA5051 internal memory address being accessed. After receiving the register byte, the TPA5051 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TPA5051 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.

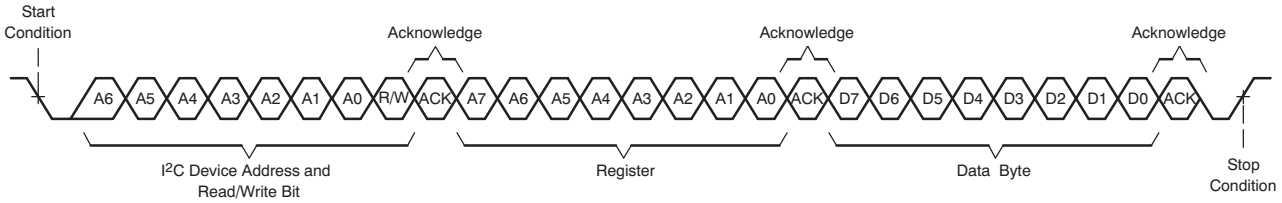


Figure 6. Single-Byte Write Transfer

MULTIPLE-BYTE WRITE AND INCREMENTAL MULTIPLE-BYTE WRITE

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TPA5051 as shown in Figure 7. After receiving each data byte, the TPA5051 responds with an acknowledge bit.

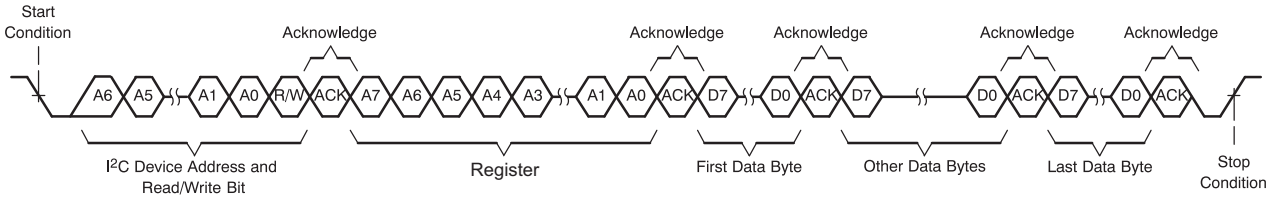


Figure 7. Multiple-Byte Write Transfer

SINGLE-BYTE READ

As shown in Figure 8, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TPA5051 address and the read/write bit, the TPA5051 responds with an acknowledge bit. The master then sends the internal memory address byte, after which the TPA5051 issues an acknowledge bit. The master device transmits another start condition followed by the TPA5051 address and the read/write bit again. This time the read/write bit is set to 1, indicating a read transfer. Next, the TPA5051 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

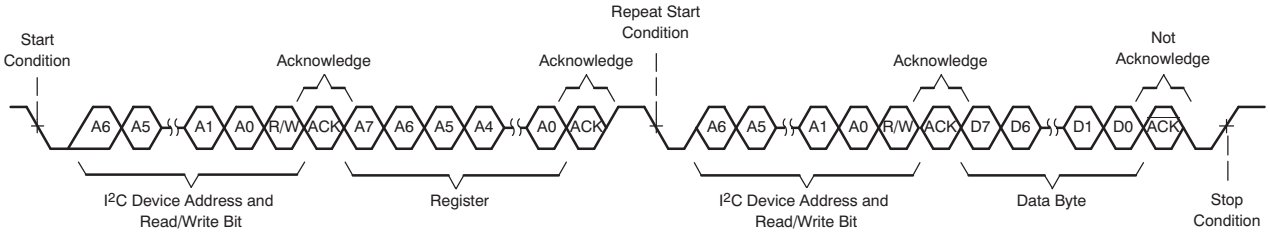


Figure 8. Single-Byte Read Transfer

MULTIPLE-BYTE READ

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TPA5051 to the master device as shown in Figure 9. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

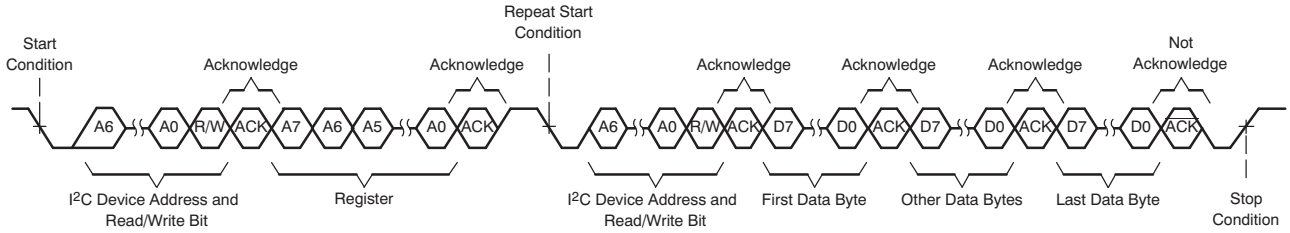


Figure 9. Multiple-Byte Read Transfer

TPA5051 Operation

The following sections describe the registers configurable via I²C commands for the TPA5051.

Only a single decoupling capacitor (0.1 µF–1 µF) is required across VDD and GND. The ADDx terminals can be directly connected to VDD or GND. Table 1 describes the I²C addresses selectable via the ADDx terminals. A schematic implementation of the TPA5051 is shown in Figure 10.

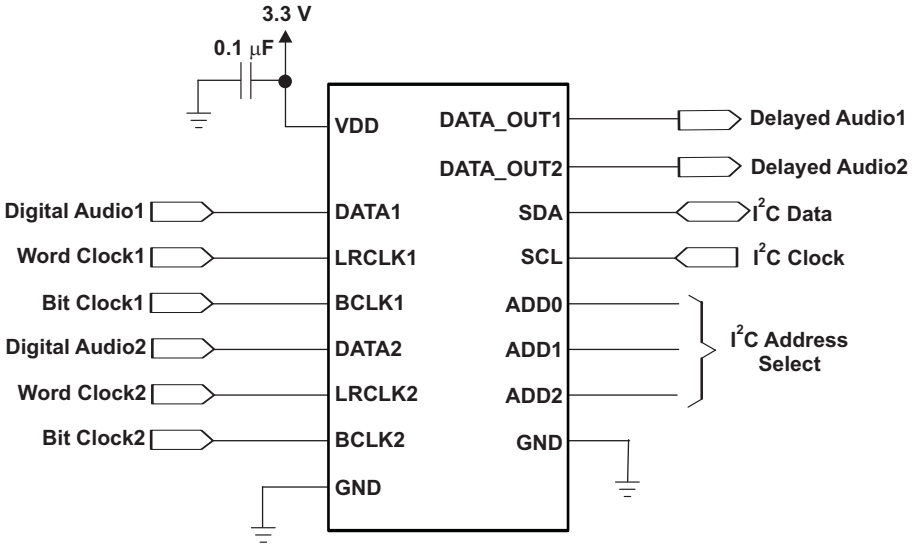


Figure 10. TPA5051 Schematic

SERIAL CONTROL INTERFACE REGISTER SUMMARY

Table 2. Serial Control Register Summary

REGISTER	REGISTER NAME	NO. OF BYTES	CONTENTS	INITIALIZATION VALUE
0x01(1)	Control Register	1	Description shown in subsequent section	00
0x02(1)	Right Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x03(1)	Right Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x04(1)	Left Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x05(1)	Left Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x06(1)	Frame Delay	1	Description shown in subsequent section	00
0x07(1)	RJ Packet Length	1	Description shown in subsequent section	00
0x08(1)	Complete Update	1	Description shown in subsequent section	00
0x09(2)	Control Register	1	Description shown in subsequent section	00
0x0A(2)	Right Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x0B(2)	Right Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x0C(2)	Left Delay Upper (5 bits)	1	Description shown in subsequent section	00
0x0D(2)	Left Delay Lower (8 bits)	1	Description shown in subsequent section	00
0x0E(2)	Frame Delay	1	Description shown in subsequent section	00
0x0F(2)	RJ Packet Length	1	Description shown in subsequent section	00
0x10(2)	Complete Update	1	Description shown in subsequent section	00

(1) I^2C registers for serial data channel 1
(2) I^2C registers for serial data channel 2

CONTROL REGISTER (0x01, 0x09)

The control register allows the user to mute a specific audio channel. It is also used to specify the data type (I^2S, Right-Justified, or Left-Justified).

Table 3. Control Registers (0x01, 0x09)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	X	X	X	X	–	–	**Left and Right channel are active.**
0	1	X	X	X	X	–	–	Left channel is MUTED.
1	0	X	X	X	X	–	–	Right channel is MUTED.
1	1	X	X	X	X	–	–	Left and Right channel are MUTED.
–	–	X	X	X	X	**0**	**0**	**I^2S data format**
–	–	X	X	X	X	0	1	Right-justified data format (see PACKET LENGTH register 0x07)
–	–	X	X	X	X	1	0	Left-justified data format
–	–	X	X	X	X	1	1	Bypass mode – data is passed straight through without delay.

(1) Default values are in **bold**.

AUDIO DELAY REGISTERS (0x02–0x05, 0x0A–0x0D)

The audio delay for the left and right channels is fixed by writing a total of 13 bits (2 byte transfer) to upper and lower registers as specified in Table 1. A multiple byte transfer should be performed starting with the control register and following with 4 bytes to fill the upper and lower registers associated with right/left channel delay. The decimal value of D0–D13 equals the number of samples to delay. The maximum number of delayed samples per channel is 4095 for the TPA5051. This equates to 85.3 ms ([4095 × (1/Fs)] at 48 kHz) of delay per channel.

Table 4. Audio Delay Registers (0x02–0x05, 0x0A–0x0D)(1)

D13	D12	D11–D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**Left and Right audio is passed to output with no delay.**
0	0	0	0	1	Left and Right audio is delayed by 1 sample (1/Fs = delay time)
1	1	1	1	1	Left and Right audio is delayed by 4095 samples (4095/Fs = delay time)

(1) Default values are in **bold**.

FRAME DELAY REGISTERS (0x06, 0x0E)

This register can be used to specify delay in video frames instead of audio samples. When the MSB is set to 1, the audio delay registers (0x01–0x04) are bypassed and the Frame Delay Register is used to set the delay based on the frame rate (D6), audio sample rate (D5–D3), and number of frames to delay (D2–D0).

The total audio delay time is calculated by the following formula:

Audio Delay (in samples) = int [# Delay Frames × (1/Frame Rate) × Audio Sample Rate]

If the result of the formula above is greater than the maximum number of delay samples (4095 for TPA5051), then the value is limited to this maximum before passing to the delay block.

Table 5. Frame Delay Registers (0x06, 0x0E)(1)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0								**Settings in this register are masked and audio delay is determined by settings in the right/left audio delay registers.**
1								Right/left audio delay registers are masked and delay is determined by settings in this register.
	0							**Frame rate = 50 Hz**
	1							Frame rate = 59.94 Hz
		0	**0**	**0**				**Audio sample rate = 32 kHz**
		0	0	1				Audio sample rate = 44.1 kHz
		0	1	0				Audio sample rate = 48 kHz
		0	1	1				Audio sample rate = 88.2 kHz
		1	0	0				Audio sample rate = 96 kHz
		1	0	1				Audio sample rate = 176.4 kHz
		1	1	0				Audio sample rate = 192 kHz
		1	1	1				Audio sample rate = 192 kHz
					0	**0**	**0**	**Delay frames = 1**
					0	0	1	Delay frames = 2
					1	1	1	Delay frames = 8

(1) Default values are in **bold**.

RJ PACKET LENGTH REGISTERS (0x07, 0x0F)

This register is only used in right justified mode. The decimal value of bits [5:0] represents the width of the useable data in a right justified audio stream. The number of BCLK transitions between LRCLK transitions must be greater than or equal to the packet length selected in this register. The maximum packet length value is 24 bits. Any setting greater whose numerical value is greater than 24 bits is limited to the maximum 24 bits.

Table 6. RJ Package Length (0x07, 0x0F)(1)

D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**Packet length = 0 bits**
0	0	0	0	0	1	Packet length = 1 bits
0	1	1	X	X	X	Packet length = 24 bits

(1) Default values are in **bold**.

COMPLETE UPDATE REGISTER (0x08, 0x10)

Since the audio delay values are divided among several registers, it is likely that multiple writes would be necessary to configure the device. This may cause interruptions in the audio stream and unwanted pops and clicks might occur as register data is passed to delay functional block.

To avoid this from happening, the **Complete Update** register is used to transfer the user settings from the register file to the delay functional block when a 1 is written to the LSB. For example, if the right delay is set to 35 samples, and the left delay is set to 300 samples, the device holds the right channel in MUTE until 35 samples of audio data have passed, and holds the left channel in MUTE until 300 samples of audio data have passed.

The **Complete Update** register must also be used when either the stream type is changed or the RJ packet length is changed. If a complete update command is not issued, the changes will not take effect.

Note that the individual channels can be muted using the upper bits of the Control Registers **without** writing to the Complete Update registers.

Table 7. Complete Update Registers (0x08, 0x10)(1)

D7–D1	D0	FUNCTION
X	**0**	**No data from the register settings is passed to the delay block.**
X	1	Stream type, right/left delay or frame delay, and packet length is passed to the delay functional block.

(1) Default values are in **bold**.

APPLICATION EXAMPLES

Connecting Two Devices in Series to Increase the Delay

It is sometimes desirable to increase the delay time beyond which one device can provide. In such cases, several TPA5051 devices can be placed in series to increase the delay. A maximum of eight devices can be placed in series. This is because each device has eight I^2 address settings. Under no circumstances should two TPA5051 devices share the same I^2S address. See Figure 11.

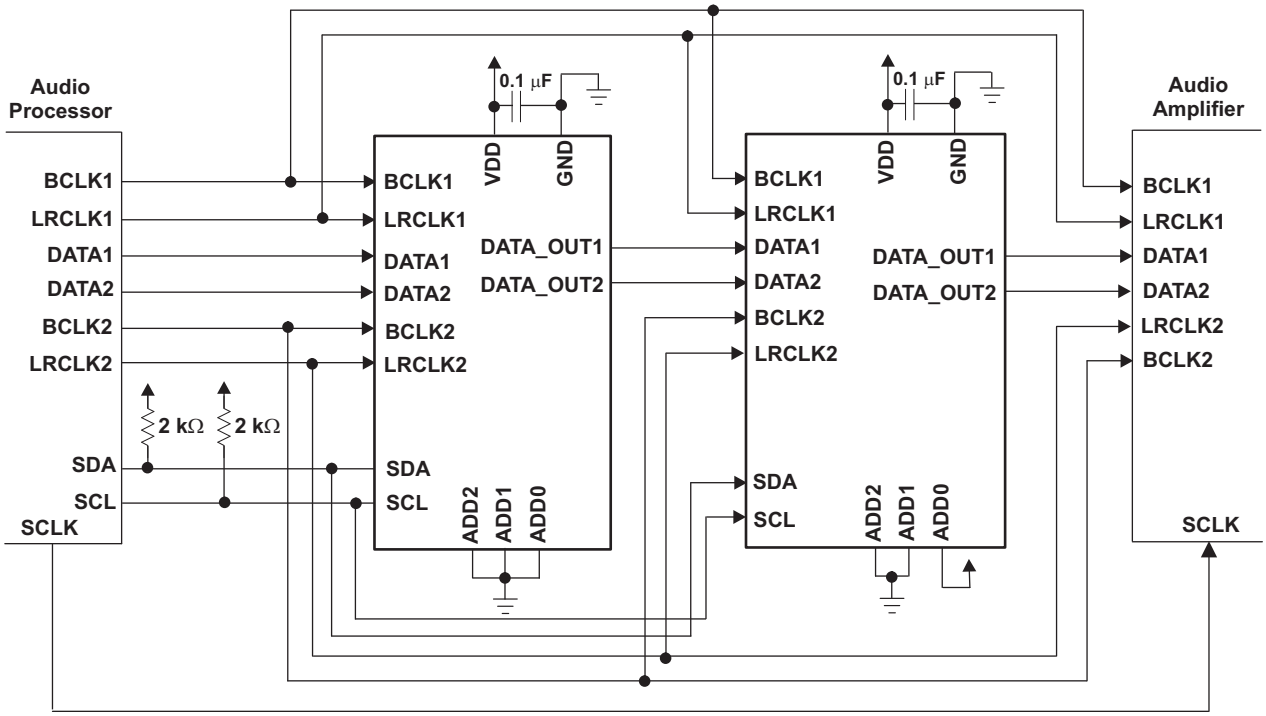


Figure 11. Two Devices Connected in Series

I²C Examples

The following are some examples of I²C commands used to read or write to the TPA5051. For all conditions, assume the address of the TPA5051 is set to 001.

Single Byte Write

In this example, the TPA5051 is set to mute both left and right channels of DATA1, and to operate in I²S mode.

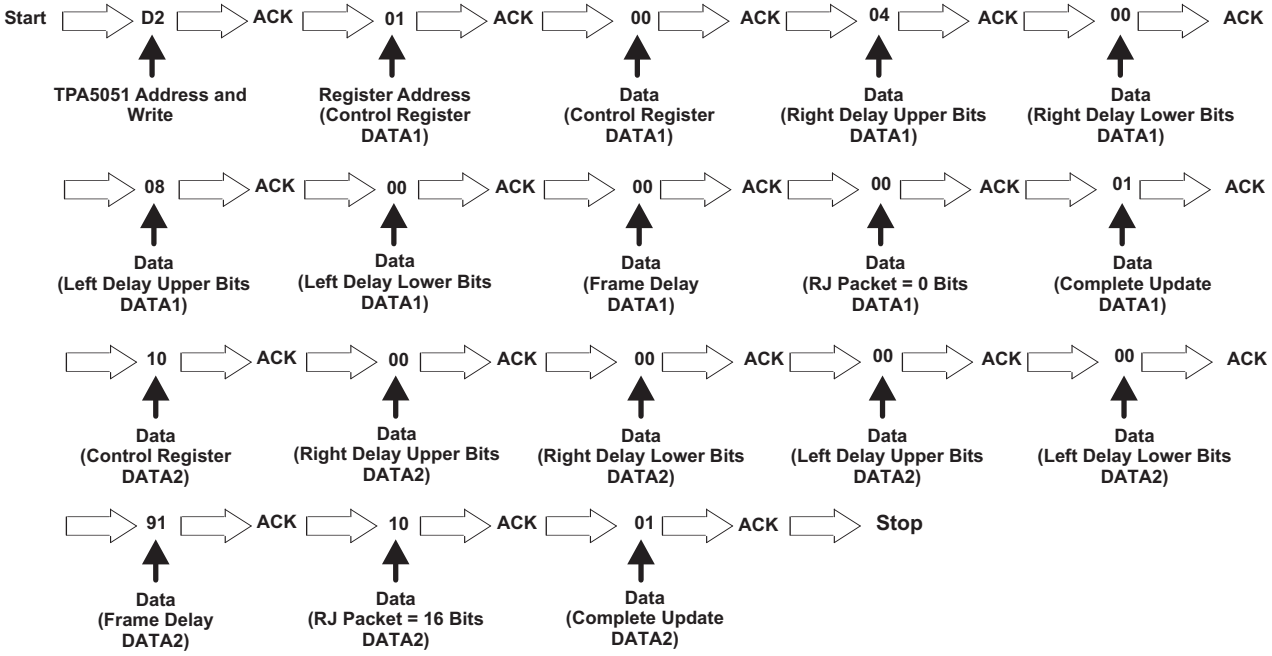


NOTE:

Because no complete update command was issued in this example, the stream type change will not take effect until a *1* is written to the *Complete Update* register.

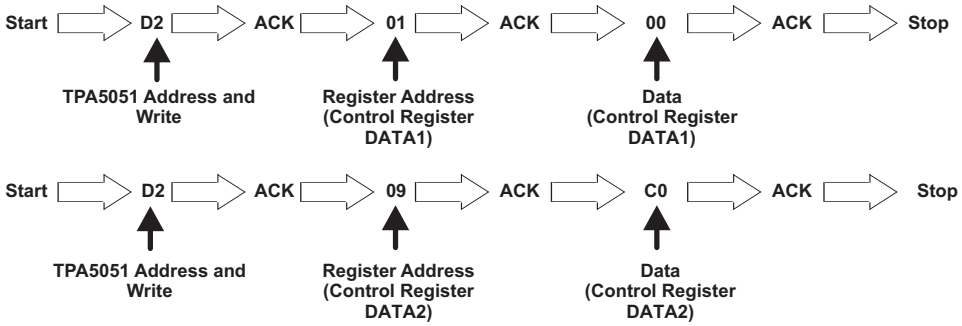
Multiple Byte Write

In this example, the TPA5051 is set to make both the left and right channels of both DATA1 and DATA2 active. DATA1 is set to operate in I²S mode, delay the right channel by 1024 samples, and delay the left channel by 2048 samples. DATA2 is set to operate in the Right-Justified mode with a packet length of 16 bits. It is to delay the audio signal by 40 ms using the Frame Delay function. Assume the audio sample rate (fs) = 48 kHz, and the Frame rate = 50 Hz. This is a sequential write, so all registers must have data written to them.



Combination of Single Byte Writes

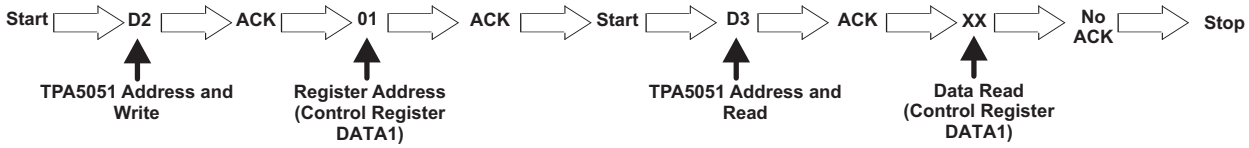
In this example, DATA1 set to operate in the I²S mode, and DATA2 is set to mute.



Note that in every circumstance where a delay or stream type is written into the memory of the TPA5051, a *1* must be written to the *Complete Update* registers for the change to take effect. In this example, the stream type change made to DATA1 would not take effect. This does not apply to muting, which occurs in the *Control* registers.

Single Byte Read

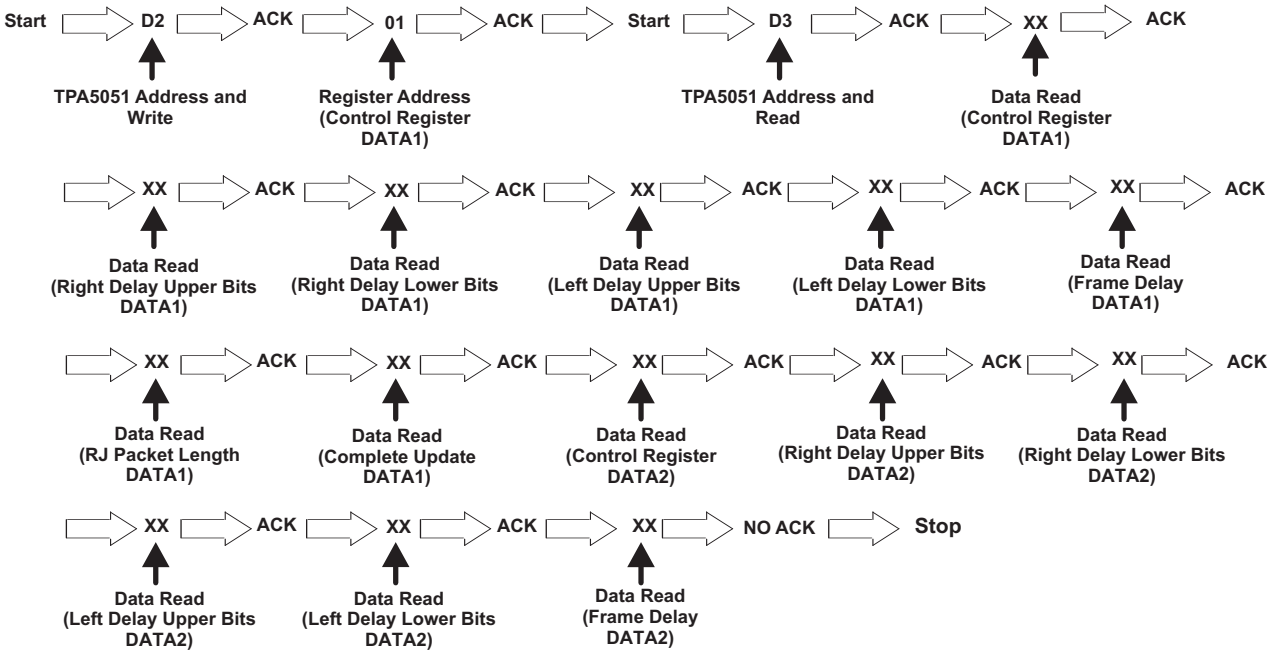
In this example, one byte of data is read from the *Control Register* (0x01). After the data (represented *xx*) by is read by the master device, the master device issues a Not Acknowledge, before stopping the communication.



Multiple Byte Read

Often, when it is necessary to read what is contained in one register, it is necessary to determine what information is contained in all registers. In such a case, a sequential read should be used. In situations where data must be read from a register at the beginning (0x01), and a register towards the end (0x0E), a sequential read is likely to be faster to implement than multiple single byte reads.

In this example, a sequential read is initiated with the *Control Register* (0x01), and ends with the *Frame Delay Register* (0x0E).



DEVICE CURRENT CONSUMPTION

The TPA5051 draws different amounts of supply current depending upon the conditions under which it is operated. As V_{DD} increases, so too does I_{DD}. Likewise, as V_{DD} decreases, I_{DD} decreases. The same is true of the sampling frequency, fs. An increase in fs causes an increase in I_{DD}. Figure 12 illustrates the relationship between operating condition and typical supply current.

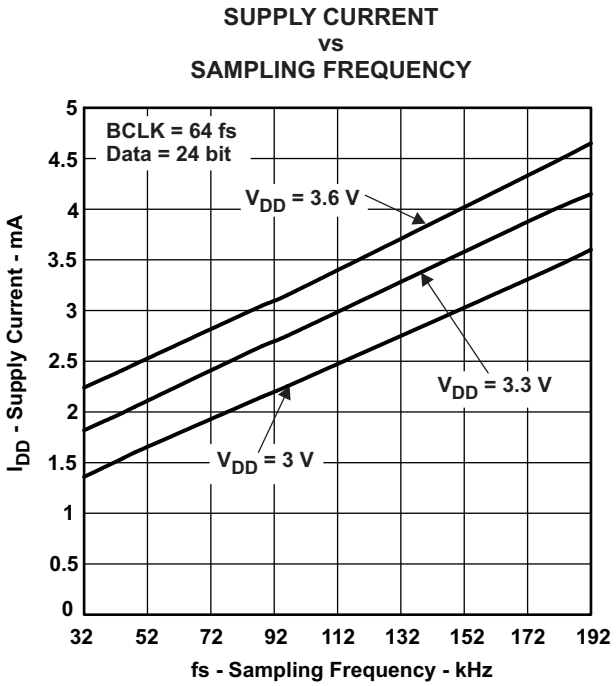


Figure 12. Typical Supply Current

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA5051RSAR	ACTIVE	QFN	RSA	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5051	Samples
TPA5051RSAT	NRND	QFN	RSA	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA 5051	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

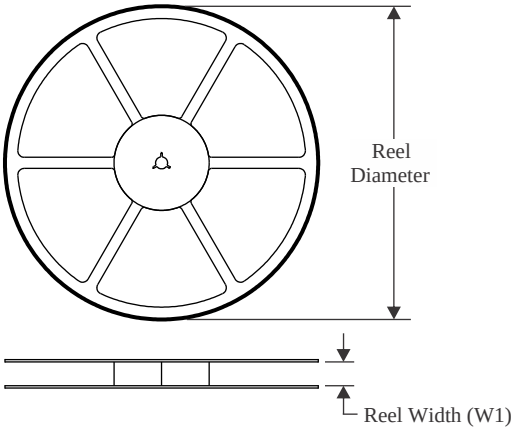
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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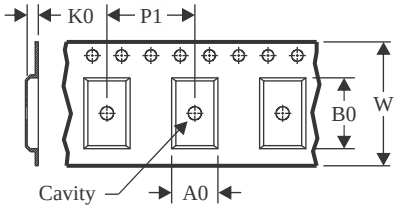
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

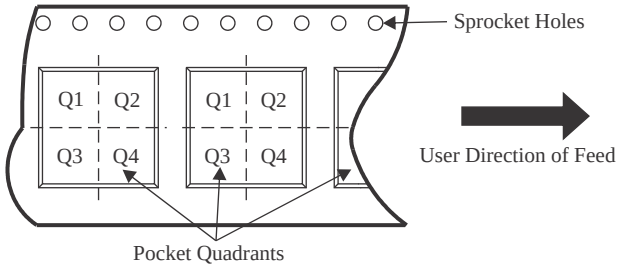


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

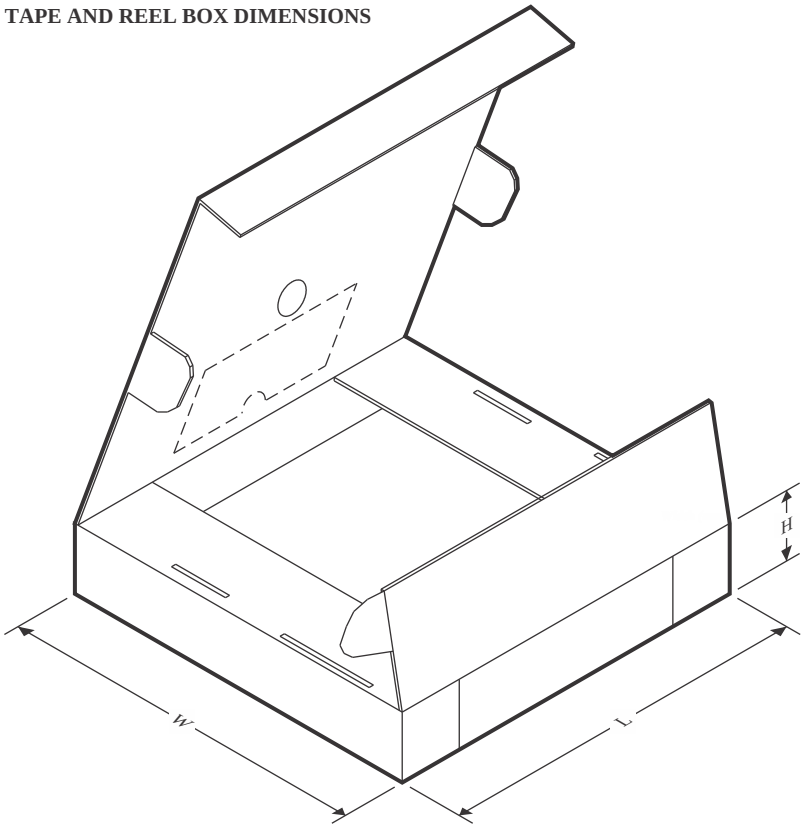
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA5051RSAR	QFN	RSA	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA5051RSAT	QFN	RSA	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

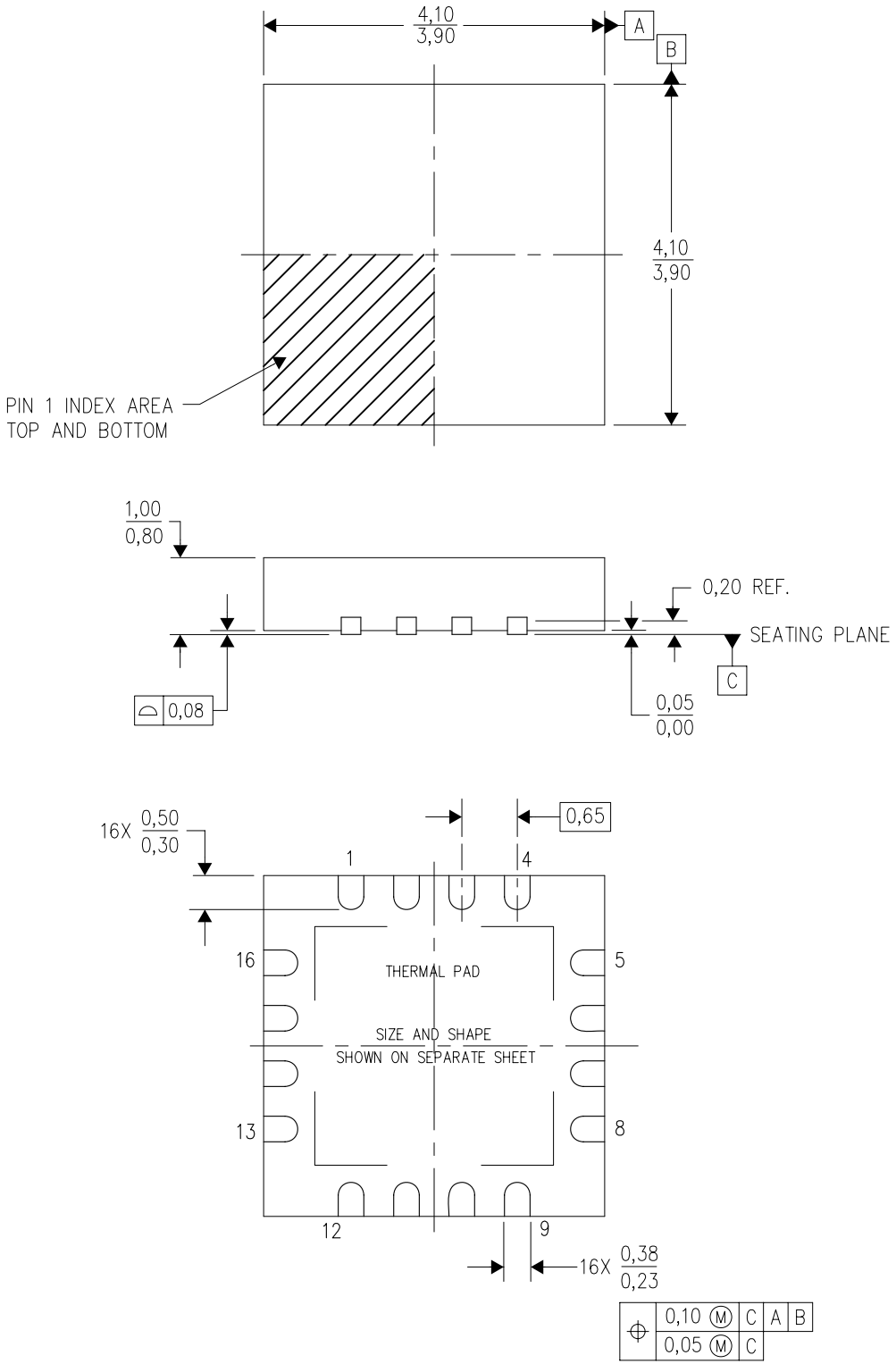
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA5051RSAR	QFN	RSA	16	3000	356.0	356.0	35.0
TPA5051RSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

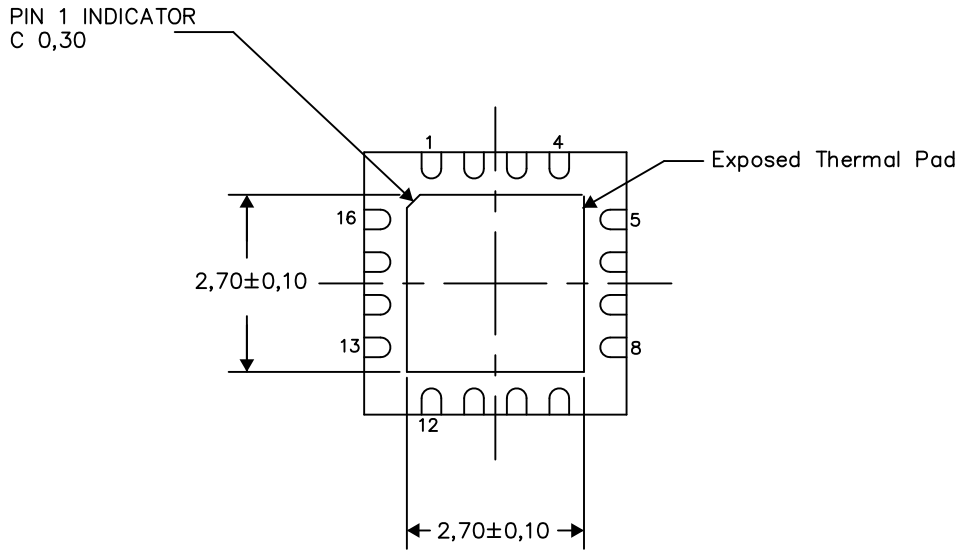
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



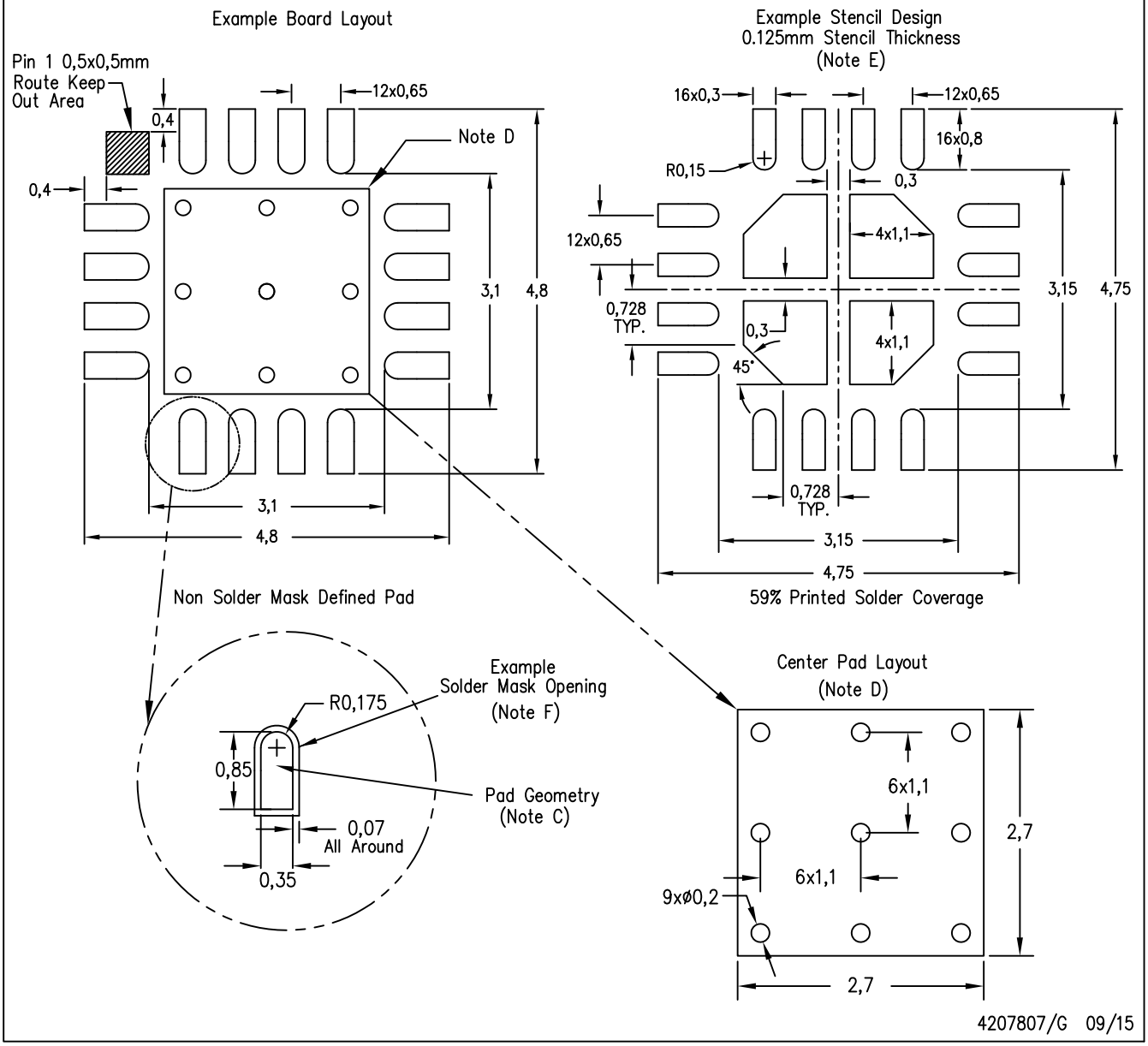
Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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