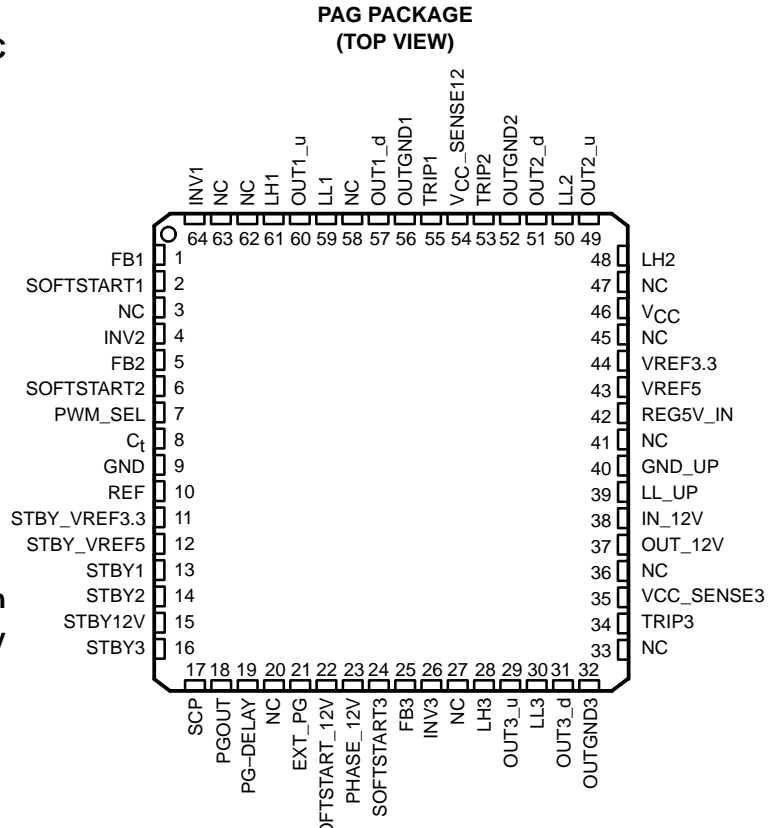


TPS5140 FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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- Three Independent Step-Down DC/DC Controllers and One 12-V Boost DC/DC Converter
- 4.5 V – 28 V Input Voltage Range
- Step-Down Controller Output Voltages Adjustable Down to 1.2 V
- Synchronous-Buck Operation for High Efficiency
- PWM Mode Control
- Auto PWM/SKIP Mode for High Efficiency Under All Load Conditions
- High Speed Error Amplifier
- Separate Standby Control and Over Current Protection for Each Channel
- Over Voltage and Under Voltage Protection
- Programmable Short Circuit Protection
- Power Good With Programmable Delay Time
- 5 V and 3.3 V Linear Regulators



description

The TPS5140 is a dc/dc controller that incorporates three synchronous-buck controllers and one nonsynchronous 12-V boost converter on one chip to power the voltage rails needed by notebook peripheral components. On-chip high-side and low-side synchronous rectifier drivers are integrated to drive less expensive N-channel power MOSFETs. The nonsynchronous boost converter includes the N channel power MOSFET and supports 120 mA for the PCMCIA power supply. The outputs are controlled independently and two of the synchronous-buck controllers operate 180 degrees out of phase, with the third lowering the input current ripple and allowing a smaller input capacitance to reduce power supply cost. For higher efficiency under all load conditions, the TPS5140 automatically adjusts each channel from the PWM mode to the skip mode independently. The skip mode enables a lower operating frequency and shortens the pulse width to the low side MOSFETs, thereby increasing the efficiency under light load conditions. To further extend battery life, the TPS5140 features dead-time control and very low quiescent current. Resistorless current protection and the fixed high-side driver voltage simplify the system design and reduce the external parts count.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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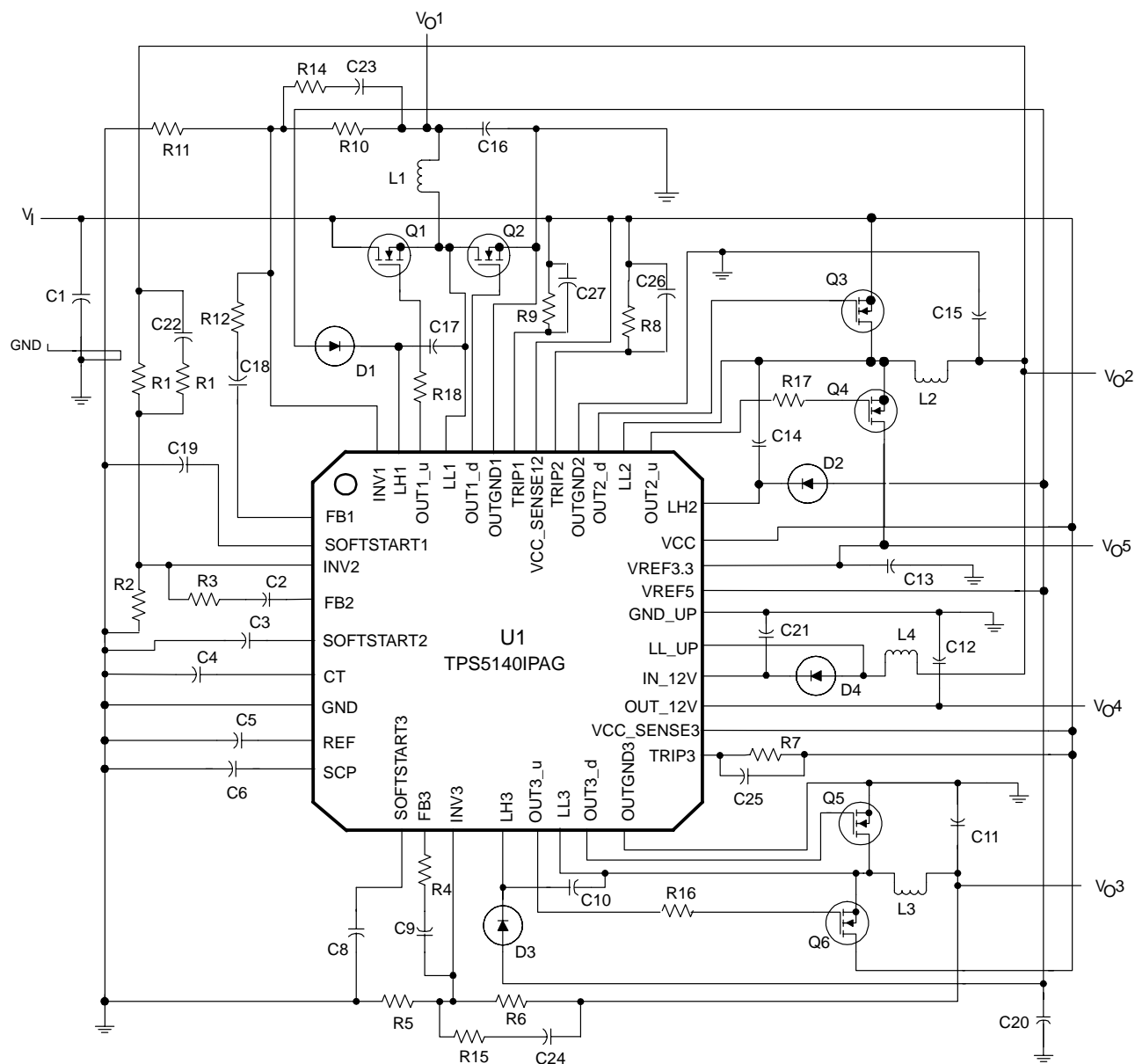
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TPS5140

FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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typical design schematic



AVAILABLE OPTIONS

| T _A | PACKAGE | |
|----------------|--------------|-----|
| | PAG | EVM |
| –20°C to 85°C | TQFP64 (PAG) | |

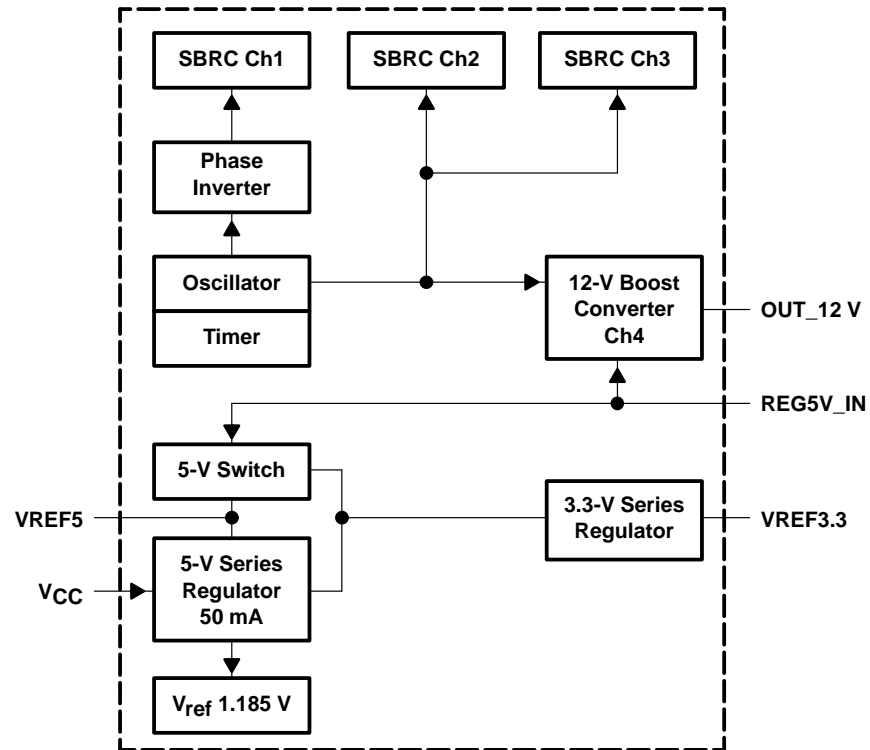


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functional block diagram—whole block

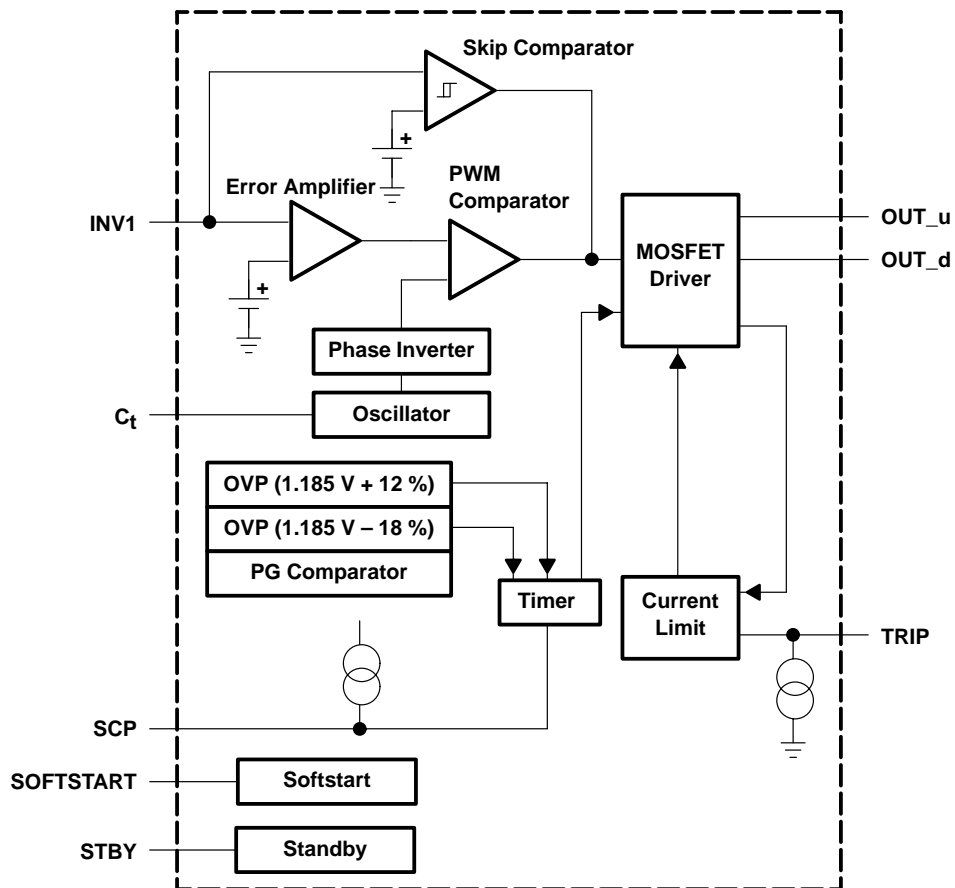


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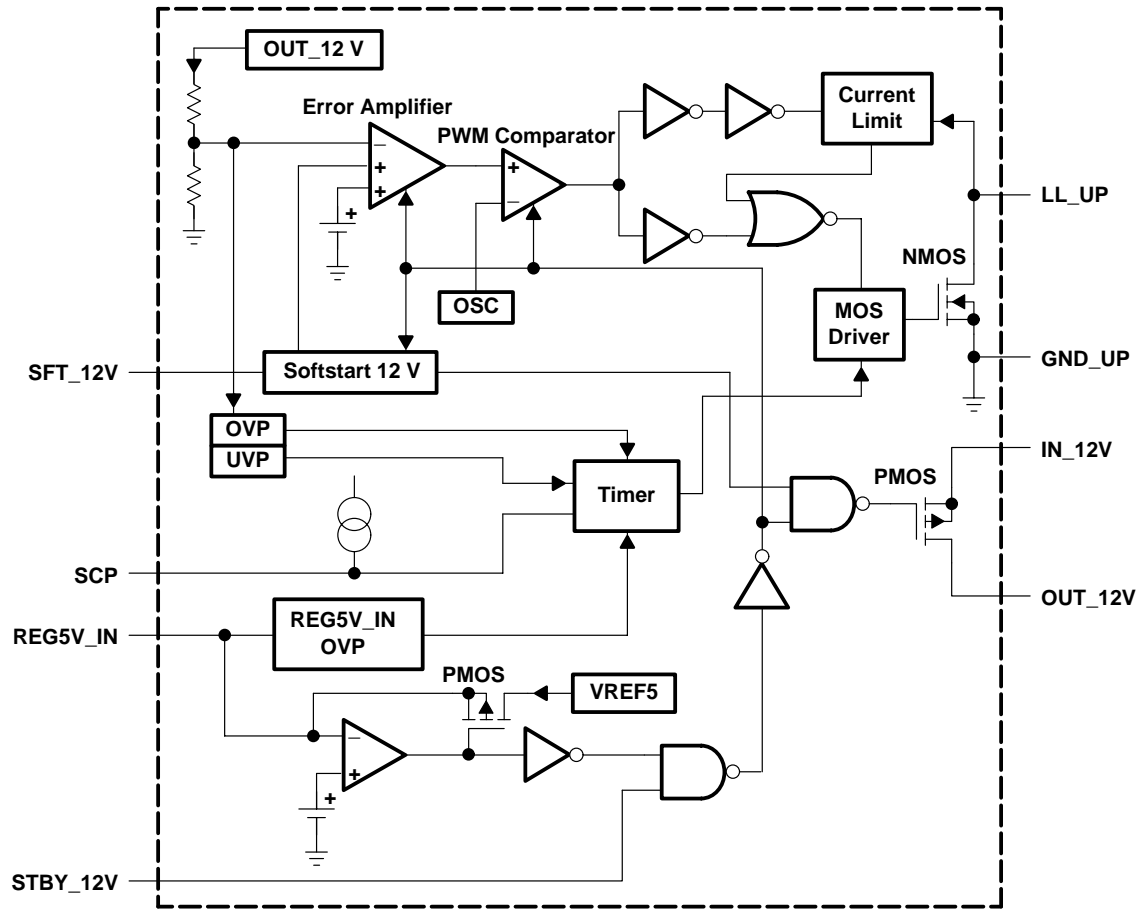
functional block diagram—SMPS block



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functional block diagram—boost 12-V block

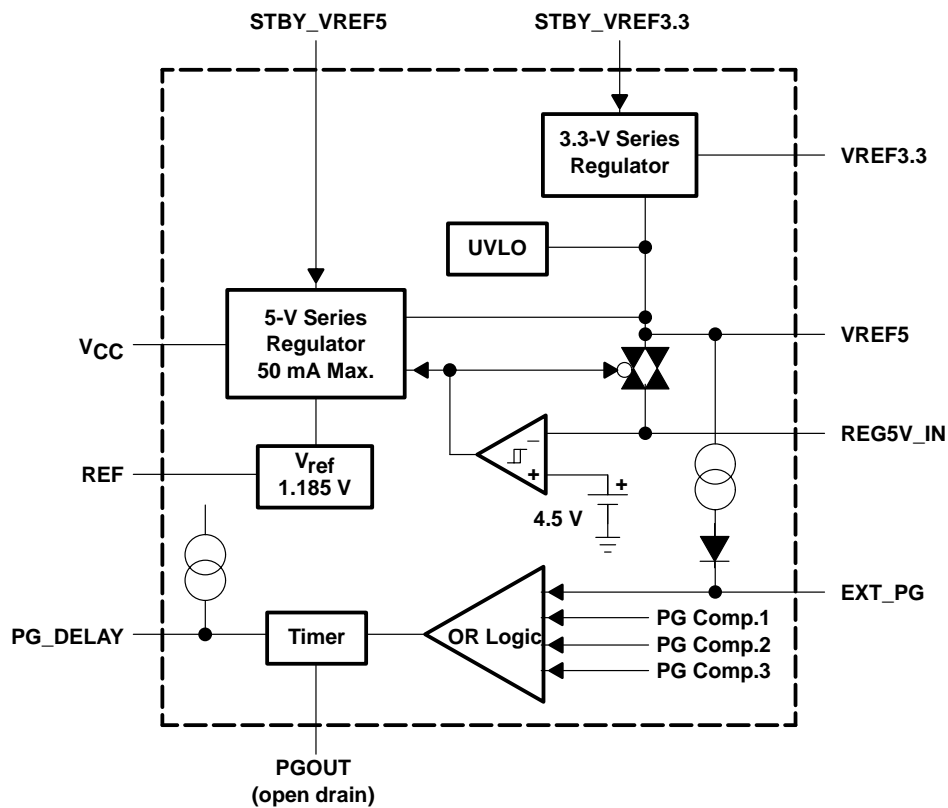


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functional block diagram—power good block



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Terminal Functions

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|--|-----|---|
| C _t | 8 | I/O | External capacitor from C _t to GND used for adjusting the triangle oscillator. |
| EXT_PG | 21 | I | External power good signal input |
| FB1 | 1 | O | Feedback output of CH1 error amplifier |
| FB2 | 5 | O | Feedback output of CH2 error amplifier |
| FB3 | 25 | O | Feedback output of CH3 error amplifier |
| GND | 9 | | Control GND |
| GND_UP | 40 | | Ground for 12-V boost converter |
| INV1 | 64 | I | Inverting input of CH1 error amplifier, skip comparator and OVP1/UVP1, PG comparator |
| INV2 | 4 | I | Inverting input of CH1 error amplifier, skip comparator and OVP2/UVP2, PG comparator |
| INV3 | 26 | I | Inverting input of CH1 error amplifier, skip comparator and OVP3/UVP3, PG comparator |
| IN_12V | 38 | I | Input of PMOS switch for 12-V boost output. Connecting to cathode of the external Schottky diode. |
| LH1 | 61 | I/O | Bootstrap capacitor connection for CH1 high side gate drive |
| LH2 | 48 | I/O | Bootstrap capacitor connection for CH2 high side gate drive |
| LH3 | 28 | I/O | Bootstrap capacitor connection for CH3 high side gate drive |
| LL1 | 59 | I/O | Bootstrap low for CH1 high side gate driving return and output current protection. Connect to the junction of the high side and low side FETs for floating drive configuration. |
| LL2 | 50 | I/O | Bootstrap low for CH2 high side gate driving return and output current protection. Connect to the junction of the high side and low side FETs for floating drive configuration. |
| LL3 | 30 | I/O | Bootstrap low for CH3 high side gate driving return and output current protection. Connect to the junction of the high side and low side FETs for floating drive configuration. |
| LL_UP | 39 | I/O | Open drain output of internal NMOS switch for 12-V boost converter. Connect between external inductor and the anode of the schottky diode. |
| NC | 3,20,27,33, 36,41,45,47 58,62,63 | | No connect |
| OUT1_d | 57 | O | Gate drive output for CH1 low side gate drive |
| OUT2_d | 51 | O | Gate drive output for CH2 low side gate drive |
| OUT3_d | 31 | O | Gate drive output for CH3 low side gate drive |
| OUT1_u | 60 | O | Gate drive output for CH1 high side switching FETs |
| OUT2_u | 49 | O | Gate drive output for CH2 high side switching FETs |
| OUT3_u | 29 | O | Gate drive output for CH3 high side switching FETs |
| OUT_12V | 37 | O | Output of PMOS switch for 12-V boost output. Connect to the output capacitor for 12-V boost output. |
| OUTGND1 | 56 | | Ground for CH1 FETs drivers. It is connected to one of the current limiting comparator input. |
| OUTGND2 | 52 | | Ground for CH2 FETs drivers. It is connected to one of current limiting comparator input. |
| OUTGND3 | 32 | | Ground for CH3 FETs drivers. It is connected to the one of current limiting comparator input. |
| PGOUT | 18 | O | Open drain output for power good signal |
| PG_DELAY | 19 | I/O | Programmable delay for power good. Connect to the external capacitor for timer delay. |
| PHASE_12V | 23 | I | Phase compensation for the 12-V boost converter. Connect to an external capacitor. But normally it is not connected. |
| PWM_SEL | 7 | I | PWM or auto PWM/SKIP modes select L: PWM fixed H: auto PWM/SKIP |
| REF | 10 | O | 1.185 V reference voltage output |



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Terminal Functions(Continued)

| TERMINAL NAME | NO. | I/O | DESCRIPTION |
|------------------|-----|-----|--|
| REG5V_IN | 42 | I | External 5 V input |
| SCP | 17 | I/O | Short circuit protection terminal. An external capacitor is connected between SCP and GND to set the SCP enable time up. |
| SOFTSTART1 | 2 | I/O | External capacitor from SOFTSTART1 to GND for CH1 soft starts control. |
| SOFTSTART2 | 6 | I/O | External capacitor from SOFTSTART2 to GND for CH2 soft starts control. |
| SOFTSTART3 | 24 | I/O | External capacitor from SOFTSTART3 to GND for CH3 soft starts control. |
| SOFTSTART_12V | 22 | I/O | External capacitor from SOFTSTART_12V to GND for CH4 (12-V boost converter) soft starts control. |
| STBY1 | 13 | I | Stand by control for CH1 |
| STBY2 | 14 | I | Stand by control for CH2 |
| STBY3 | 16 | I | Stand by control for CH3 |
| STBY12V | 15 | I | Stand by control for 12-V boost converter |
| STBY_VREF3.3 | 11 | I | Stand by control for 3.3-V linear regulator |
| STBY_VREF5 | 12 | I | Stand by control for 5-V linear regulator |
| TRIP1 | 55 | I | External resistor connection for CH1 output current protection control |
| TRIP2 | 53 | I | External resistor connection for CH2 output current protection control |
| TRIP3 | 34 | I | External resistor connection for CH3 output current protection control |
| VCC | 46 | | Supply voltage input |
| VCC_SENSE12 | 54 | I | Supply voltage input and input voltage terminal for CH1/2 output current sense |
| VCC_SENSE3 | 35 | I | Supply voltage input and input voltage terminal for CH3 output current sense |
| VREF3.3 | 44 | O | 3.3-V linear regulator output |
| VREF5 | 43 | O | 5-V linear regulator output |

detailed description

REF (1.185 V)

The reference voltage is used for setting the output voltage and voltage protection. This reference voltage is dropped down from the 5-V regulator. The tolerance is 1.5 % over the entire temperature range.

CH1, 2, 3 (synchronous buck controller)

The TPS5140 includes three synchronous buck controllers. CH2 and CH3 (5 V and 2.5 V) are operated in phase, but CH1 (3.3 V) is operated 180° out of phase from CH2 and CH3, but at the same frequency. All channels have separate standby and softstart control.

12-V boost converter

OUT_12V is a 12-V boost converter output . It can isolate V_I (5 V) and V_O fully.

5-V regulator

An internal linear voltage regulator is used for the high-side driver bootstrap voltage and as the source of V_{ref} . When the 5-V regulator is disconnected from the MOSFET drivers, it is used only for the source of V_{ref} . Since the input voltage is from 4.5 V to 28 V, this feature offers a fixed bootstrap voltage to simplify the drive design. The 5-V regulator is also used for powering the low side driver. The 5-V regulator is active if STBY_VREF5 is high and has a tolerance of 4%.



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detailed description (continued)

3.3-V regulator

TPS5140 has a 3.3-V linear regulator. The output is made from the internal 5 V regulator or external 5 V from REG5V_IN. The 3.3-V regulator has an output current limit. The maximum output current is 30 mA.

5-V switch

If the internal 5-V switch senses a 5-V input from the REG5V_IN terminal, the internal 5-V linear regulator will be disconnected from the MOSFET drivers. The external 5 V will be used for both the low-side driver and the high-side bootstrap, thus increasing the efficiency.

auto PWM/SKIP

The PWM_SEL terminal selects either the auto PWM/SKIP or fixed PWM mode. If this terminal is lower than 0.5 V, the outputs operate in the fixed PWM mode. If 2.5 V (minimum) is applied, the outputs operate in auto PWM/SKIP mode. In the auto PWM/SKIP mode, the operation changes from the PWM mode to the SKIP mode automatically under light load conditions. Avoid using a MOSFET with very low $r_{DS(on)}$ if the auto SKIP function is implemented.

error amp

All three synchronous buck channels have their own error amplifier to regulate the output. The error amplifier is used in the PWM mode for high output current conditions (> 0.2 A). Voltage mode control is implemented.

skip comparator

In skip mode, all three synchronous buck channels have their own hysteresis comparator to regulate the output voltages. The hysteresis voltage is set internally and typically at 8.5 mV. The delay from the comparator input to the driver output is typically 1.2 μ s.

low-side driver

The low-side driver is designed to drive low- $r_{DS(on)}$ n-channel MOSFETs. The maximum drive voltage is 5 V from VREF5. Ch1, 2, and 3 MOSFET driver capability is 1.5 A, source and sink.

high-side driver

The high-side driver is designed to drive low- $r_{DS(on)}$ n-channel MOSFETs. CH1 and CH2 MOSFET drivers have 1.2 A capability, source and sink. When configured as a floating driver, the bias voltage to the driver is developed from VREF5, limiting the maximum drive voltage between OUT_u and LL to 5 V. The maximum voltage that can be applied between LHx and OUTGND is 33 V.

dead time

Dead time prevents shoot-through current from flowing through the main power MOSFETs during switching transitions by actively controlling the turnon time of the MOSFETs drivers.

current protection

Current protection is achieved by sensing the drain-to-source voltage drop of the low-side power MOSFET during the low-side MOSFET's on time at OUTGND and LL. An external resistor between V_{CC}_SENSE and TRIP terminal in series with the internal current source adjusts the current limit. When the voltage drop during the low-side MOSFET on-time is high enough, the current comparator triggers the current protection and the MOSFET drivers are turned off. After a programmable time delay, the SCP circuit latches off all MOSFET drivers. The internal current source tolerance is $\pm 10\%$. CH2 monitors both high-side and low-side MOSFET voltage drops.

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detailed description (continued)

OVP

For over voltage protection, the TPS5140 monitors INV terminal voltage. When the INV voltage becomes higher than 1.185 V (+12%), the OVP comparator output becomes high and the SCP timer starts to charge the SCP capacitor. After a programmable time delay, the SCP circuit forces CH1, 2, 3 high-side MOSFET drivers to latch off and the low-side MOSFET drivers to latch on.

UVP

For under voltage protection, the TPS5140 monitors INV terminal voltage. When the INV voltage becomes lower than 1.185 V (–18 %), the UVP comparator output becomes high and the SCP timer starts to charge the SCP capacitor. Also, when the current comparator of CH1, 2, 3 triggers the OCP, the UVP comparator detects the under voltage output and the SCP capacitor starts to charge. After the programmable time delay, the SCP circuit forces the CH1, 2, 3 MOSFET drivers to latch off.

SCP

When an OVP or UVP comparator output becomes high, the SCP circuit starts to charge the SCP capacitor. The charging source current value is different between OVP alert and UVP alert.

$$\text{SCP source current (OVP)} = \text{SCP source current (UVP)} \times 5$$

The threshold voltage of SCP comparator is 1.185 V.

power good

The power good output reports the output fail condition. PG comparators monitor an under voltage or over voltage of CH1, 2, 3, with a threshold of –7 % and 7 %. TPS5140 has an EXT_PG terminal, which can be used for the input of an external PG signal. Delay time is programmable by charging an external capacitor on the PG_DELAY terminal.

SOFTSTART1, 2, 3

Separate soft start terminals make it possible to customize the start-up time of each output. The voltage on the charging softstart capacitor gradually raises, limiting the surge current and voltage. A soft start is initiated when the STBY terminals are switched.

STBY1, 2, 3, 12V

CH1, 2, 3 and 12V can be switched into standby mode separately by grounding the STBY terminal.

STBY_VREF3.3, 5V

STBY_VREF3.3 shuts down the 3.3-V regulator by grounding the STBY_VREF3.3 terminal. When STBY_VREF5 is high, only the 5-V regulator is operating.

UVLO

When the input voltage exceeds 4 V, the IC is turned on and is ready to function. When the input voltage is lower than the turn on value, the IC is turned off. The typical hysteresis voltage is 40 mV.

phase inverter

The phase inverter controls the phase of CH1 and CH2, 3. CH2, 3 operate in the same phase as OSC. CH1 operates 180° out of phase from OSC. Out-of-phase operation enables a smaller input capacitor.

OVP (12-V boost converter)

The TPS5140 monitors over voltage of the 12-V boost converter. When an output over voltage is detected, the timer starts to charge an external capacitor that is connected to the SCP terminal. After a programmable time delay, the SCP circuit forces all (CH1, 2, 3 and 12 V) MOSFET drivers to latch-off.



detailed description (continued)

UVP (12-V boost converter)

TPS5140 monitors output under voltage of the 12-V boost converter. When an output under voltage is detected, the timer starts to charge an external capacitor that is connected to the SCP terminal. After a programmable time delay, the SCP circuit forces all (CH1, 2, 3, and 12 V) MOSFETs drivers to latch off.

SOFTSTART_12V

An internal capacitor exists for 12-V soft start. If the soft start time needs to be extended, an external capacitor should be connected to this terminal. The 12-V boost converter must start when REG5V_IN terminal is over 4.5 V.

current limit of 12-V boost converter

The 12-V boost current limit monitors the current flowing through the internal MOSFET. When the voltage drop across the internal N-channel MOSFET is high enough during its on time, the current limit circuit forces the internal N-channel MOSFET to turn off.

PHASE_12V

The 12-V boost converter does not typically require phase compensation. If there is reason to change the phase, the 12-V boost converter can be phase compensated by inserting external resistors and capacitors to GND. Otherwise, the PHASE_12V terminal should be left open.

logic charts

Table 1. Logic Chart1

| STBY1 | STBY2 | STBY3 | CH1 | CH2 | CH3 | PGOUT |
|-------|-------|-------|---------|---------|---------|---------------------|
| L | L | L | Disable | Disable | Disable | N/A |
| L | L | H | Disable | Disable | Enable | Active [†] |
| L | H | L | Disable | Enable | Disable | Active [†] |
| L | H | H | Disable | Enable | Enable | Active [†] |
| H | L | L | Enable | Disable | Disable | Active [†] |
| H | L | H | Enable | Disable | Enable | Active [†] |
| H | H | L | Enable | Enable | Disable | Active [†] |
| H | H | H | Enable | Enable | Enable | Active [†] |

[†] During softstart, PGOUT is active low.

Table 2. Logic Chart2

| STBY_VREF5 | STBY_VREF3.3 | VREF5 [‡] | VREF3.3 |
|------------|--------------|--------------------|---------|
| L | L | N/A | Disable |
| H | L | Enable | Disable |
| L | H | Enable | Enable |
| H | H | Enable | Enable |

[‡] To disable VREF5, all STBY1, 2, 3, STBY_VREF3.3 and STBY_VREF5 must be L.

Table 3. Logic Chart3

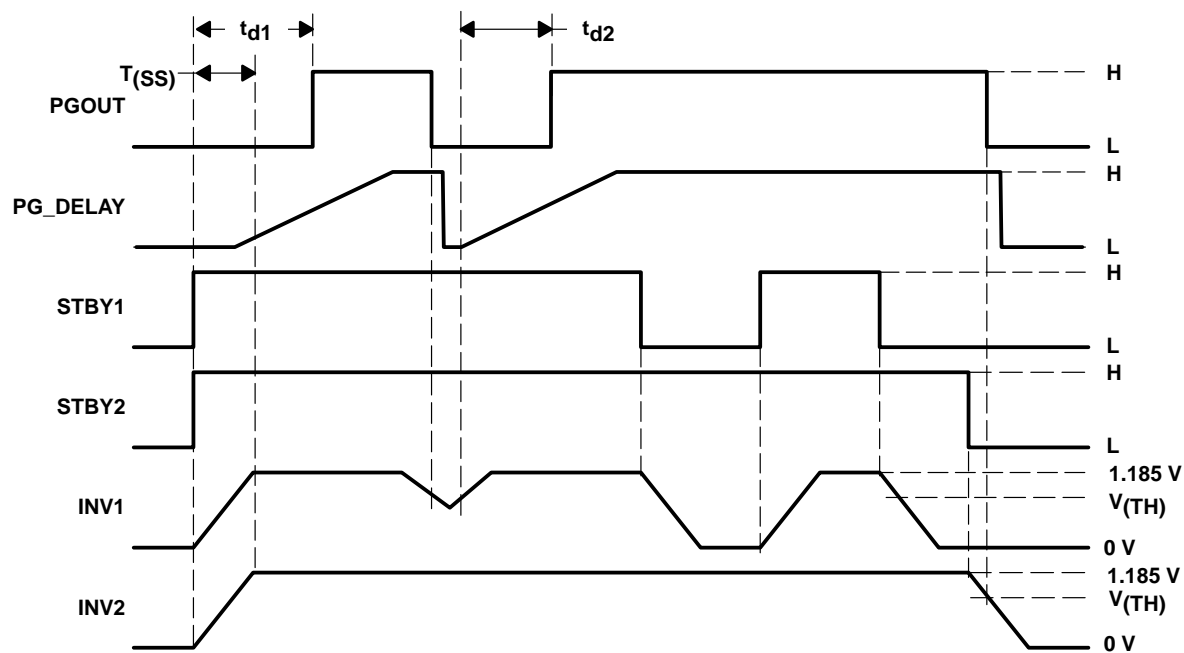
| STBY12V | REG5V_IN | 12 VOUT |
|---------|----------|---------|
| L | L | Disable |
| L | H | Disable |
| H | L | Disable |
| H | H | Enable |

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PGOUT timing chart



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | –0.3 V to 30 V |
| Input voltage; INV1/2/3, CT, PWM_SEL, REG5V_IN, SOFTSTART1/2/3, SOFTSTART_12V | –0.3 V to 7 V |
| SCP, PG_DELAY, PHASE_12V, OUT1/2/3_d, VREF3.3/5, FB1/2/3 | –0.3 V to 7 V |
| PGOUT, EXT_PG | –0.3 V to 7 V |
| STBY1/2/3/12V, STBY_VREF3.3/5, TRIP1/2/3 | –0.3 V to 30 V |
| VCC_SENSE12/3, LL1/2/3 | –0.3 V to 30 V |
| LL_UP, OUT_12V, IN_12V | –0.3 V to 16 V |
| LH1/2/3, OUT1/2/3_u | –0.3 V to 35 V |
| REF | –0.3 V to 3 V |
| Operating free-air temperature range, T_A (see Note 3) | –20°C to 85°C |
| Storage temperature range, T_{stg} | –55°C to 155°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to the network ground terminal.
 2. This rating is specified at duty = 10% on output rise and fall each pulse. Each pulse width (rise and fall) for the peak current should not exceed 2 μ s.
 3. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER DISSIPATION | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER DISSIPATION |
|---------|--|---|---|
| PAG | 1811 mW | 14.49 mW/°C | 941.6 mW |

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|--|------|-----|-----|------|
| Supply voltage, V _{CC} | | 4.5 | | 28 | V |
| Input voltage, V _I | INV1/2/3, CT, PG_DELAY, PWM_SEL SOFTSTART1/2/3 SOFT-START_12V, SCP PHASE_12V, PGOUT, EXT_PG, | | | 6 | V |
| | REG5V_IN | −0.1 | | 5.5 | |
| | STBY1/2/3/12V STBY_VREF3.3/5, TRIP1/2/3, V _{CC} _SENSE12/3 | −0.1 | | 28 | |
| | OUT1/2/3_u, LH1/2/3 | −0.1 | | 33 | |
| | LL_UP, OUT_12V, IN_12V | −0.1 | | 15 | |
| Oscillator frequency, f _{OSC} | CT capacitance‡ | 44 | | | pF |
| Operation temperature range, T _A | | −20 | | 85 | °C |

[‡] The recommended maximum operating frequency is typically 300 kHz.

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7$ V (unless otherwise noted)

reference voltage

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-------|-------|------|------|
| V_{ref} Reference voltage | | | 1.185 | | V |
| $V_{ref(tol)}$ Reference voltage tolerance | $T_A = 25^\circ\text{C}$, $I_{(vref)} = 50 \mu\text{A}$ | –1% | | 1% | |
| | $I_{(vref)} = 50 \mu\text{A}$ | –1.5% | | 1.5% | |
| Line regulation | $V_{CC} = 4.5$ V to 28 V, $I_{(vref)} = 50 \mu\text{A}$ | | 0.05 | 3 | mV |
| Load regulation | $I_{(vref)} = 0.1 \mu\text{A}$ to 1 mA | | 0.15 | 5 | mV |



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7\text{ V}$ (unless otherwise noted) (continued)

oscillator

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---------------------------|--|-----|------|-----|------|
| f_{osc} | Frequency | PWM mode, $CT = 56\text{ pF}$, $T_A = 25^\circ\text{C}$ | | 250 | | kHz |
| $V_{OS(CH)}$ | High-level output voltage | DC | 1 | 1.1 | 1.2 | V |
| | | $f_{osc} = 250\text{ kHz}$ | | 1.17 | | |
| $V_{OS(CL)}$ | Low-level output voltage | DC | 0.4 | 0.5 | 0.6 | V |
| | | $f_{osc} = 250\text{ kHz}$ | | 0.43 | | |

error amplifier

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|------------------------|--------------------------|-----|-----|-----|------|
| V_{IO} | Input offset voltage | $T_A = 25^\circ\text{C}$ | | 2 | 10 | mV |
| $A(V)$ | Open-loop voltage gain | | | 90 | | dB |
| $G(B)$ | Unity-gain bandwidth | | | 2.5 | | MHz |
| $I_{(snk)}$ | Output sink current | $V_O = 1\text{ V}$ | 0.3 | 0.7 | | mA |
| $I_{(src)}$ | Output source current | | 0.4 | 0.9 | | |

duty control

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|---------------------------------------|-----|-----|-----|------|
| Maximum duty cycle | | CH1/3, $f_{osc} = 250\text{ kHz}$ | 75% | | | |
| | | CH2, $f_{osc} = 250\text{ kHz}$ | 85% | | | |
| | | 12V boost, $f_{osc} = 250\text{ kHz}$ | | 70% | | |

control

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------|--|-----|-----|-----|------|
| V_{IH} | High-level input voltage | STBY1/2/3/12V, EXT_PGPWM_SEL, STBY_VREF5/3.3 | 2 | | | V |
| V_{IL} | Low-level input voltage | STBY1/2/3/12V, EXT_PGPWM_SEL, STBY_VREF5/3.3 | | | 0.3 | V |

5-V internal switch

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|-------------------|------|-----------------|--|-----|-----|-----|------|
| $V_{(TLH)}$ | Threshold voltage | High | REG5V_IN | | 4.2 | | 4.8 | V |
| $V_{(THL)}$ | | Low | REG5V_IN | | 4.1 | | 4.7 | |
| V_{hys} | Hysteresis | | | | 30 | | 200 | mV |

VREF5

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-------------|------------------------------|------|---|--|-----|-----|-----|------|
| V_O | Output voltage | | $I_O = 0\text{ mA to }50\text{ mA}$, $V_{CC} = 5.5\text{ V to }28\text{ V}$, $T_A = 25^\circ\text{C}$ | | 4.8 | | 5.2 | V |
| | Line regulation | | $V_{CC} = 5.5\text{ V to }28\text{ V}$, $I_O = 10\text{ mA}$ | | | | 20 | mV |
| | Load regulation | | $I_O = 1\text{ mA to }10\text{ mA}$, $V_{CC} = 5.5\text{ V}$ | | | | 40 | mV |
| I_{OS} | Short circuit output current | | $V_{ref} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ | | 65 | | | mA |
| $V_{(TLH)}$ | UVLO threshold voltage | High | VREF5 voltage | | 3.6 | | 4.2 | V |
| $V_{(THL)}$ | | Low | | | 3.5 | | 4.1 | |
| V_{hys} | Hysteresis | | VREF5 voltage | | 30 | | 200 | mV |



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electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 7\text{ V}$ (unless otherwise noted) (continued)

VREF3.3

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|------------------------------|---|------|------|------|------|
| V_O | Output voltage | $I_O = 0\text{ mA to }30\text{ mA}$, $V_{CC} = 5.5\text{ V to }28\text{ V}$, $T_A = 25^\circ\text{C}$ | 3.15 | 3.30 | 3.45 | V |
| | Line regulation | $V_{CC} = 5.5\text{ V to }28\text{ V}$, $I_O = 10\text{ mA}$ | | | 20 | mV |
| | Load regulation | $I_O = 1\text{ mA to }10\text{ mA}$, $V_{CC} = 5.5\text{ V}$ | | | 40 | mV |
| I_{OS} | Short circuit output current | $V_{ref} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ | -40 | | | mA |

output

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|------------------|--|------|------|-----|---------------|
| OUT_u | Sink current | $V_O = 3\text{ V}$ | | 1.2 | | A |
| | Source current | $V_O = 2\text{ V}$ | | -1.2 | | |
| OUT_d | Sink current | $V_O = 3\text{ V}$ | | 1.5 | | A |
| | Source current | $V_O = 2\text{ V}$ | | -1.5 | | |
| LL_UP | Sink current | $V_{LL_UP} = 0.3\text{ V}$, $OUT_12V = 12\text{ V}$ | | 0.65 | | A |
| OUT_12V | Output impedance | $IN_12V = 12\text{ V}$, $I_{OUT_12V} = 150\text{ mA}$ | | 1.1 | | Ω |
| $I_{(TRIP)}$ | TRIP current | $TRIP1/2/3$, $T_A = 25^\circ\text{C}$ | 11.5 | 13 | 15 | μA |

softstart

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--------------------|-----------------|------|--------|------|---------------|
| $I_{(CTRL)}$ | Soft start current | Softstart1/2/3 | -1.6 | -2.3 | -2.9 | μA |
| | | Softstart_12V | | -0.007 | | |

output voltage monitor

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-------------------------|---|------|------|------|---------------|
| OVP comparator threshold voltage | | CH1/2/3 | 1.28 | 1.33 | 1.38 | V |
| | | 12 V boost | 12.9 | 13.4 | 13.9 | |
| UVP comparator threshold voltage | | CH1/2/3 | 0.90 | 0.95 | 1 | V |
| | | 12 V boost | 9 | 9.5 | 10 | |
| PG comparator threshold voltage | | PG comparator1/2/3, upper threshold | 1.22 | 1.27 | 1.32 | V |
| | | PG comparator1/2/3, lower threshold | 1.05 | 1.1 | 1.15 | |
| PG propagation delay from INV to PG_OUT | | INV = 0.985 V to 1.185 V, PG_DELAY = open | | 3.7 | | μs |
| | | INV = 1.185 V to 0.985 V, PG_DELAY = open | | 8.9 | | |
| I_{PG_DELAY} | PG_DELAY source current | | 1.1 | 1.7 | 2.3 | μA |
| $I_{(SCP)}$ | SCP source current | UVP protection | 1.5 | 2.3 | 3.1 | μA |
| | | OVP protection | 8 | 11.5 | 15 | |

whole device

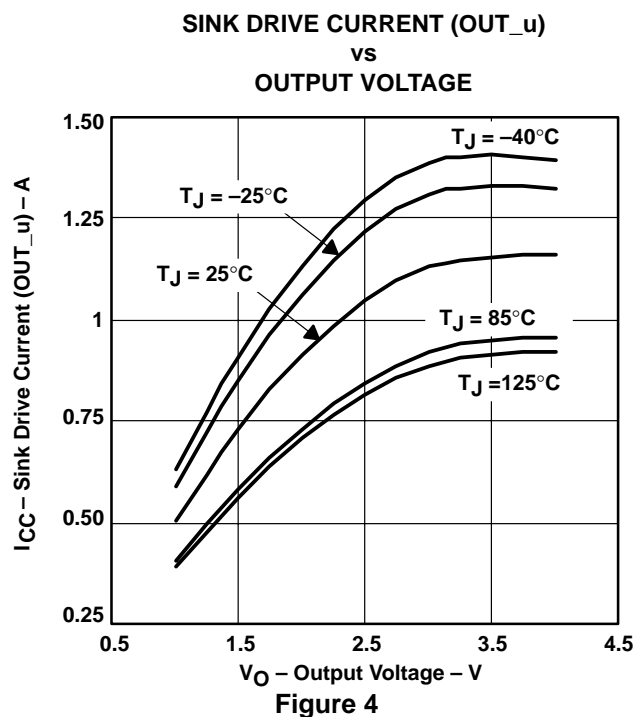
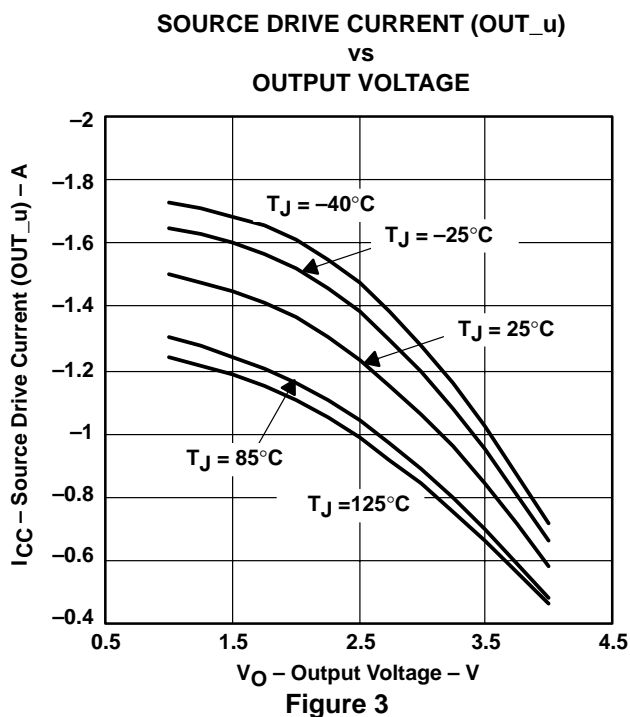
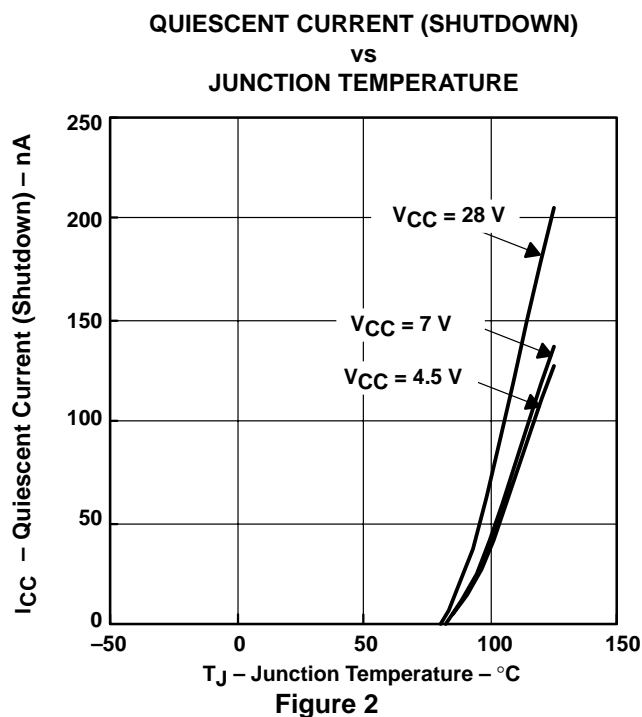
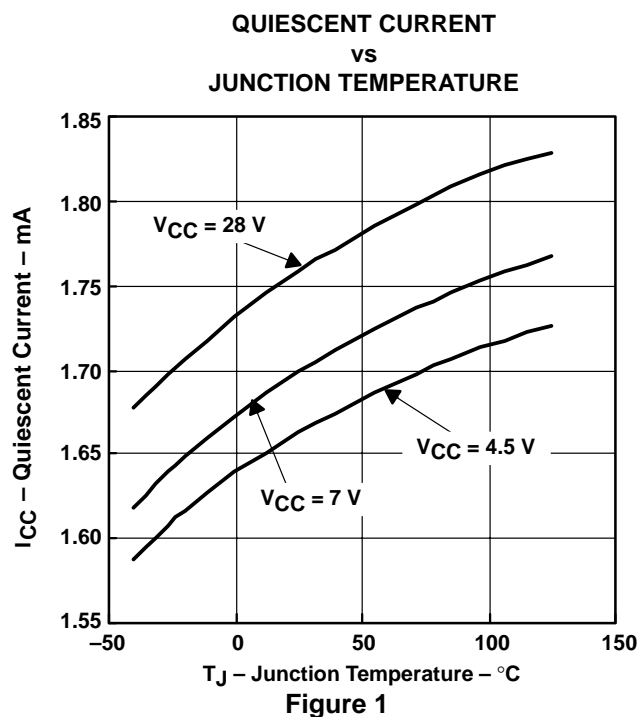
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|------------------|-------------------------------------|-----|-------|-----|---------------|
| I_{CC} | Supply current | | | 1.8 | 2.6 | mA |
| $I_{O(SD)}$ | Shutdown current | STBY1/2/3/12V, STBY_VREF5/3.3 = 0 V | | 0.001 | 10 | μA |



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TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

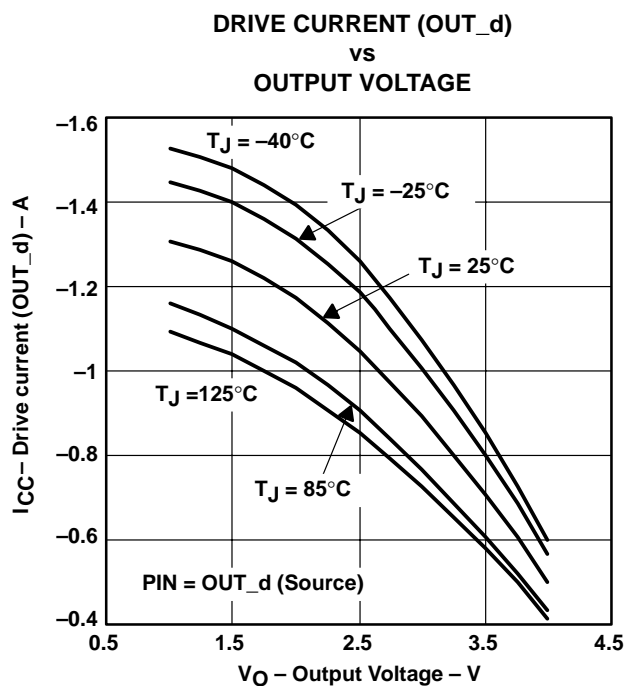


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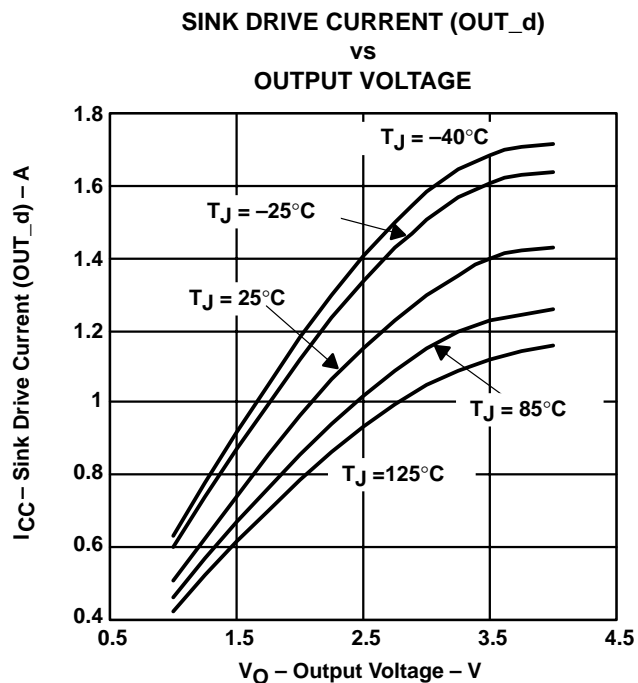


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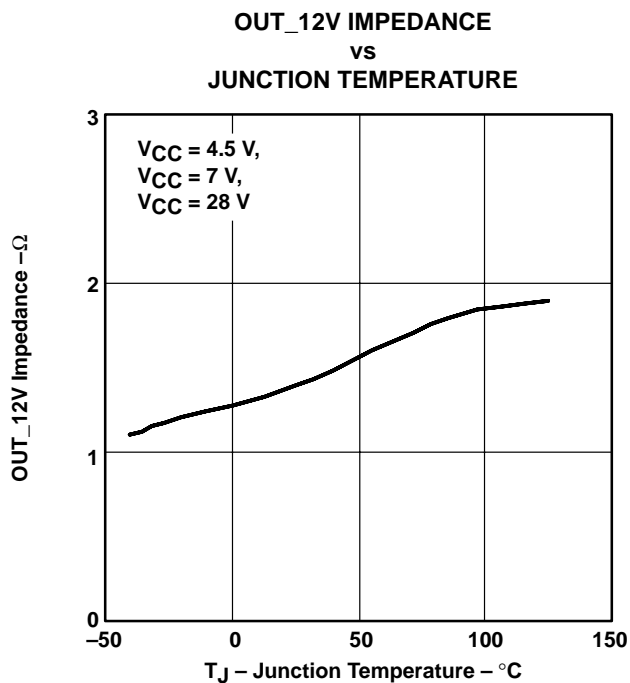


Figure 7

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TYPICAL CHARACTERISTICS

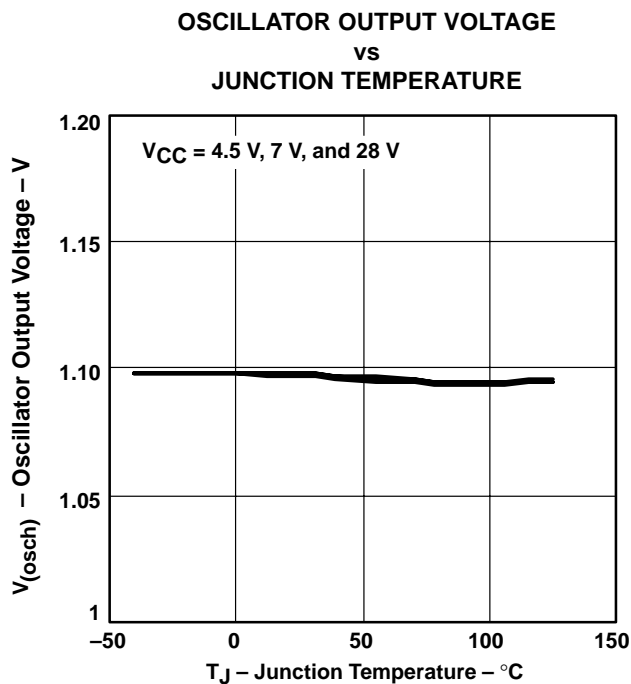


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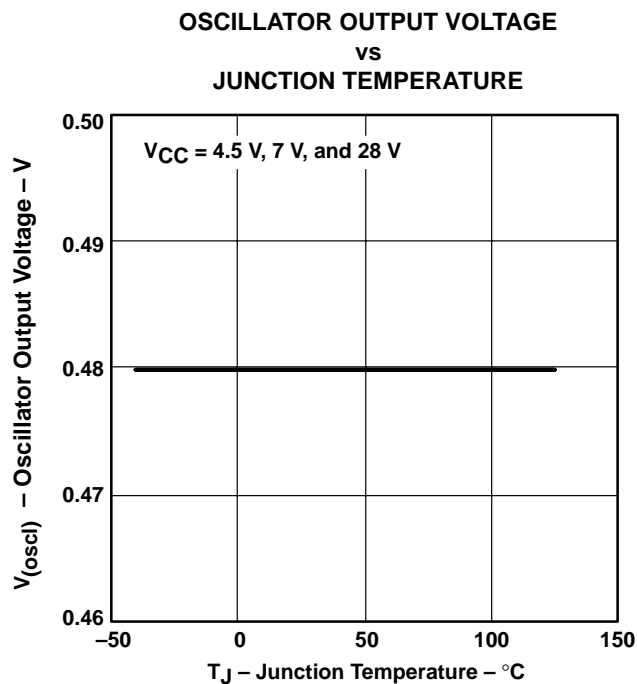


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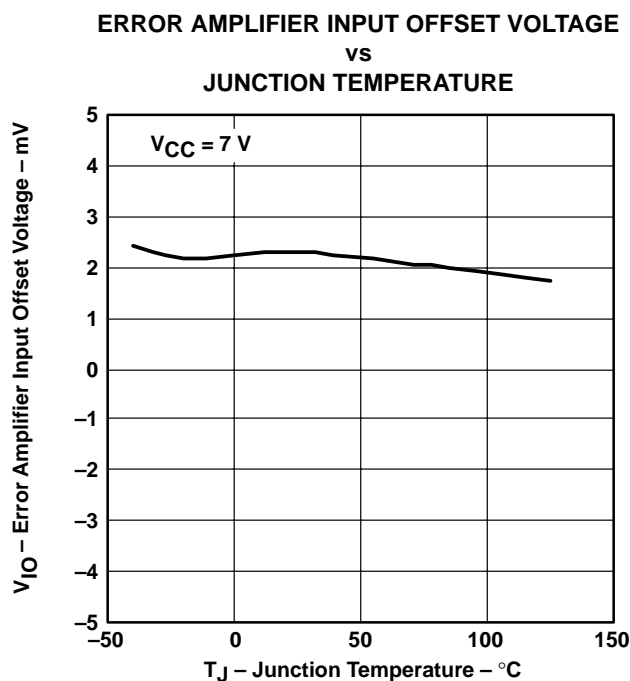


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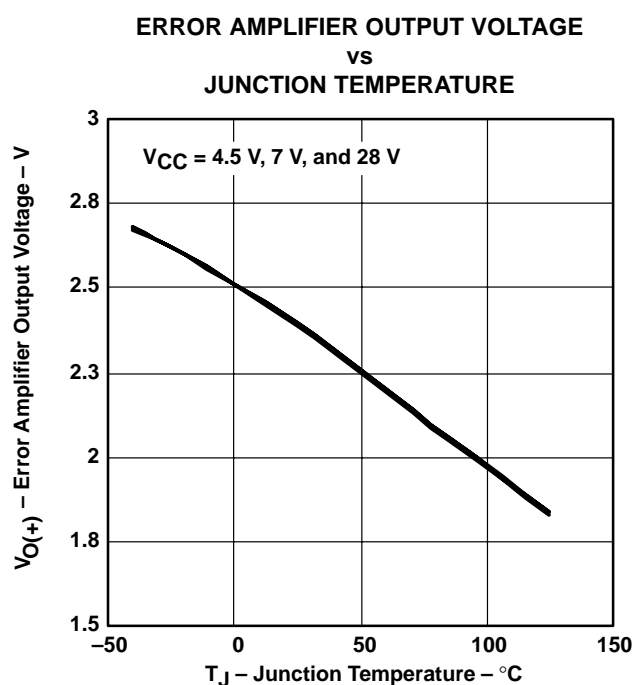


Figure 11

TYPICAL CHARACTERISTICS

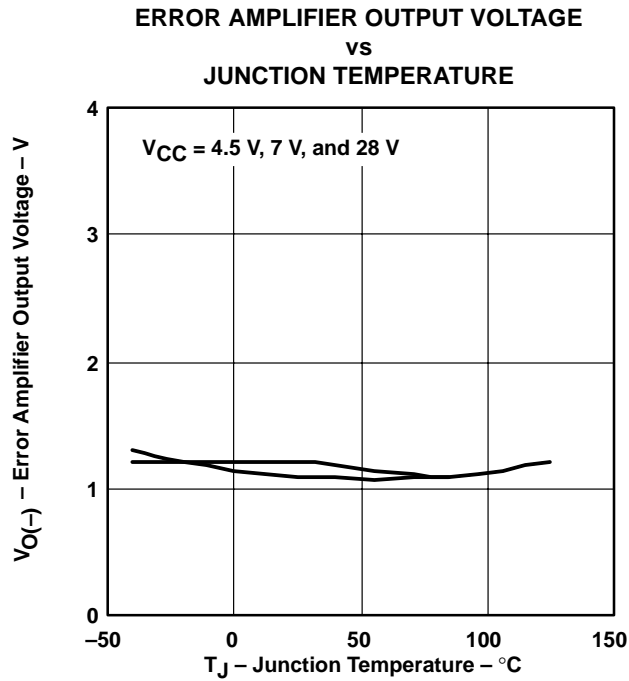


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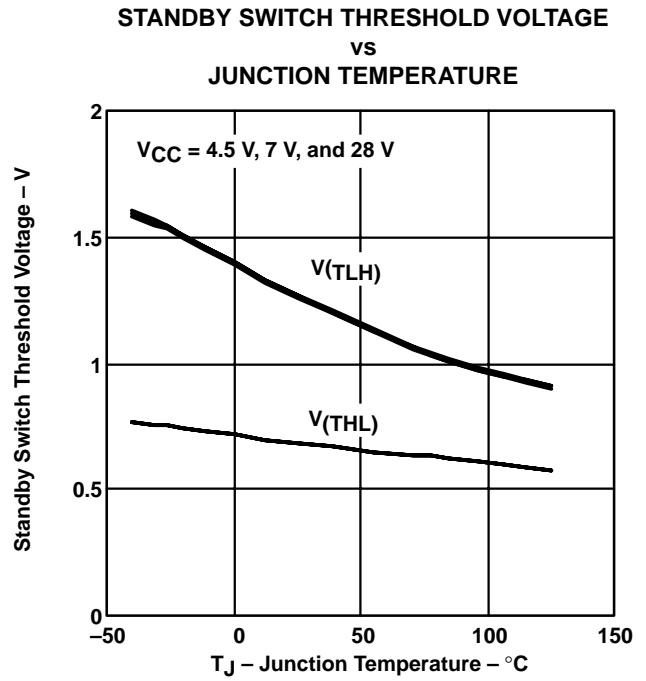


Figure 13

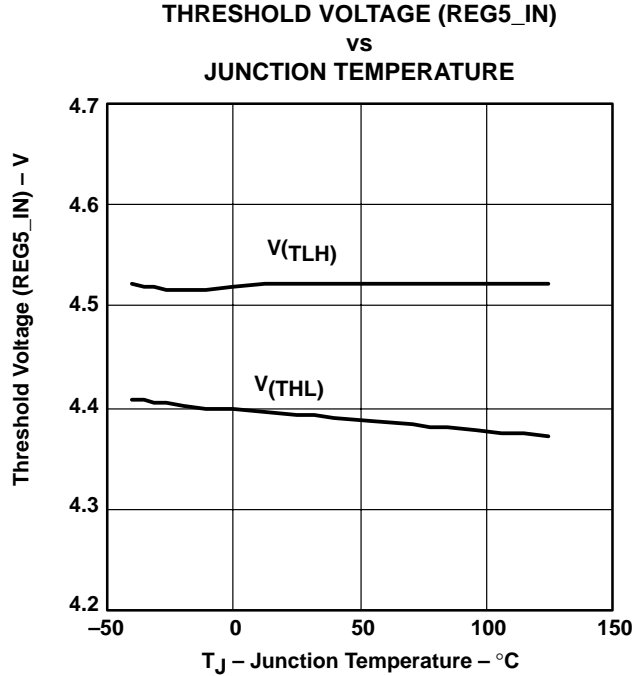


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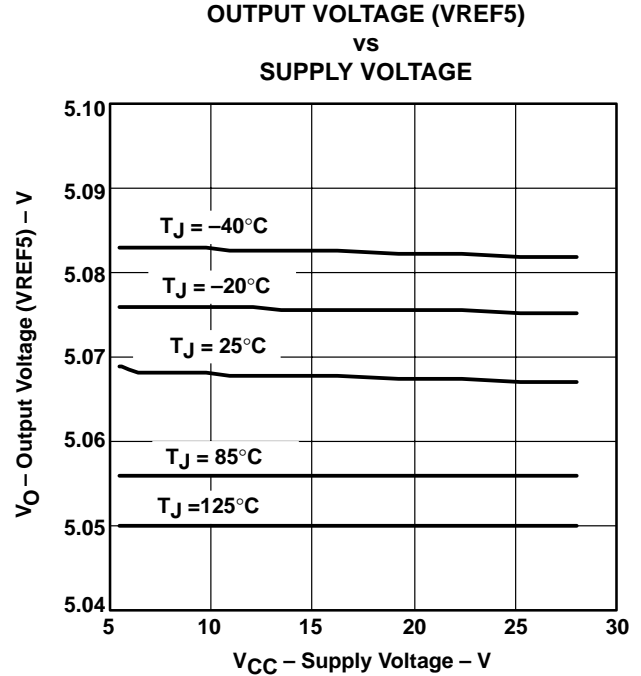


Figure 15

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TYPICAL CHARACTERISTICS

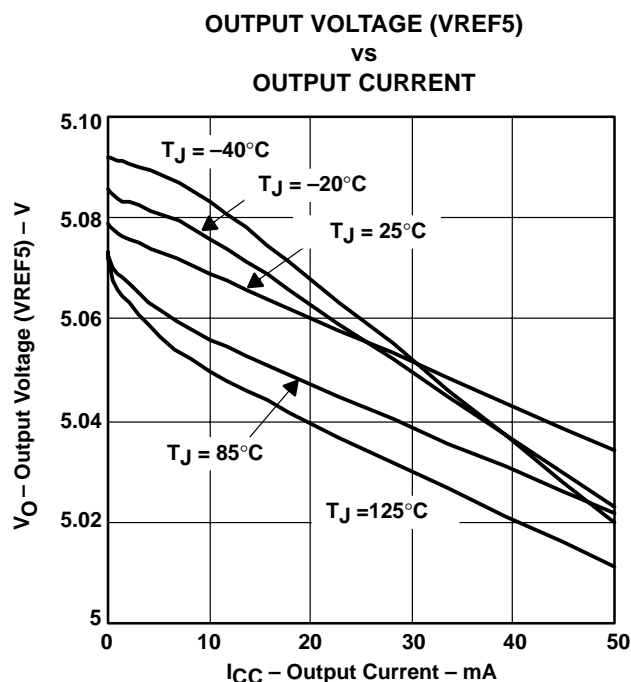


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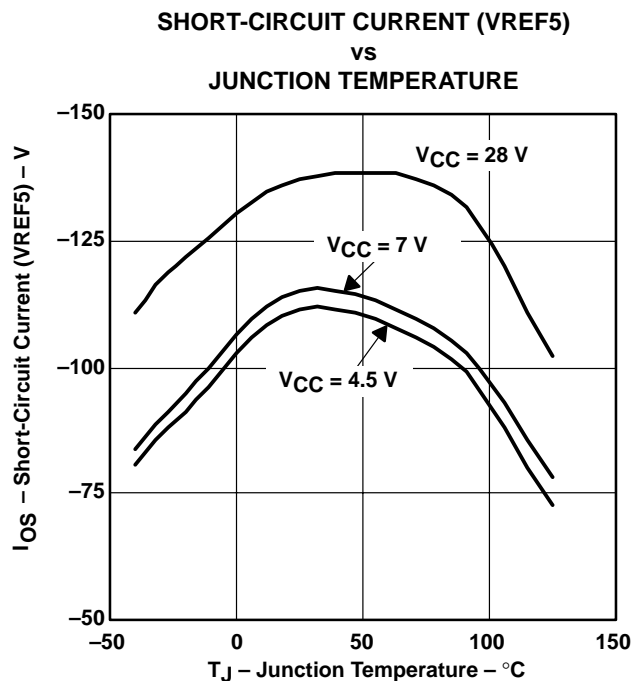


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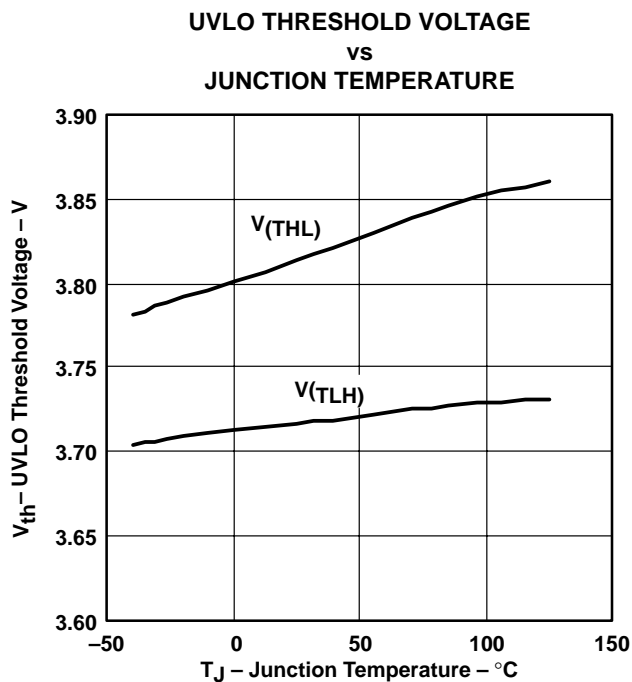


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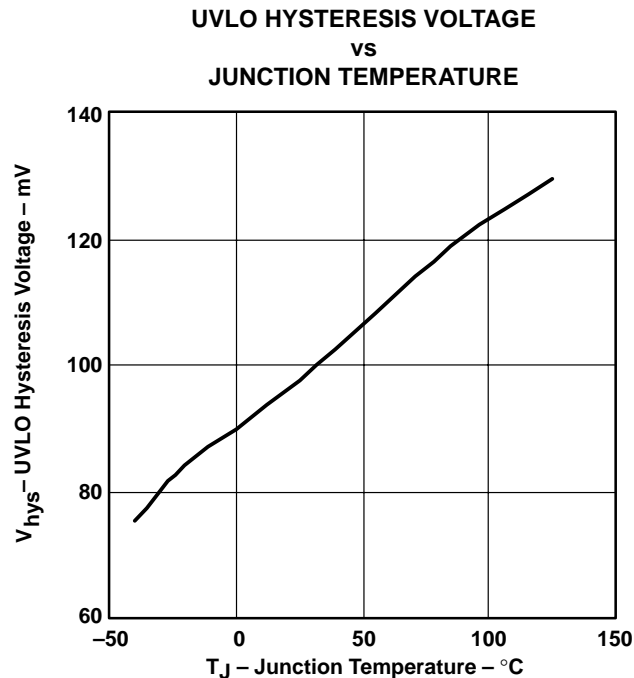


Figure 19

TYPICAL CHARACTERISTICS

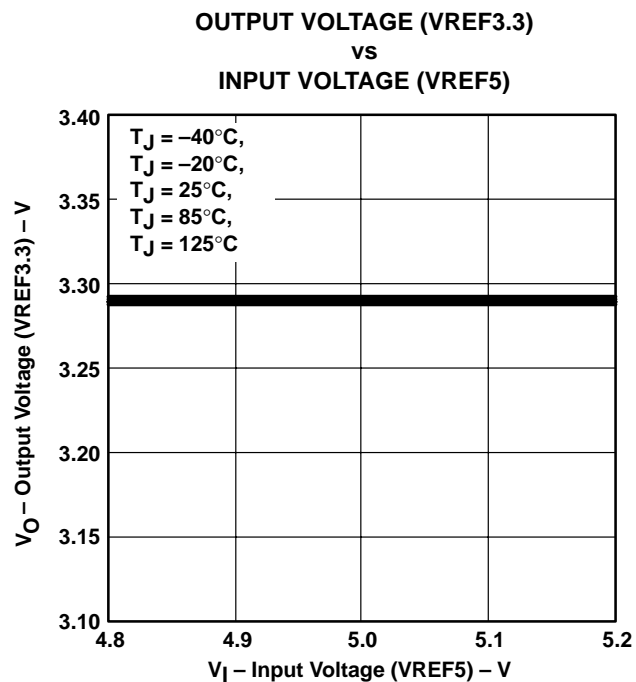


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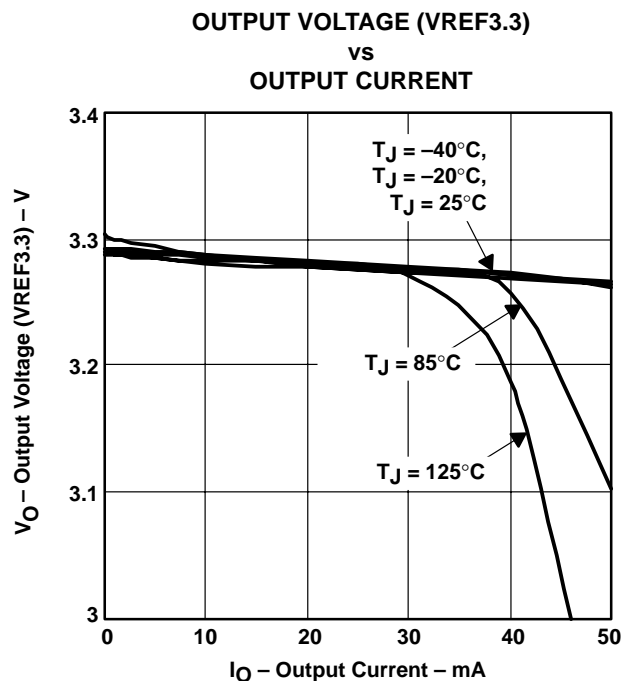


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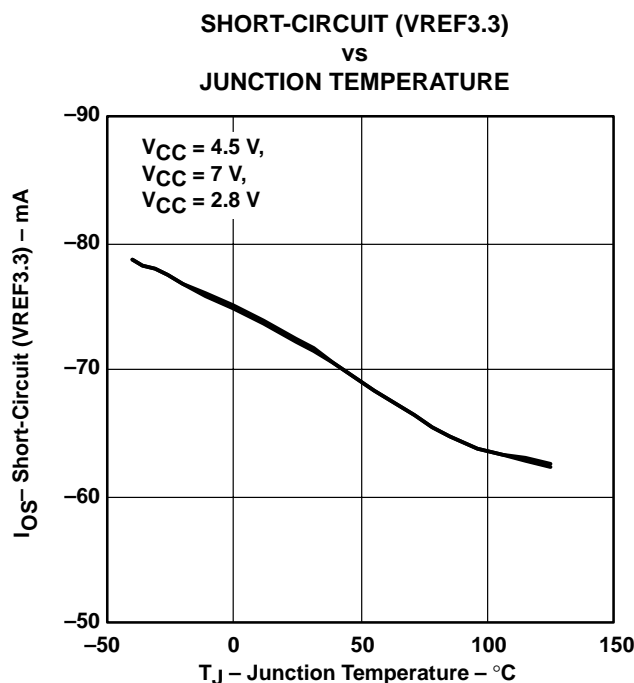


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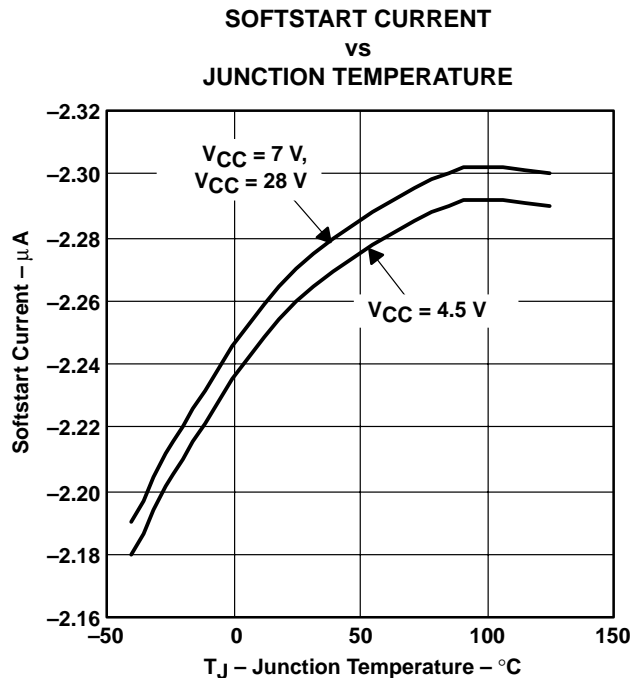


Figure 23

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TYPICAL CHARACTERISTICS

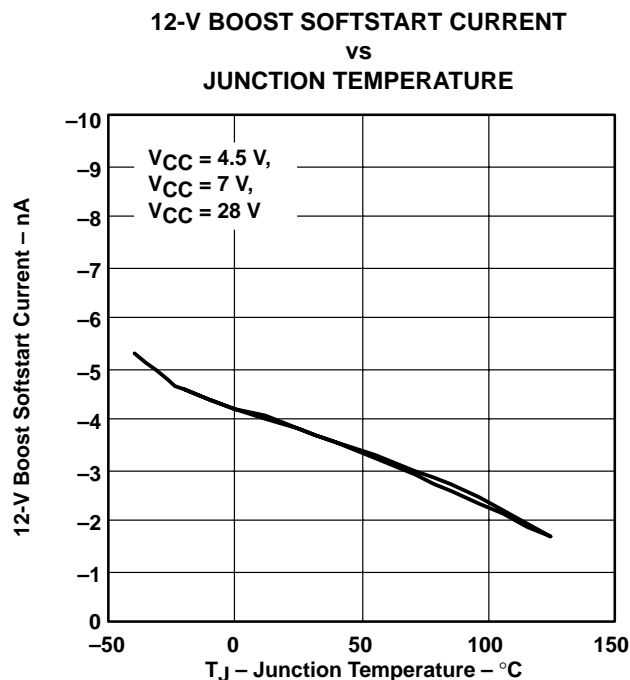


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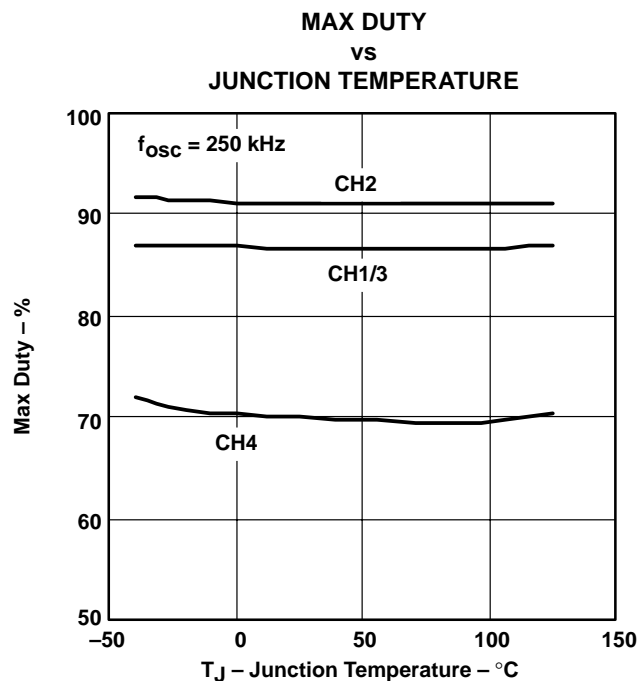


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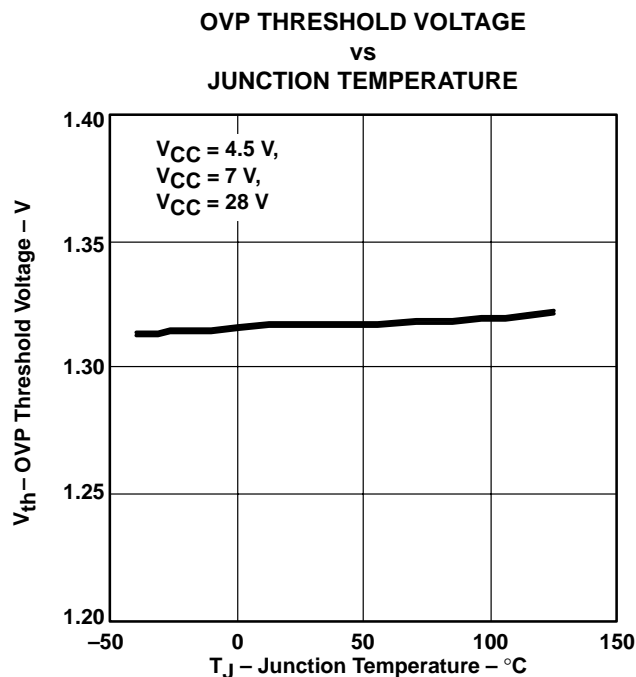


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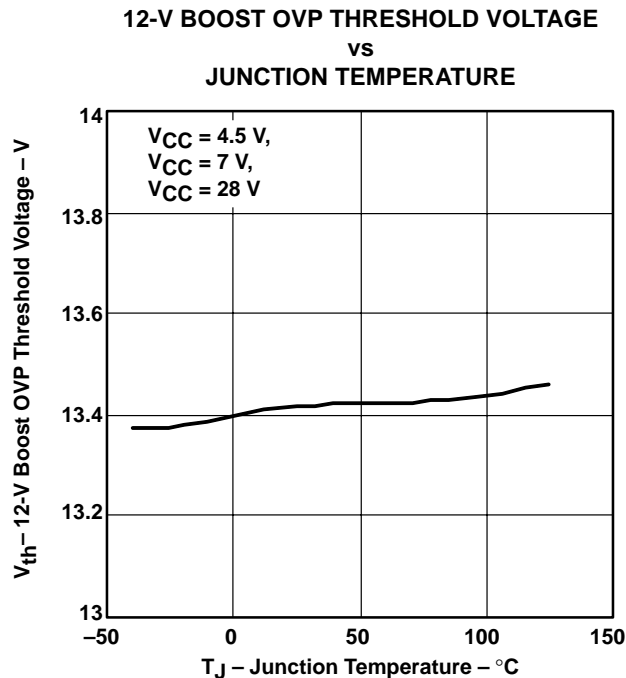


Figure 27

TYPICAL CHARACTERISTICS

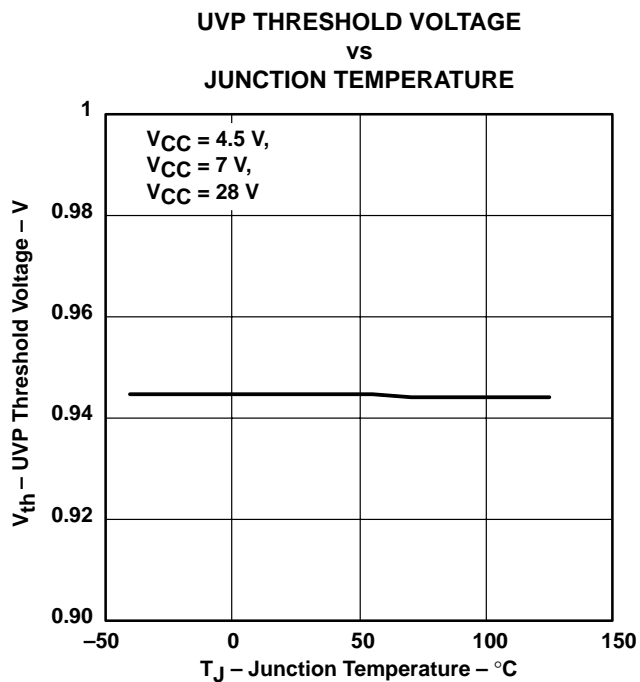


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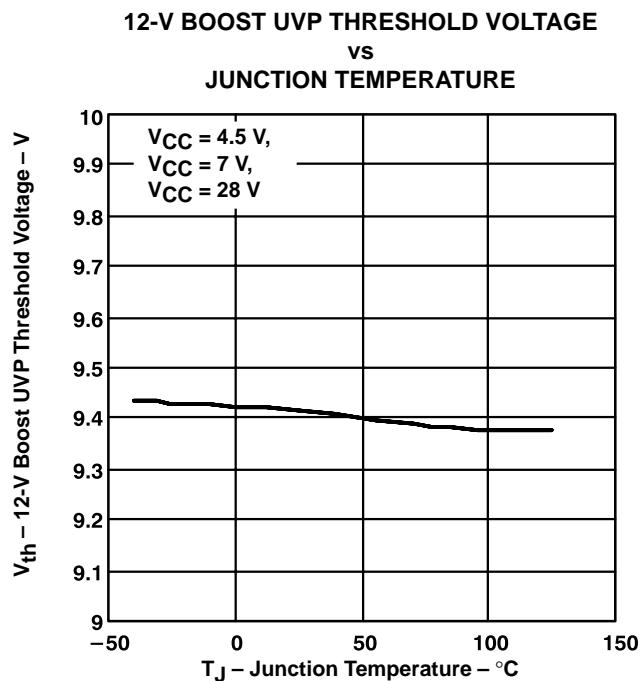


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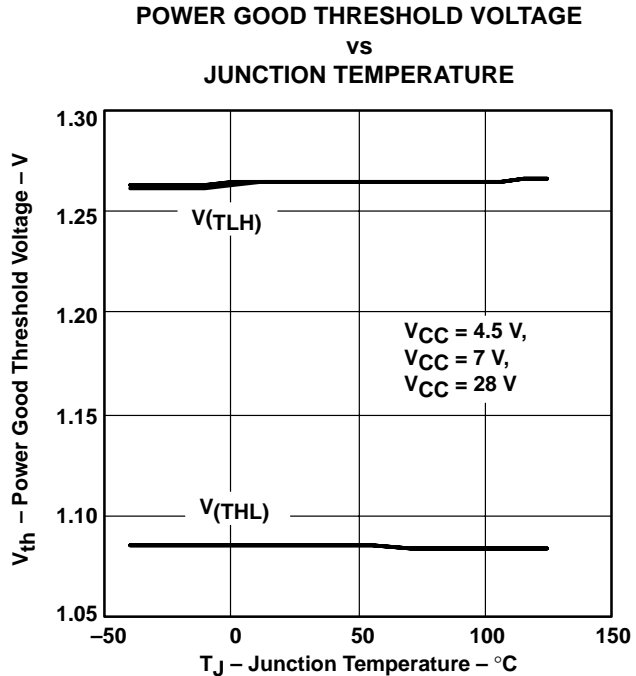


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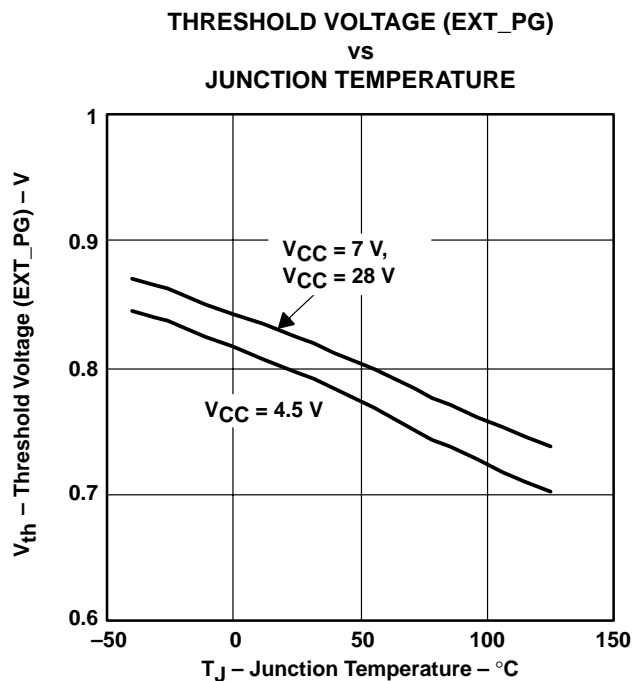


Figure 31

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TYPICAL CHARACTERISTICS

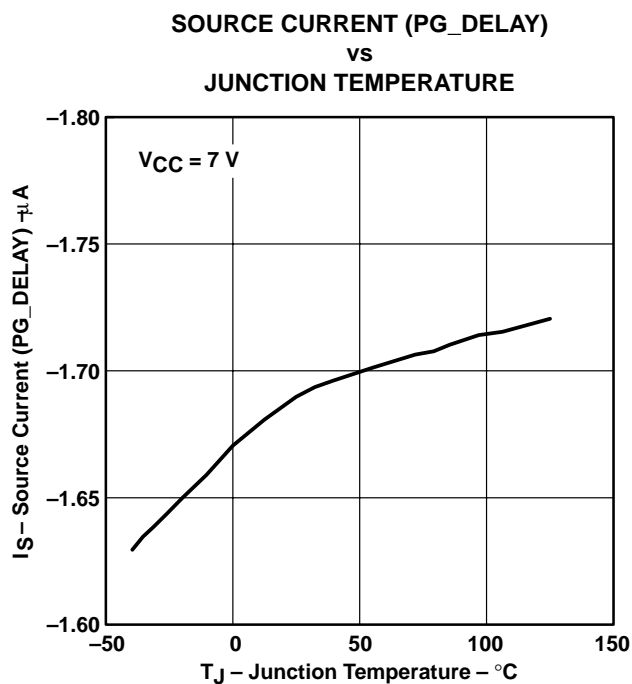


Figure 32

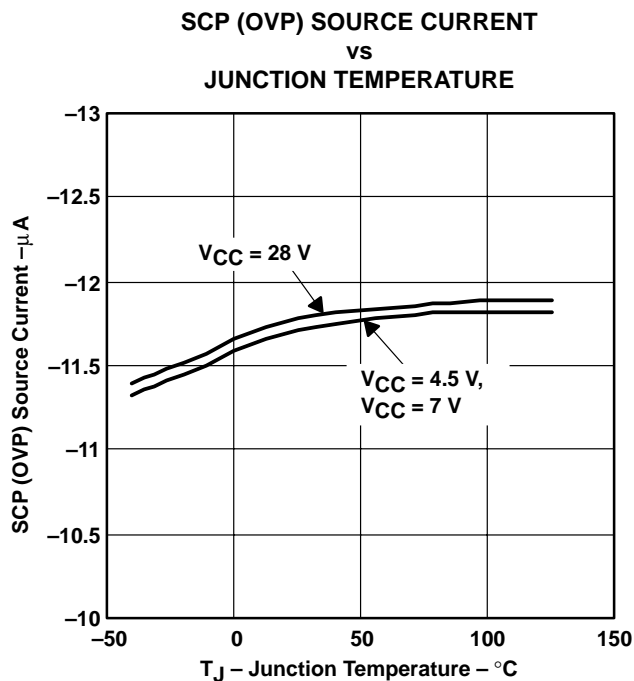


Figure 33

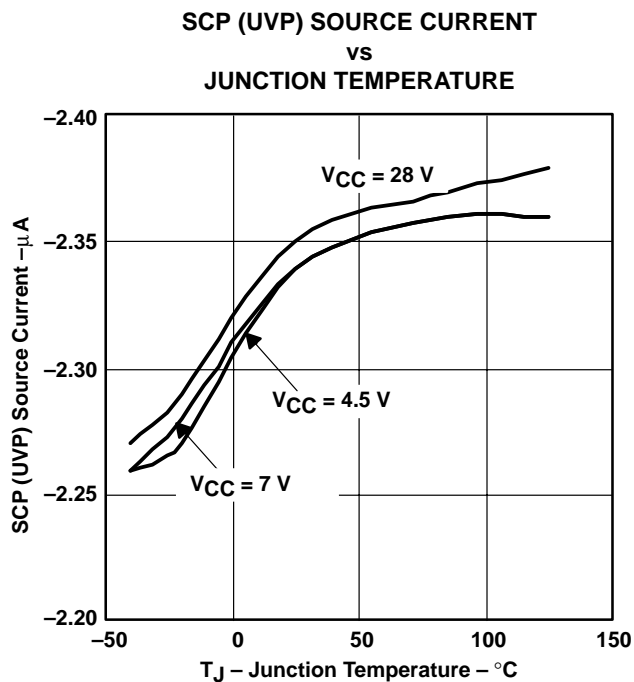


Figure 34

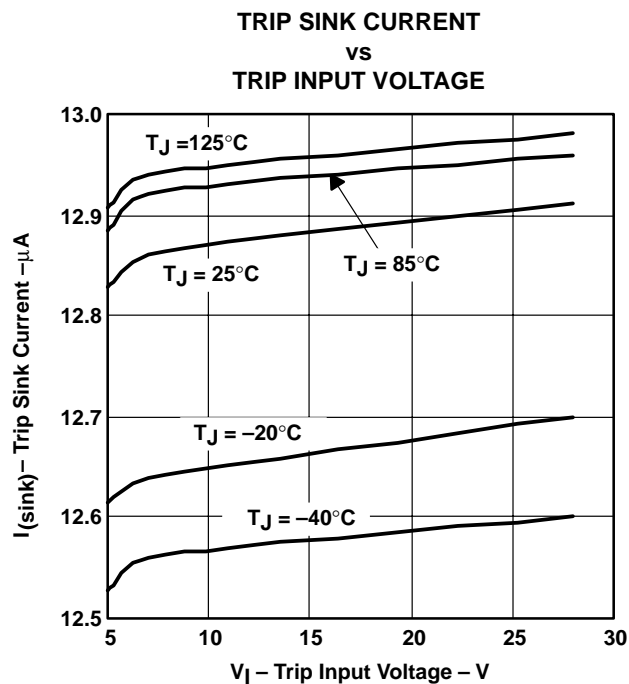


Figure 35

TYPICAL CHARACTERISTICS

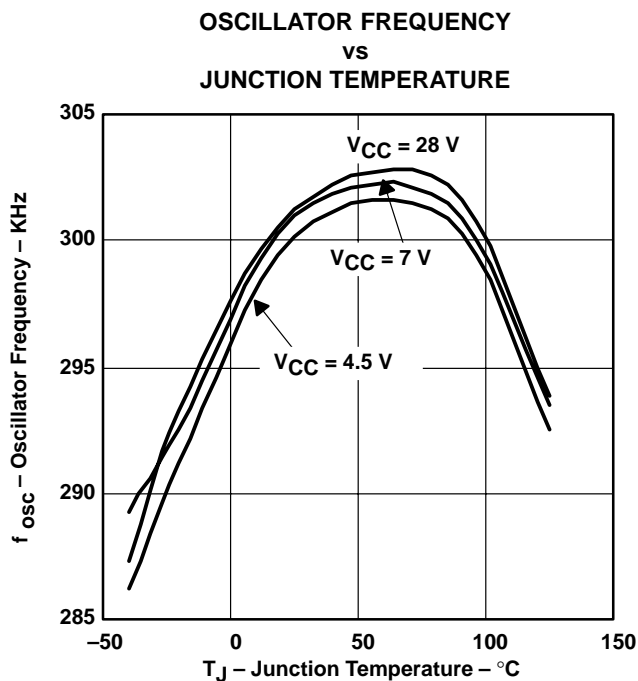


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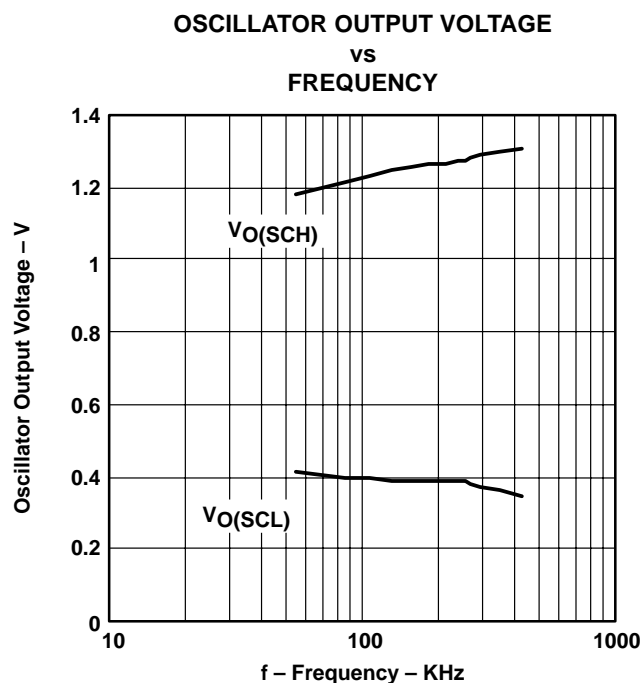


Figure 37

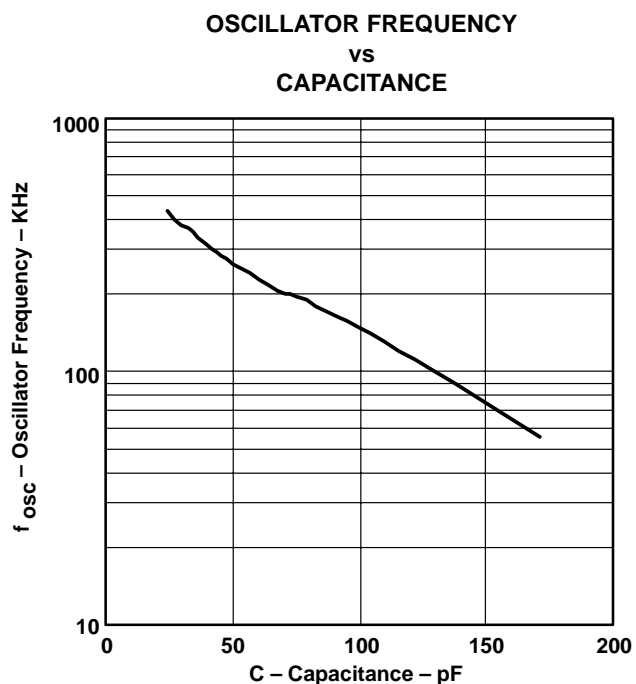


Figure 38

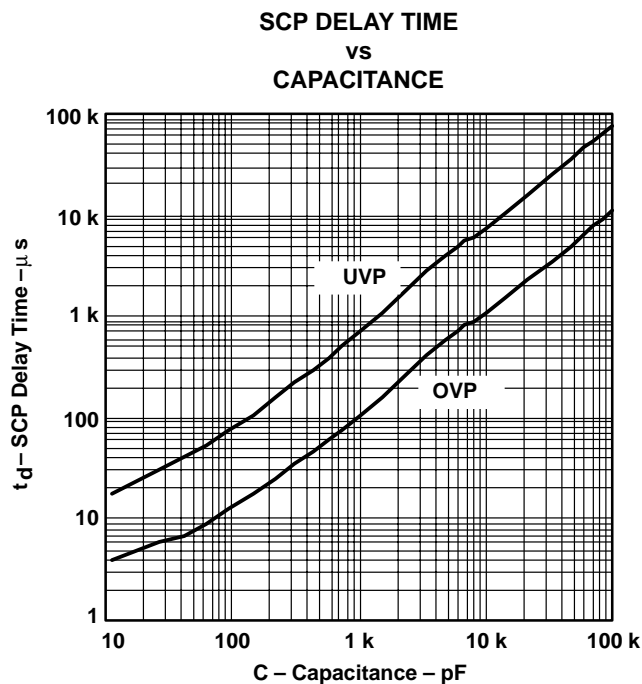


Figure 39

TPS5140 FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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TYPICAL CHARACTERISTICS

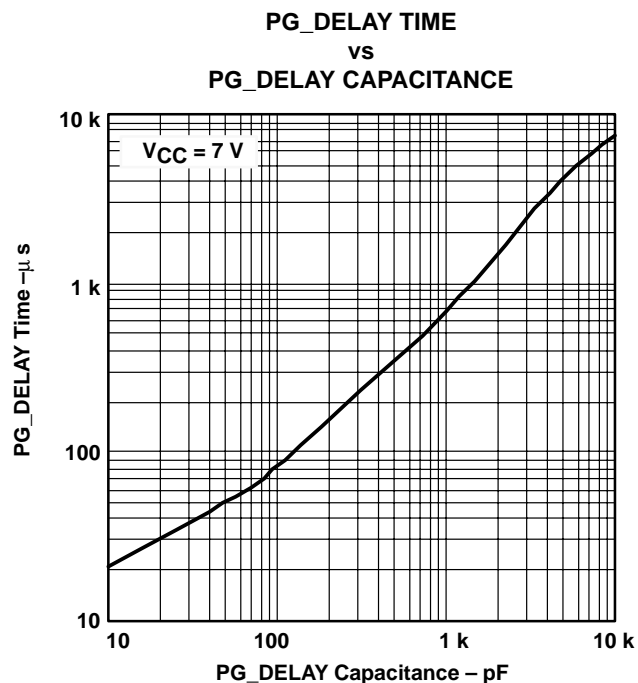


Figure 40

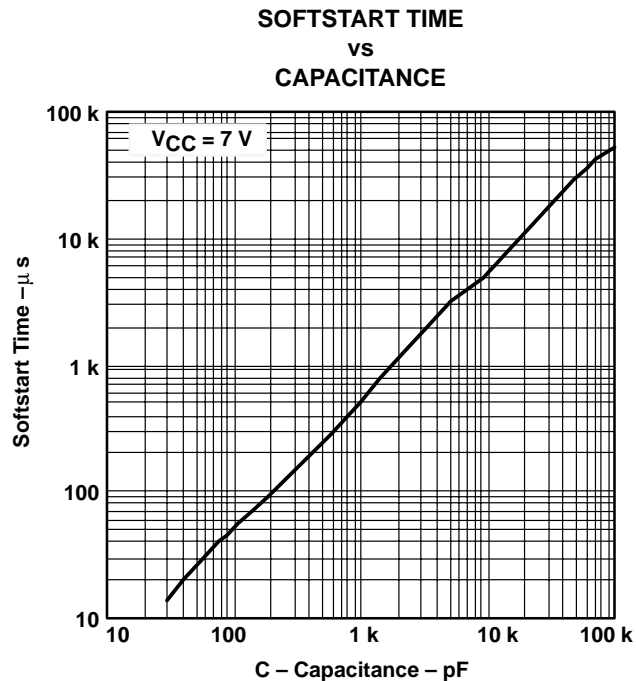


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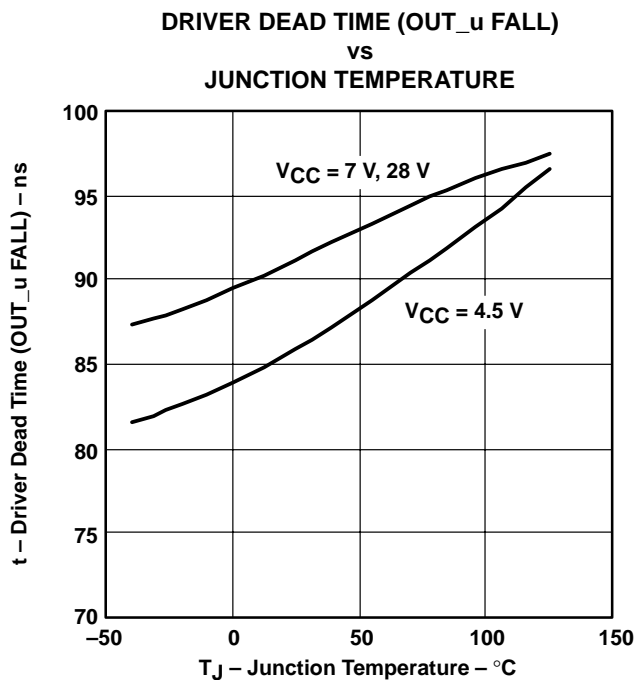


Figure 42

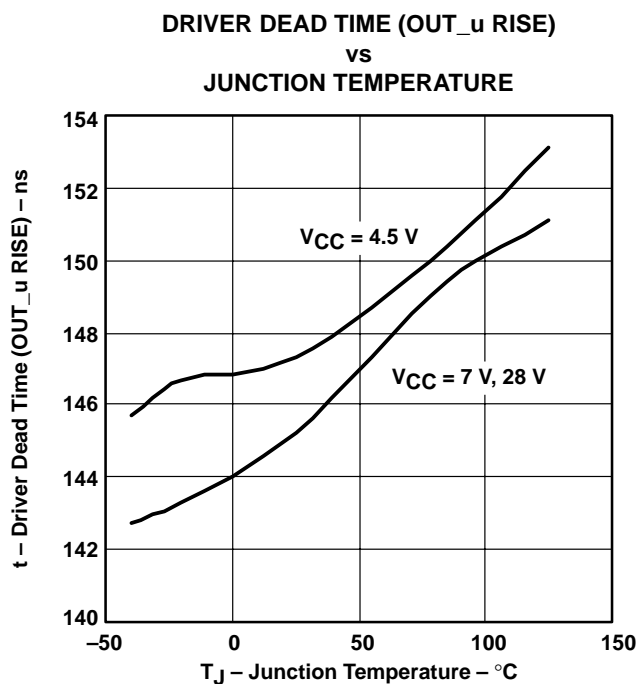


Figure 43

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APPLICATION INFORMATION

The design shown in this data sheet is a reference design for system power of notebook PC applications. An evaluation module (EVM), TPS5140EVM-172 (SLVP172), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users' PCB to shorten design cycle. The following key design procedures will aid in the design of the notebook PC power supply using the TPS5140.

EVM input and outputs

| | | V _{O1} | V _{O2} | V _{O3} | V _{O4} |
|------------------------|---|-----------------|-----------------|-----------------|-----------------|
| Output voltage | V _I range = 7 V \approx 25 V | 3.3 V | 5 V | 2.5 V | 12 V |
| Maximum output current | I _{I(max)} = 9 A | 4 A | 5 A | 2 A | 120 mA |



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APPLICATION INFORMATION

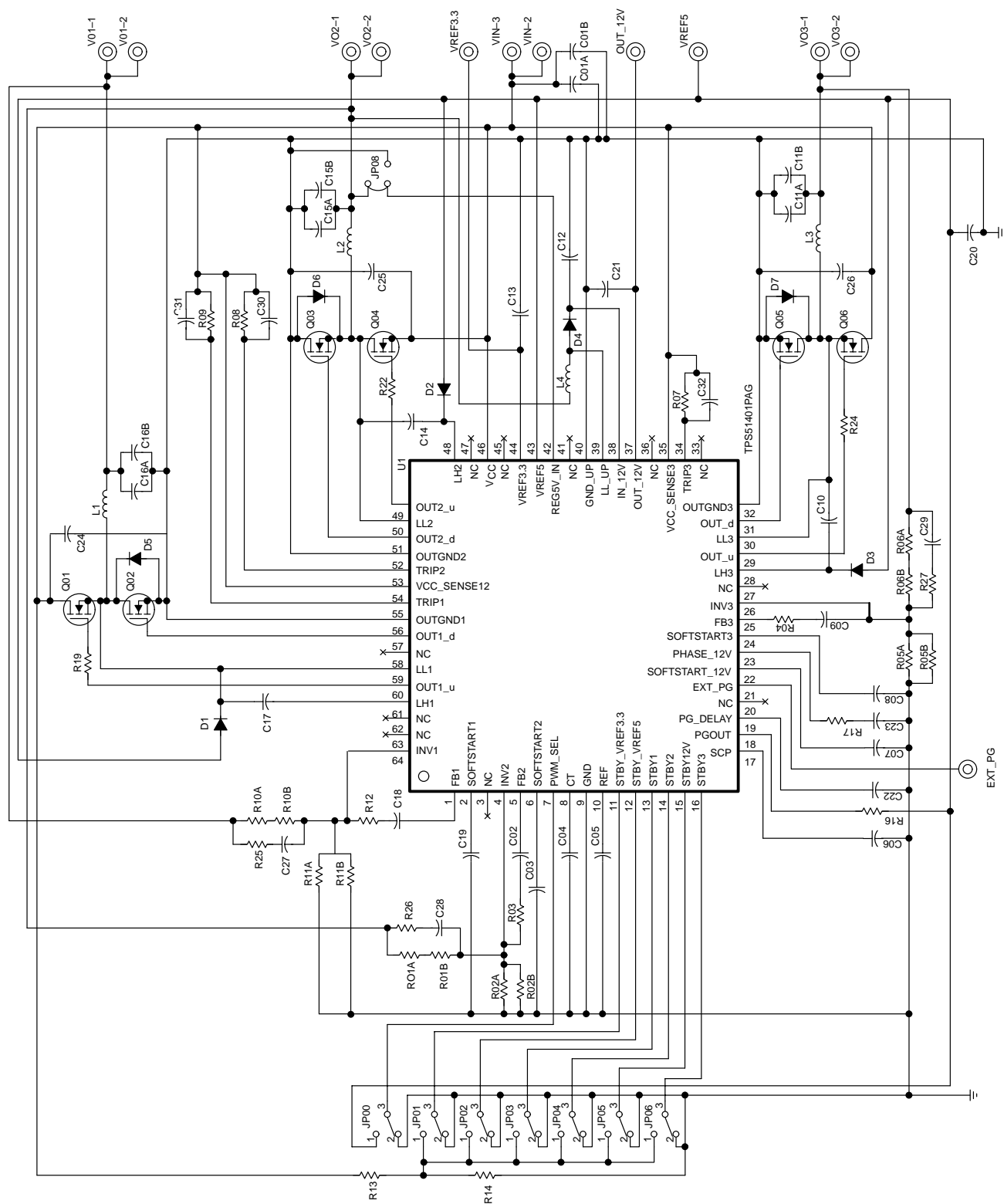


Figure 44. EVM Schematic

APPLICATION INFORMATION

SMPS (synchronous mode power supply)

output voltage setpoint calculation

The reference voltage and the voltage divider set the output voltage. In the TPS5140, the reference voltage is 1.185 V, and the divider is composed of two resistors in the EVM design that are R01A, R01B and R02A, R02B, or R10A, R10B and R11A, R11B, or R06A, R06B and R05A, R05B. The equation for the setpoint is:

$$R1 = \frac{R2 \times (V_O - V_{ref})}{V_{ref}}$$

where R1 is the top resistor (kΩ) (R01A and R01B, R10A and R10B or R06A and R06B); R2 is the bottom resistor (kΩ) (R02A and R02B, R11A and R11B or R05A and R05B); V_O is the required output voltage (V); V_{ref} is the reference voltage (1.185 V in TPS5140).

Example: $R2 = 10 \text{ k}\Omega$; $V_{ref} = 1.185 \text{ V}$; $V_O = 5 \text{ V}$, then $R1 = 32.19 \text{ k}\Omega$

Some of the most popular output voltage setpoints are calculated in the table below:

| V_O | 1.3 V | 1.5 V | 1.8 V | 2.5 V | 3.3 V | 5 V |
|------------------|-------|-------|-------|-------|-------|-------|
| R1 (top) (kΩ) | 0.97 | 2.66 | 5.19 | 11.10 | 17.85 | 32.19 |
| R2 (bottom) (kΩ) | 10 | 10 | 10 | 10 | 10 | 10 |

If user changes the resistor value, the R2 (bottom) value should be over 10 kΩ due to the phase compensation.

output inductor ripple current

The output inductor current $I_{(ripple)}$ can affect not only the efficiency, but also the output voltage ripple. The equation is exhibited below:

$$I_{(ripple)} = \frac{V_I - V_O - I_O \times (r_{DS(on)} + R_L)}{L_{(out)}} \times D \times t_s$$

where ripple is the peak-to-peak ripple current (A) through the inductor; V_I is the input voltage (V); V_O is the output voltage (V); I_O is the output current; $r_{DS(on)}$ is the on-time resistance of the MOSFET (Ω); R_L is the parasitic resistance of the inductor; D is the duty cycle; and t_s is the switching period (s). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: If $V_I = 10 \text{ V}$; $V_O = 5 \text{ V}$; $I_O = 5 \text{ A}$; $r_{DS(on)} = 26 \text{ m}\Omega$; $R_L = 5 \text{ m}\Omega$; $D = 0.50$; $t_s = 4 \text{ }\mu\text{s}$; $L_{(out)} = 6.1 \text{ }\mu\text{H}$, then the ripple current $I_{(ripple)} = 1.589 \text{ A}$.

output capacitor RMS current

Assuming the inductor ripple current goes completely through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$I_{O(rms)} = I_{(ripple)} \times \frac{\sqrt{3}}{6}$$

where $I_{O(rms)}$ is the maximum RMS current in the output capacitor (A) and $I_{(ripple)}$ is the peak-to-peak inductor ripple current (A).

Example: $I_{(ripple)} = 1.589 \text{ A}$, so $I_{O(rms)} = 0.459 \text{ A}$

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APPLICATION INFORMATION

SMPS (synchronous mode power supply) (continued)

input capacitor RMS current

Assuming the input current goes completely into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

$$I_{I(rms)} = \sqrt{I_O^2 \times D \times (1-D)}$$

where $I_{I(rms)}$ is the input RMS current in the input capacitor (A), I_O is the output current (A), and D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example: $I_O = 5$ A; $D = 0.50$

Then, $I_{I(rms)} = 2.5$ A.

soft start

The soft start timing can be adjusted by selecting the soft start capacitor value. The equation is exhibited below:

$$C(\text{soft}) = \frac{2.3 \times T(\text{soft})}{1.185}$$

where $C(\text{soft})$ is the soft start capacitor (μF) (C19, C03 or C08 in EVM design), and $T(\text{soft})$ is the start up time (s).

Example: $T(\text{soft}) = 5$ ms, so $C(\text{soft}) = 0.01$ μF .

current limit protection

The current limit in the TPS5140 on each channel is set using an internal current source and an external resistor (R09, R08 or R07). The sensed low-side MOSFET drain-to-source voltage is compared to the set point. If the voltage exceeds the limit, the internal oscillator is activated, and it continuously resets the current limit until the over-current condition is removed or SCP latches outputs off (see timer-latch SCP). The equation below should be used for calculating the external resistor value for the current protection set point. Also, only CH2 monitors both high-side and low-side MOSFET drain-to-source voltage.

$$R(\text{cl}) = \frac{r_{DS(\text{on})} \times \left(I_{(\text{trip})} + \frac{I_{(\text{ripple})}}{2} \right)}{0.000013}$$

where $R(\text{cl})$ is the external current limit resistor (R09, R08 or R07), and $r_{DS(\text{on})}$ is the low side MOSFET (Q02, Q03 or Q05) on-time resistance. $I_{(\text{trip})}$ is the required current limit and $I_{(\text{ripple})}$ is the peak-to-peak output inductor current.

Example: $r_{DS(\text{on})} = 26$ m Ω , $I_{(\text{trip})} = 7$ A, $I_{(\text{ripple})} = 1.589$ A, so $R(\text{cl}) = 16$ k Ω .

APPLICATION INFORMATION

SMPS (synchronous mode power supply) (continued)

timer-latch SCP

The TPS5140 includes the function of the fault latch with timer to latch the MOSFET driver after constant time passes since the unusual condition of the output was detected. When the OVP or UVP comparator detects a fault condition, the timer starts to charge the SCP capacitor (C06), which is connected to the SCP terminal. If the SCP terminal goes up to 1.185 V, the fault latch is set.

- **over current protection and under voltage protection**

When the current limit circuit limits the output current, then the output voltage will go below the target output voltage and the UVP comparator detects a fault condition. The timer starts to charge the SCP capacitor when the UVP comparator detects the output under voltage and the fault latch will be set after $T_{(uvplatch)}$ has past. When UVP is latched, all output MOSFET drivers of the TPS5140 turn *OFF*. The equation below should be used for calculating the $T_{(uvplatch)}$:

$$C_{(scp)} = \frac{2.3 \times T_{(uvplatch)}}{1.185}$$

- **over voltage protection**

When OVP comparator detects the output over voltage, the timer starts to charge the SCP capacitor, and the fault latch will be set after $T_{(ovplatch)}$ has past. In case of OVP-latch, the high-side drivers of both channels are forced *OFF* and the low-side drivers of both channels are forced *ON*. The equation below should be used for calculating the $T_{(ovplatch)}$:

$$C_{(scp)} = \frac{11.5 \times T_{(ovplatch)}}{1.185}$$

where $C_{(scp)}$ is the external capacitor, $T_{(uvplatch)}$ is time from the UVP detection to latch, and $T_{(ovplatch)}$ is the time from OVP detection to latch.

Example: $T_{(uvplatch)} = 515 \mu s$, $T_{(ovplatch)} = 103 \mu s$, so $C_{(scp)} = 0.001 \mu F$

notice—usage of timer-latch

The SCP should not be set to a lower voltage (or GND) while the device is holding the latch-off status of the OVP or UVP. If the SCP terminal is manually set to a lower voltage in this term, an output overshoot may occur. The TPS5140 must be reset by grounding the STBY1,2,3 and STBY_VREF5,3.3 or by dropping the V_{CC} below the UVLO voltage.

disablement the protection function

When debugging the circuit once preliminary calculations have been performed, the evaluation may be hampered because the protection circuitry does not operate properly. In this case, the TPS5140 is able to invalidated the protection circuits for debugging.

OCP: Removing the resistor for the current limit and opening the TRIP terminal can disable the OCP.
OVP, UVP: Grounding the SCP terminal can disable the OVP and UVP.

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APPLICATION INFORMATION

3.3 V linear regulator

The VREF3.3 terminal is the output of the 3.3-V linear regulator. The VREF3.3 terminal should be connected to an output capacitor. A ceramic capacitor of 4.7 μ F is recommended for stability of the output voltage.

REG5V_IN

The REG5V_IN terminal should be connected to the external 5 V (output of CH2), to decrease the power dissipation. Also, this terminal has an OVP comparator. If this terminal voltage exceeds a threshold voltage, the timer starts to charge the SCP capacitor, and all of output is forced to *OFF*.

12 V boost up converter

The TPS5140 has a boost up converter (12 V). The inductor (L4) which uses this boost up converter should be connected to the external 5 V. Also, the inductor value is recommended to be 22 μ H. The OUT_12V terminal should be connected to the output capacitor. A ceramic capacitor of 10 μ F is recommended for stability of the output voltage. It is also recommended that a ceramic capacitor (around 0.1 μ F) be connected between the IN_12V terminal and the GND_UP terminal.

soft start 12 V

This soft start terminal is connected to the internal capacitor. To extend the soft start time, this terminal should be connected to the external capacitor. The equation is:

$$\left(30 + C_{(\text{ext})} \right) \times 1.185 = 3.8 \times T_{(\text{soft_12V})}$$

where $C_{(\text{ext})}$ is the 12-V soft start capacitor (pF) and $T_{(\text{soft_12V})}$ is the start-up time (ms).

Example: $C_{(\text{ext})} = 33$ pF, so $T_{(\text{soft_12V})} = 19.6$ ms

APPLICATION INFORMATION

phase compensation for 12-V boost

The 12-V boost up converter is compensated to the phase margin. If the output components are changed, the phase margin will change. Therefore, the phase margin needs to be compensated. A resistor and capacitor should be connected in series from the PHASE_12V terminal to GND. If the inductor used is 22 μ H and the output capacitor is 10 μ F (ceramic), there is no need to compensate. The equivalent circuit of the 12-V boost is shown in Figure 45.

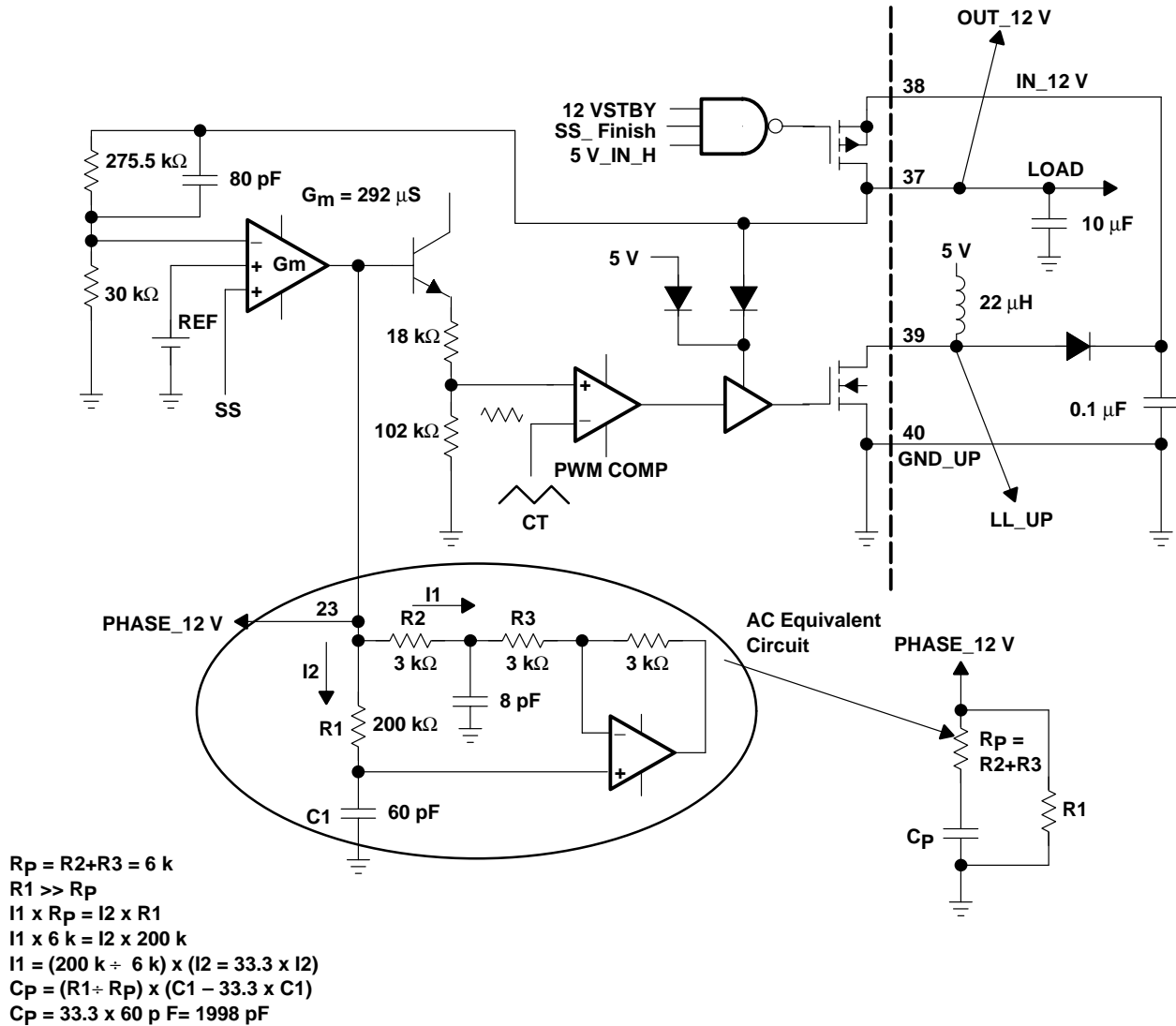


Figure 45. THS5140 12-V boost circuit

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APPLICATION INFORMATION

auto PWM/SKIP

Auto PWM/SKIP function monitors the drain-source voltage of the low-side MOSFET.

In the PWM mode to SKIP mode, when output currents decrease, the negative voltage between LL to GND is decreasing. If this voltage is positive voltage to GND, the auto SKIP circuit detects the SKIP mode. After a fixed time, the controller changes to SKIP mode.

In the SKIP mode to PWM mode, when output currents increase, the positive voltage between LL to GND is decreasing. In the SKIP mode, the auto PWM detect circuit has an offset voltage of about 20 mV. If the positive voltage between LL to GND decreases and becomes negative beyond the offset voltage of the GND level, then the auto PWM circuit detects the PWM mode, and the controller changes to the PWM mode.

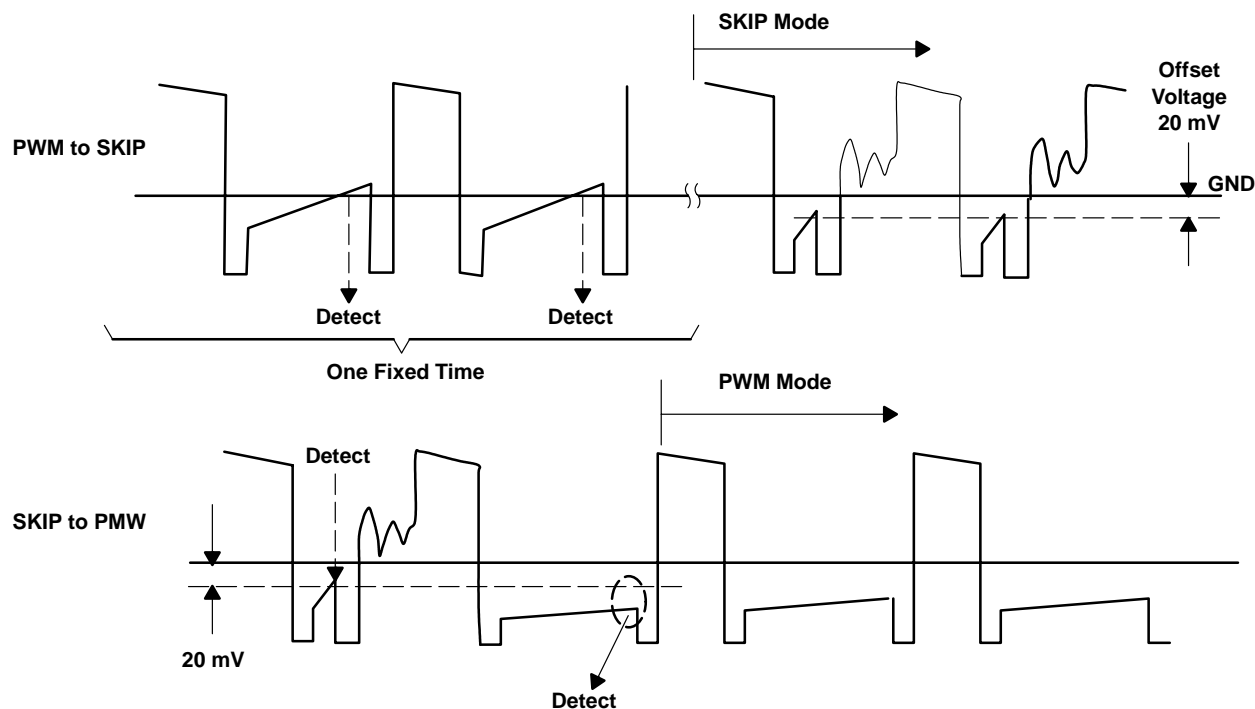


Figure 46. Timing Chart for the Auto PWM/SKIP Mode Function

APPLICATION INFORMATION

layout guidelines

Good power supply results will only occur when care is given to proper design and layout. Layout will affect noise pickup and generation yet cause a good design to perform with less than expected results. With a range of currents from milliamps to tens of amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, parallel the low-level components. Below are several specific points to consider before the layout of a TPS5140 design begins.

- ANAGND and DRVGND should be isolated as much as possible.
- All sensitive analog components should reference to ANAGND. Terminals INV1/2/3, REF, CT, GND, SCP, and SOFTSTART1/2/3/12V should be placed in ANAGND.
- Ideally, all of the area under TPS5140 is also ANAGND.
- The source of the low-side MOSFETs should not be placed in the trace from ANAGND to DRVGND otherwise ANAGND is under the influence of output noise.
- The switch transitions in one channel may disturb the operation of other channels. So, the impedance between V_{CC} and GND wiring pattern should be as small as possible.
- The PCB is a four-layer pattern. This should be composed of power plane, power ground plane, signal ground plane, and signal plane.

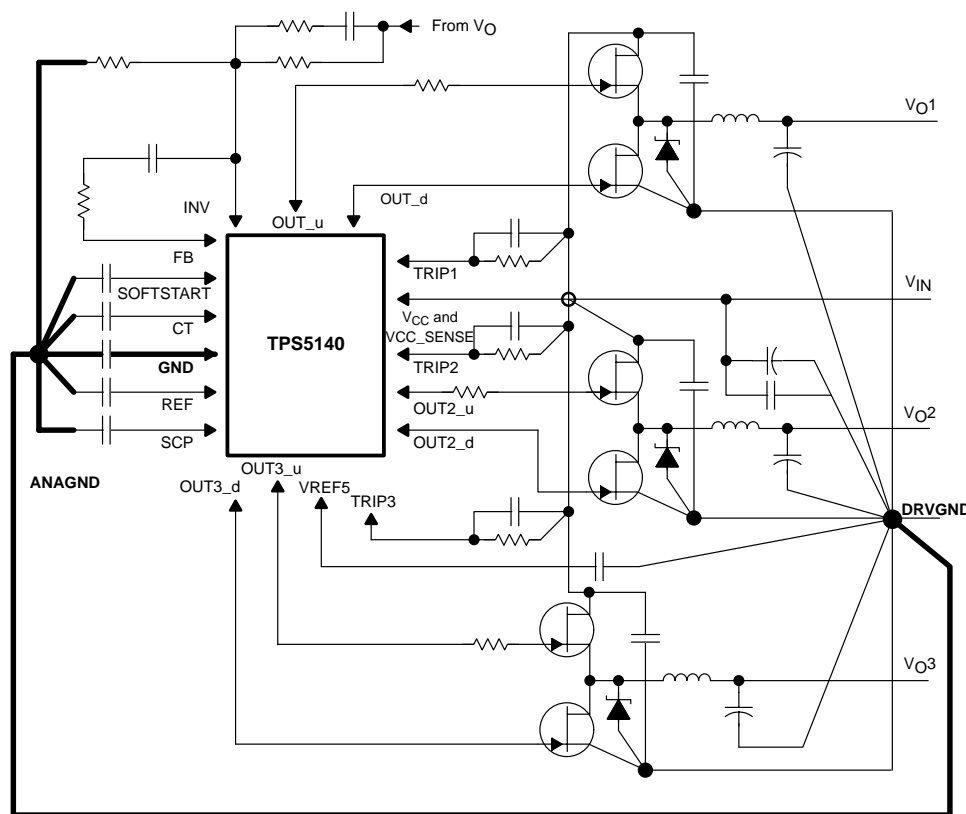


Figure 47. SLVP172 Four Layer PCB Diagram

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APPLICATION INFORMATION

layout guidelines (continued)

- DRVND will connect to the main ground plane, close to the source of the low-side MOSFET.
- OUTGND1/2/3 should be placed close to the source of low-side MOSFET.
- The parallel Schottky diode, the high frequency bypass capacitors for MOSFETs, and the source of the low-side MOSFETs should be placed as close to each other as possible.

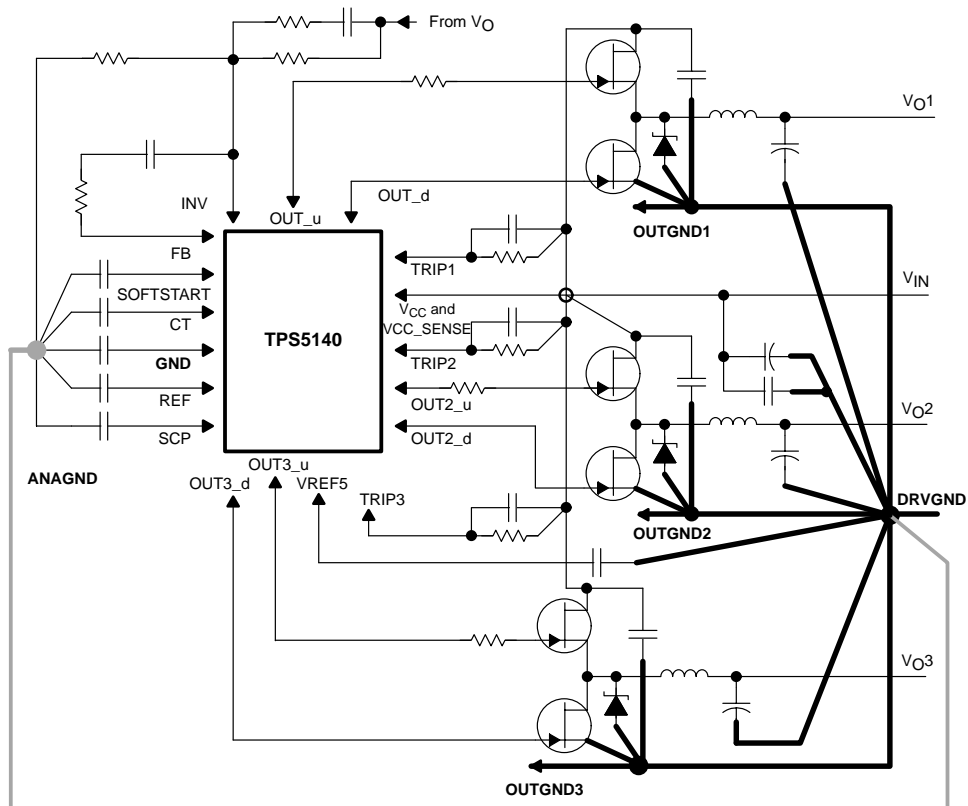


Figure 48. SLVP172 Low-Side MOSFETs Diagram

APPLICATION INFORMATION

layout guidelines (continued)

- Connections from the drivers to the gate of the power FETs should be as short and as wide as possible to reduce stray inductance. This becomes more critical if the external gate resistors are not being used. In addition, when dealing with current limit noise when using a MOSFET with a large input capacitance, a gate resistor should be inserted on the high side MOSFET to reduce the switching noise of the MOSFET.
- The connection from LL to the power FETs should be as short as and wide as possible.

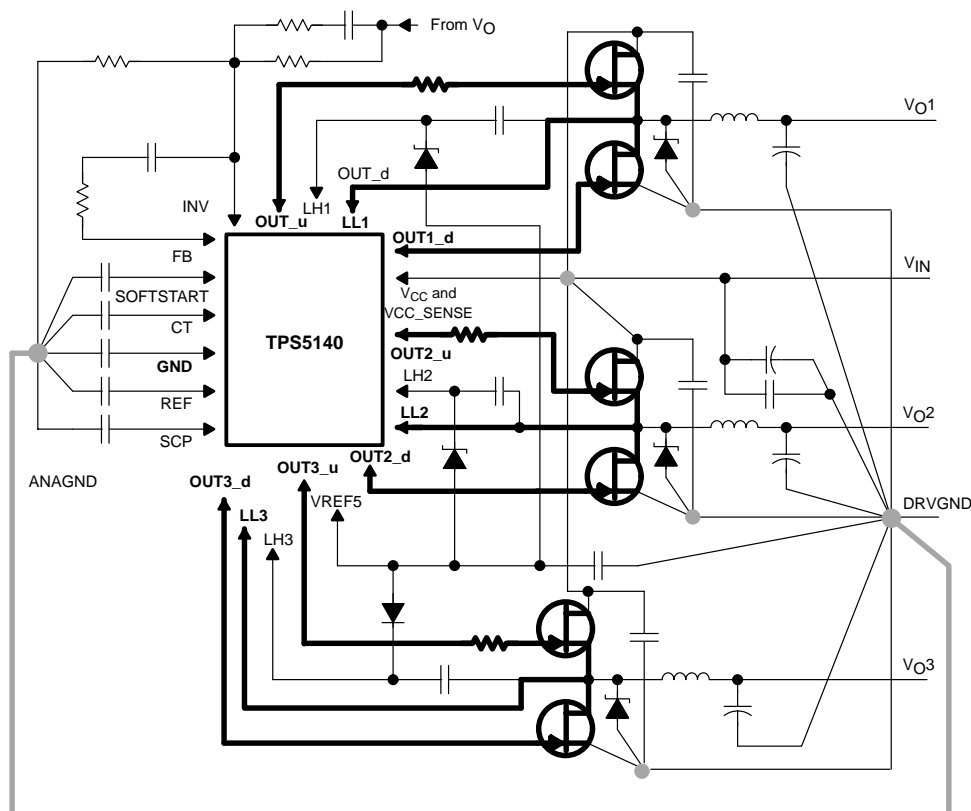


Figure 49. Connections From the Drivers to the Gate Diagram

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APPLICATION INFORMATION

layout guidelines (continued)

- The bypass capacitor for V_{CC} should be placed close to the TPS5140.
- The bulk storage capacitors across V_I should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
- Current limit set resistors must be connected to the drain of the high-side FET. A 0.1- μ F capacitor should be placed in parallel with these resistors to align the phase between the drain of high-side FETs and the trip pin.

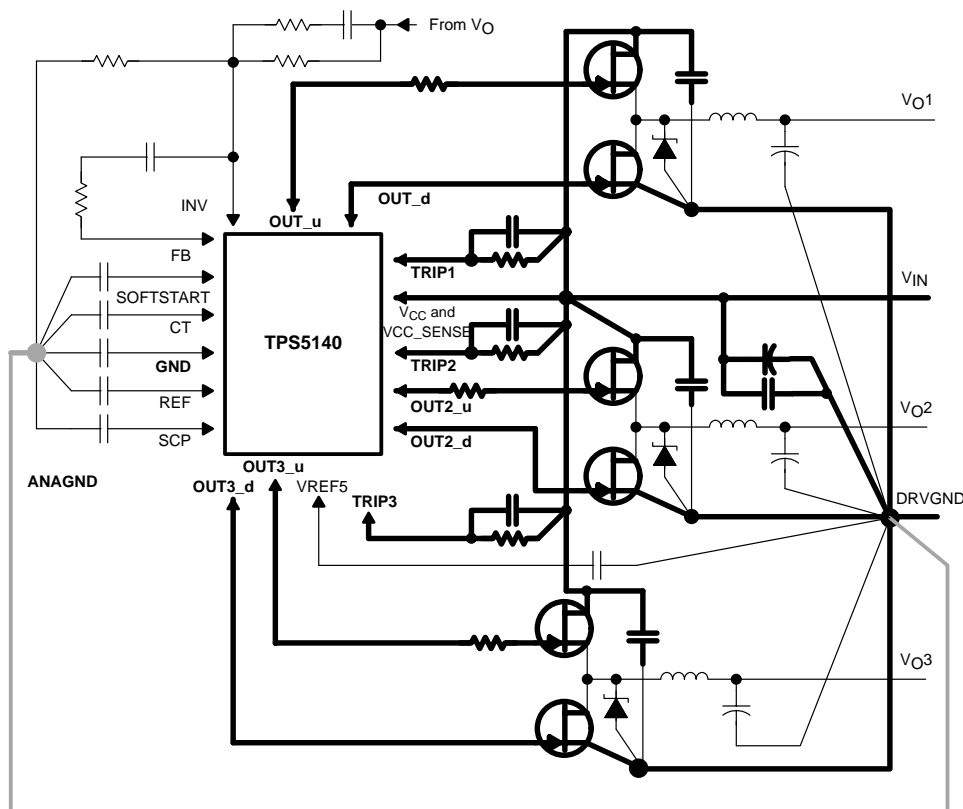


Figure 50. Bypass Capacitor Diagram

APPLICATION INFORMATION

layout guidelines (continued)

- The capacitor for VREF5 should be placed close to the TPS5140.
- The bootstrap capacitor (connected from LH to LL) should be placed close to the TPS5140.
- LH and LL should be routed close to each other to minimize differential mode noise coupling to these traces.
- The VREF5 capacitor should be placed close to DRVGNDA.
- LH and LL should not be routed near the control pin area. (ex. INV, FB, REF, etc.)

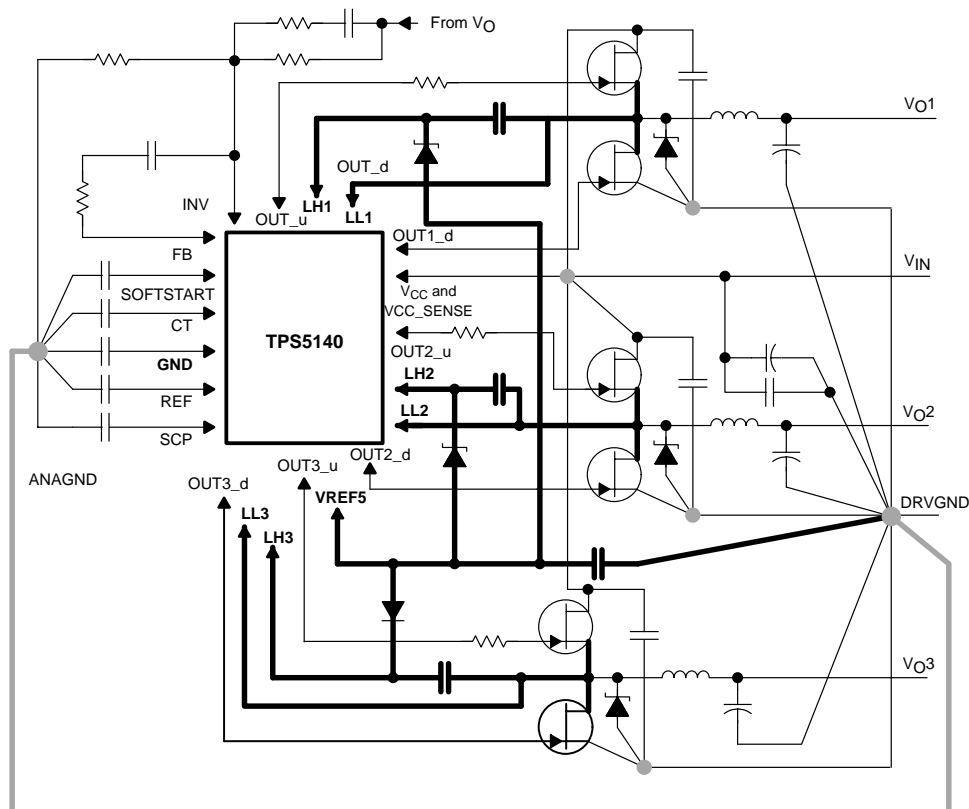


Figure 51. VREF5 Capacitor Diagram

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APPLICATION INFORMATION

layout guidelines (continued)

- The output voltage sensing trace should be isolated by either ground trace.
- The output voltage sensing trace should not be routed under the inductors on same layer of the PCB.
- The feedback components should be isolated from the output components such as MOSFETs, inductors, and output capacitors. Otherwise noise from the output components may couple into the feedback signal lines.
- The resistors for the output voltage set point should be connected to ANAGND.
- INV1/2/3 line should be as short as possible.

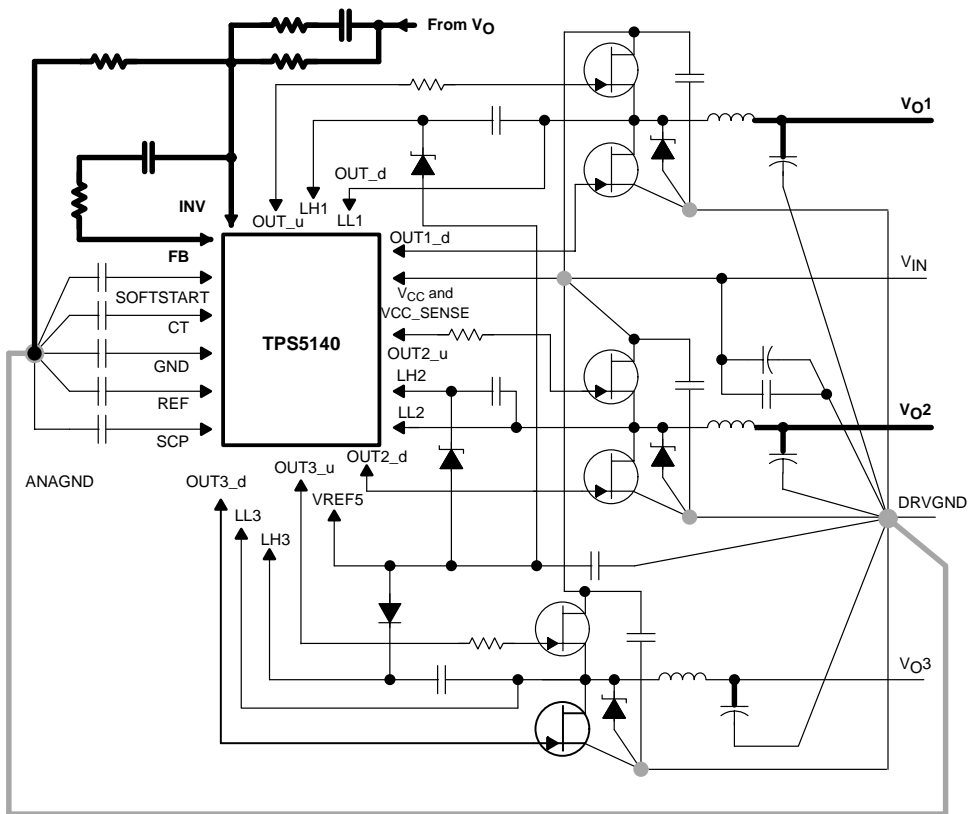


Figure 52. Output Voltage Diagram

APPLICATION INFORMATION

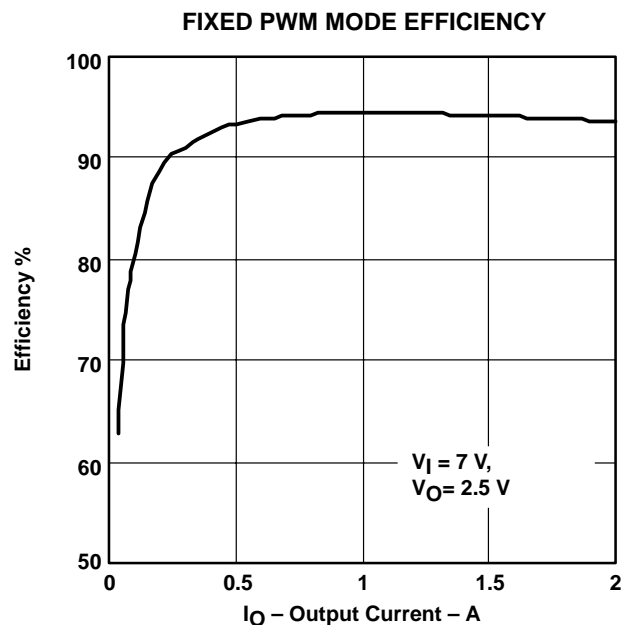


Figure 53

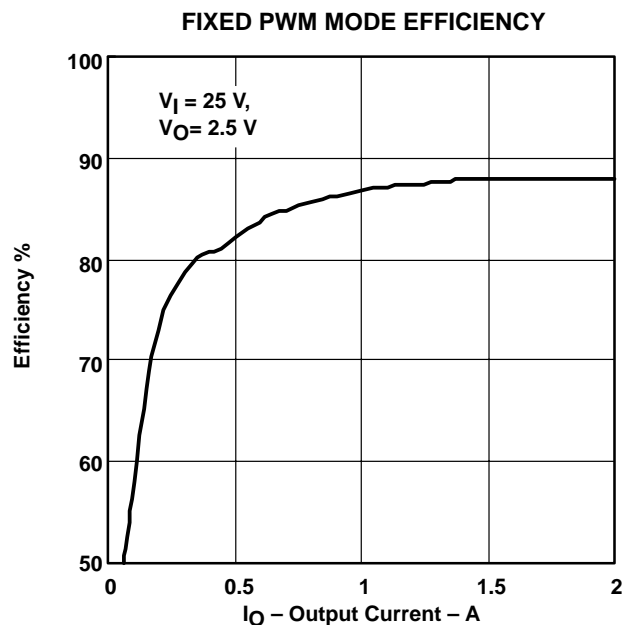


Figure 54

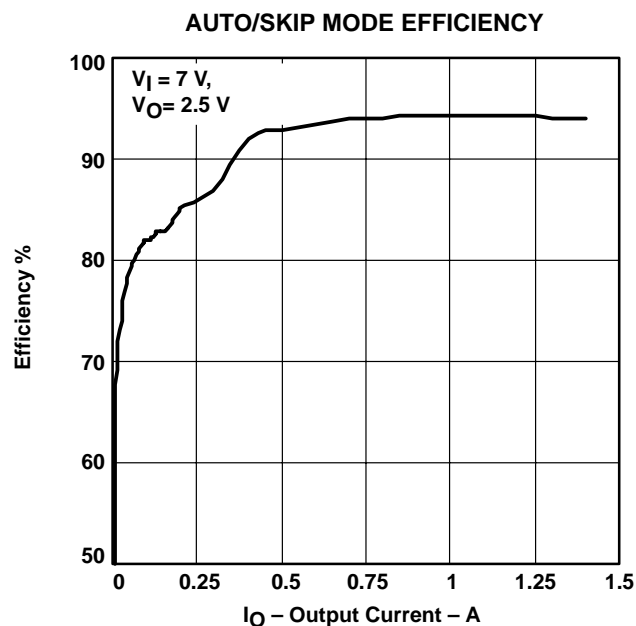


Figure 55

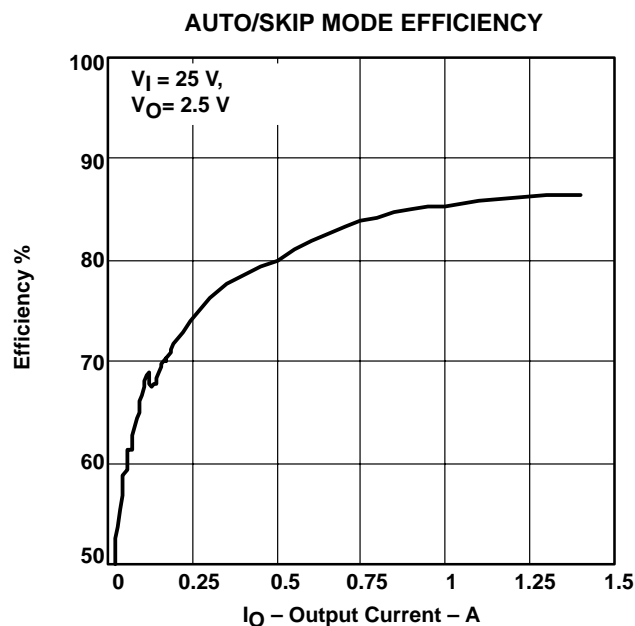


Figure 56

TPS5140 FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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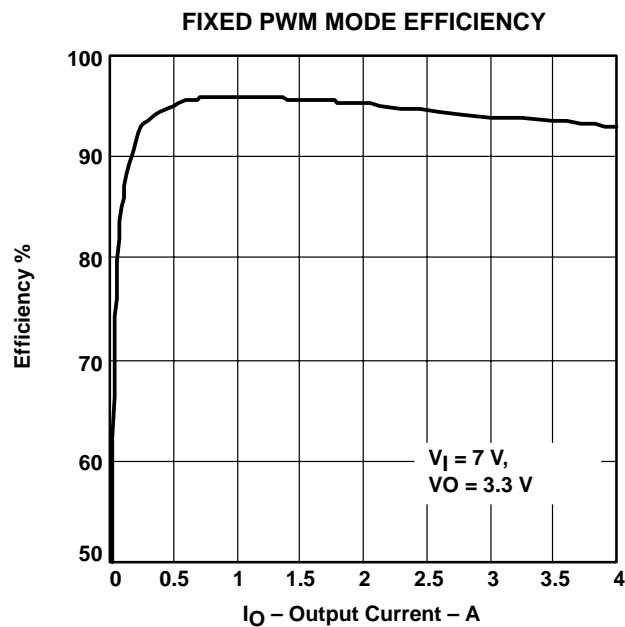


Figure 57

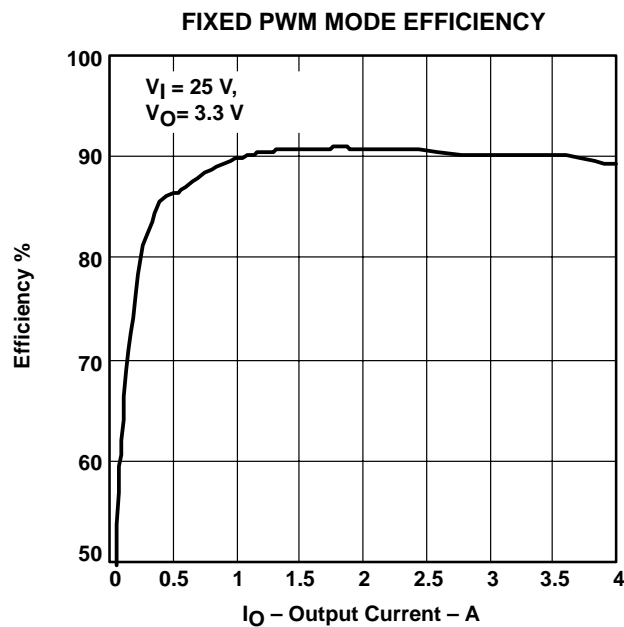


Figure 58

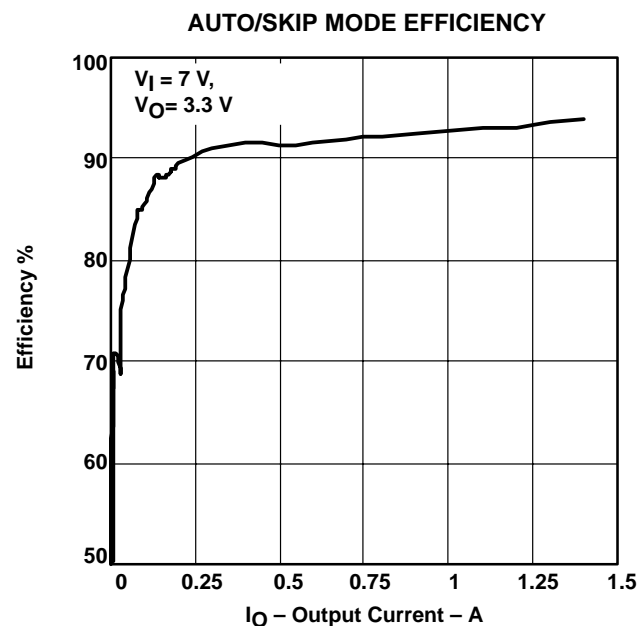


Figure 59

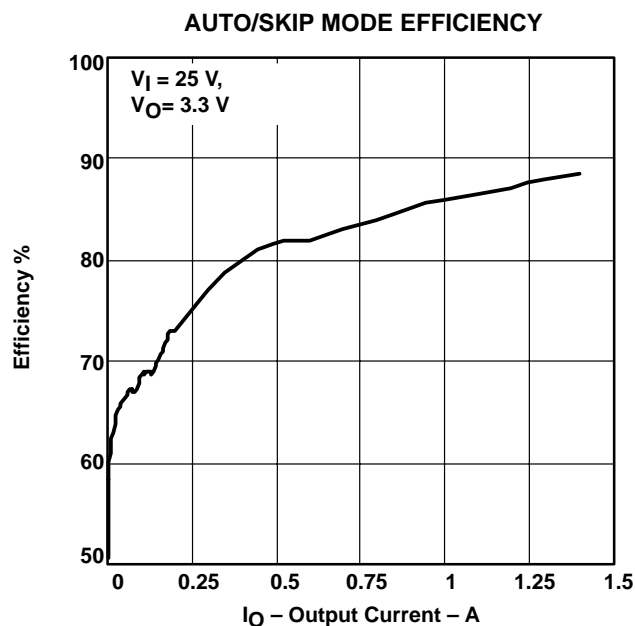


Figure 60

APPLICATION INFORMATION

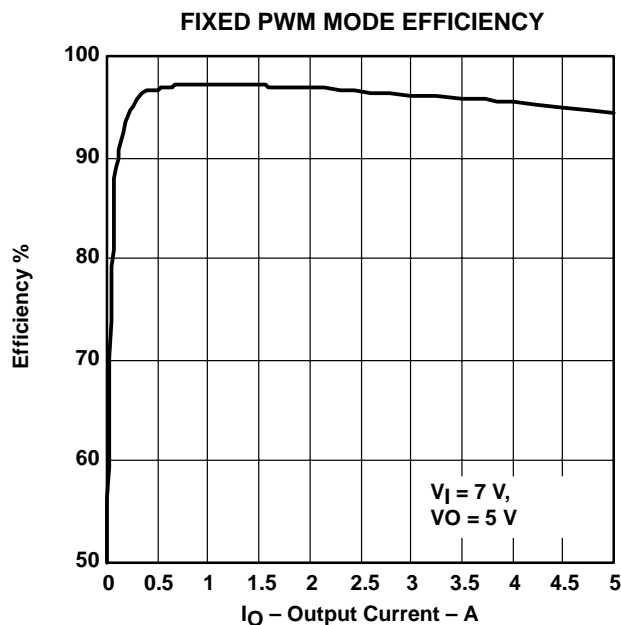


Figure 61

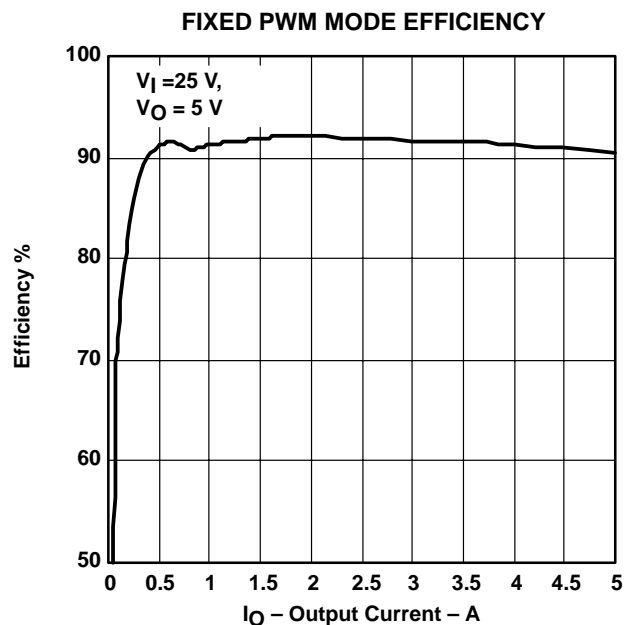


Figure 62

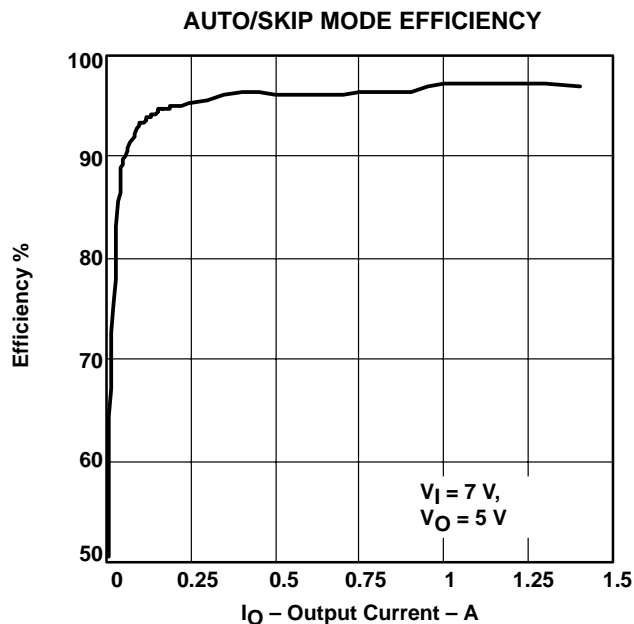


Figure 63

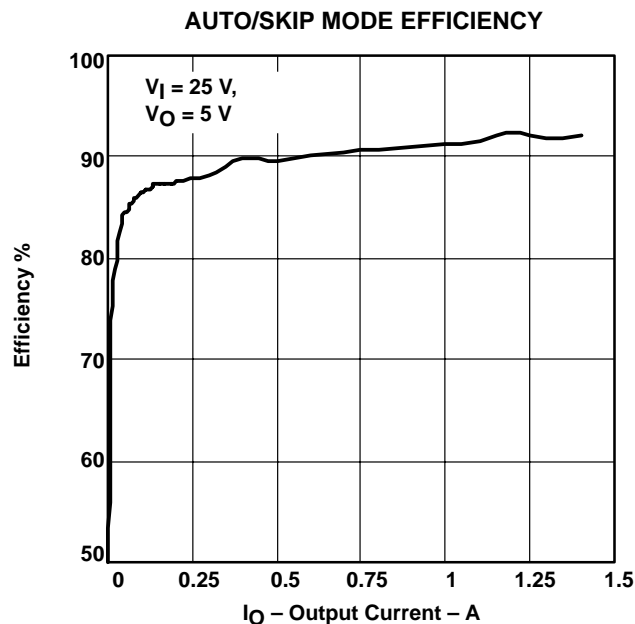


Figure 64

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APPLICATION INFORMATION

12 V BOOST EFFICIENCY

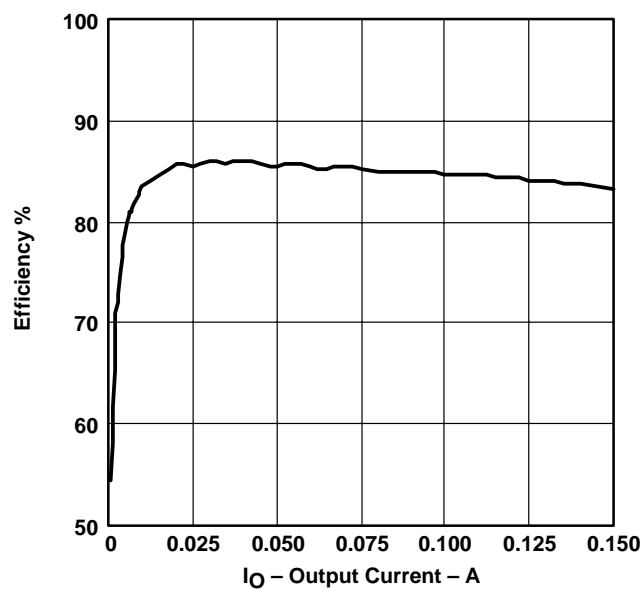


Figure 65

OUTPUT LINE REGULATION

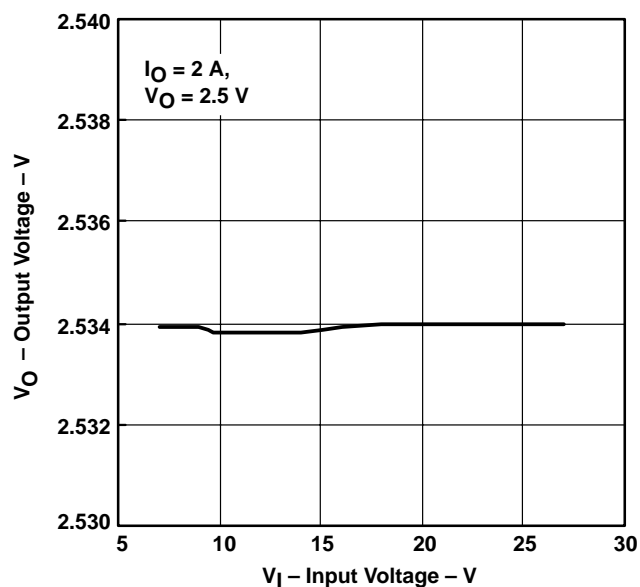


Figure 66

OUTPUT LINE REGULATION

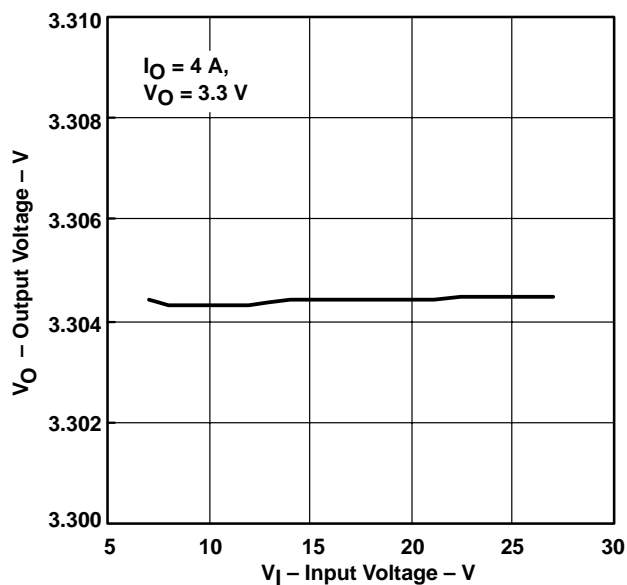


Figure 67

OUTPUT LINE REGULATION

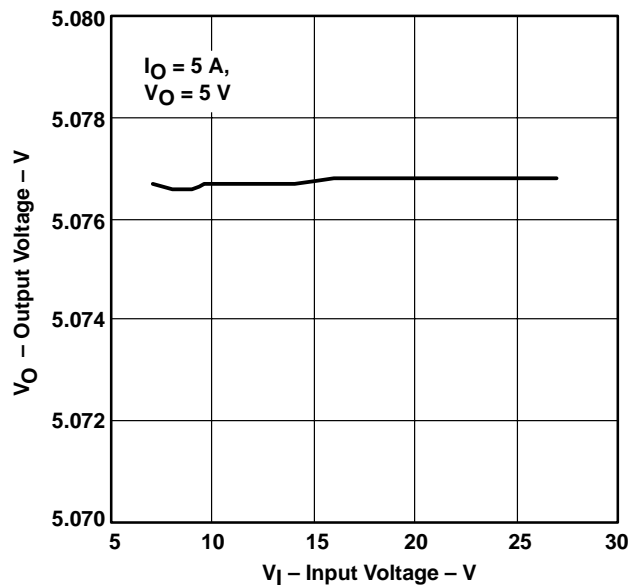


Figure 68

APPLICATION INFORMATION

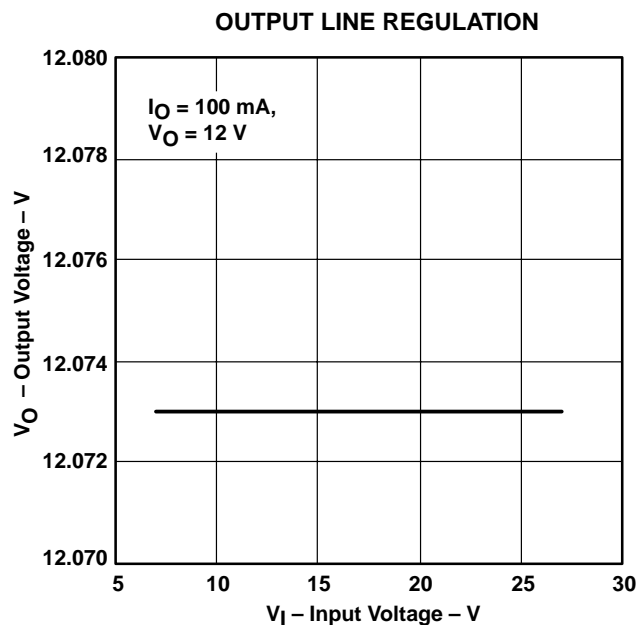


Figure 69

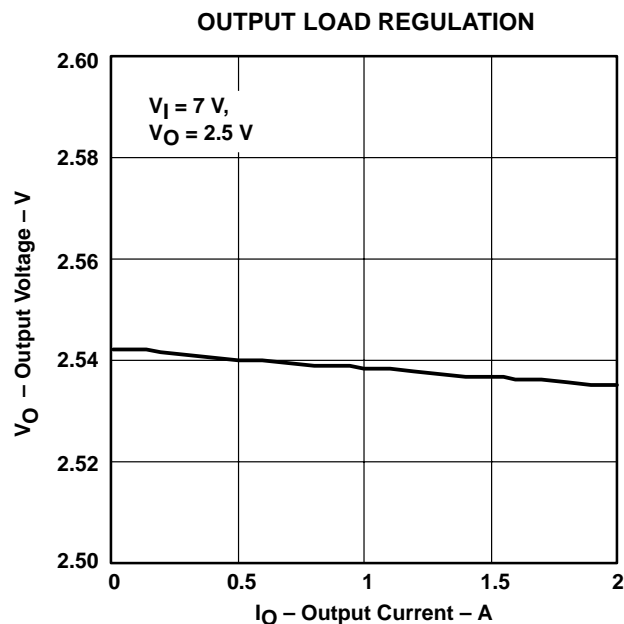


Figure 70

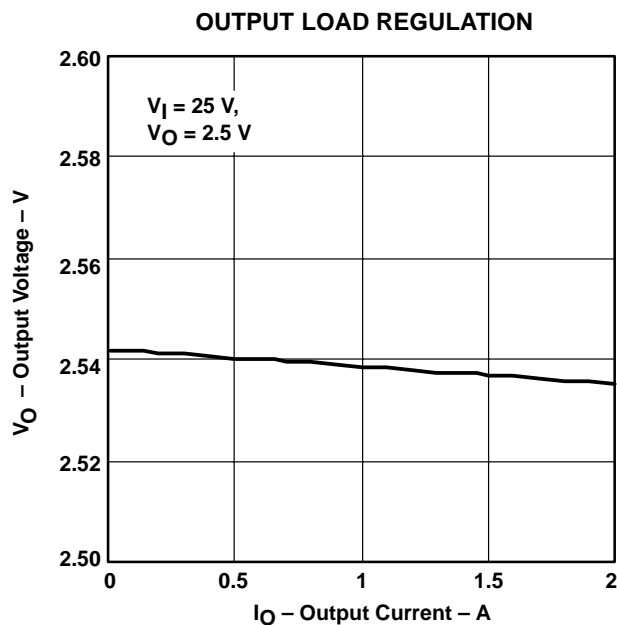


Figure 71

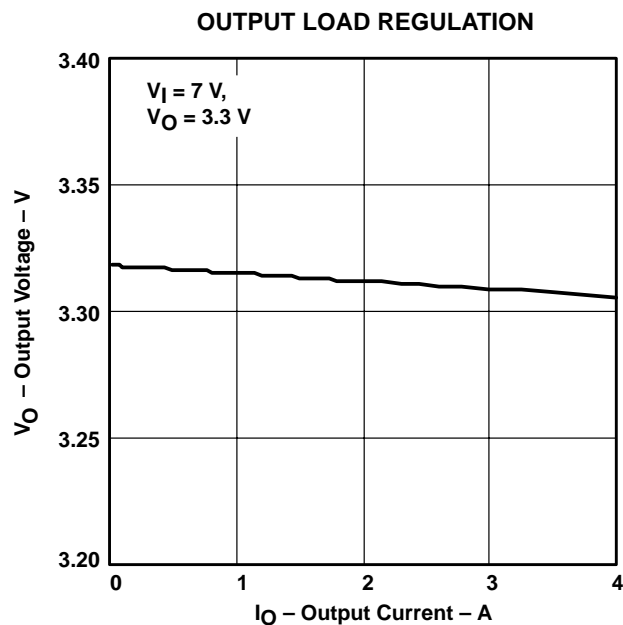


Figure 72

TPS5140

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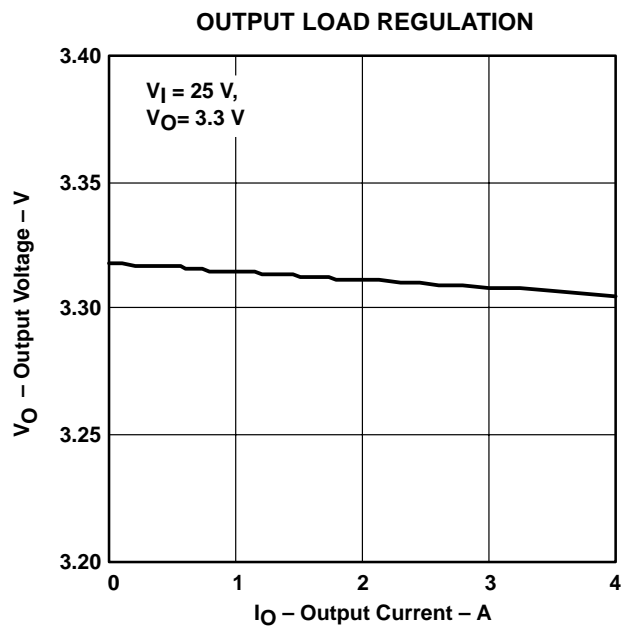


Figure 73

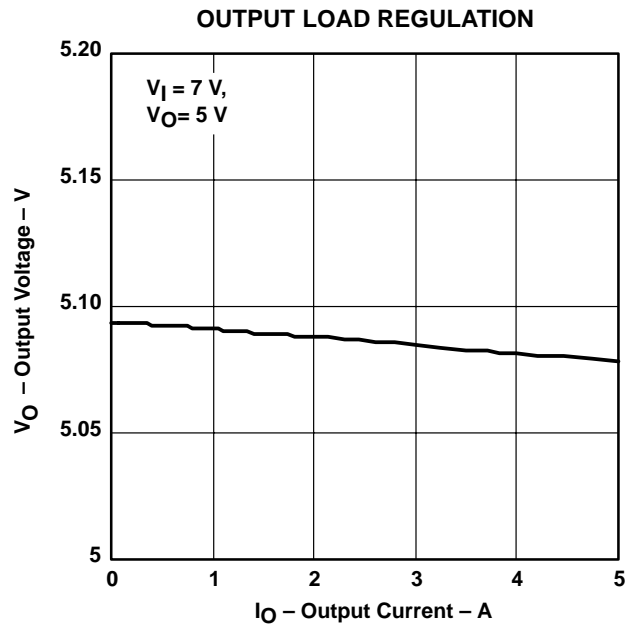


Figure 74

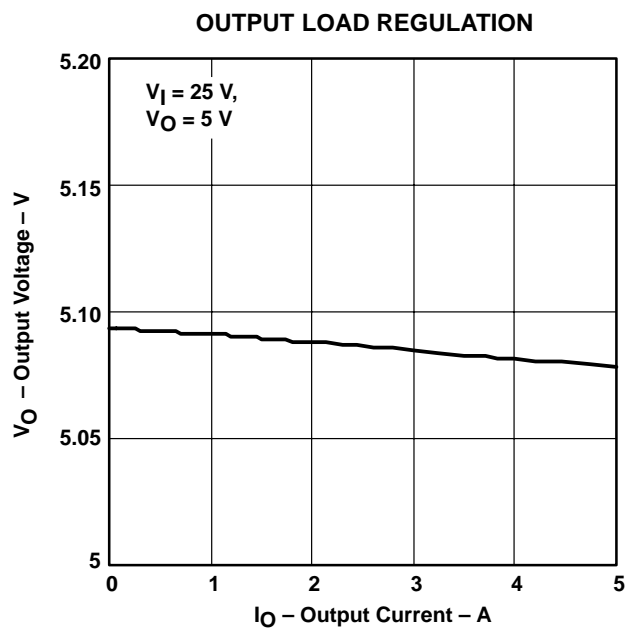


Figure 75

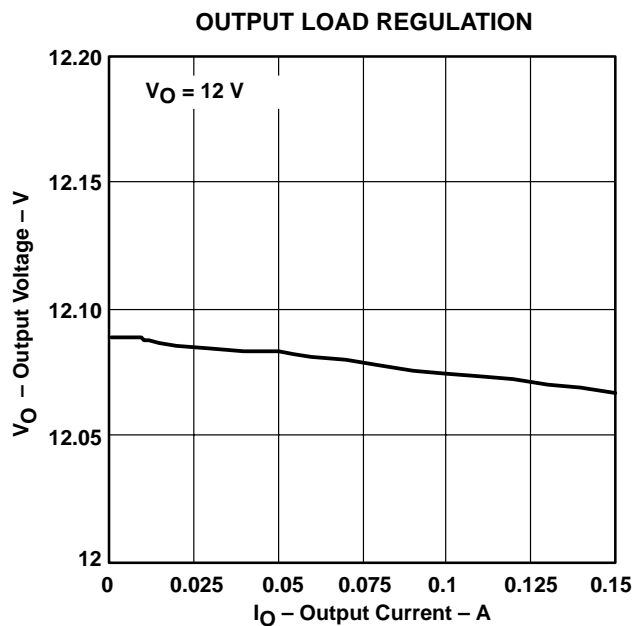


Figure 76

APPLICATION INFORMATION

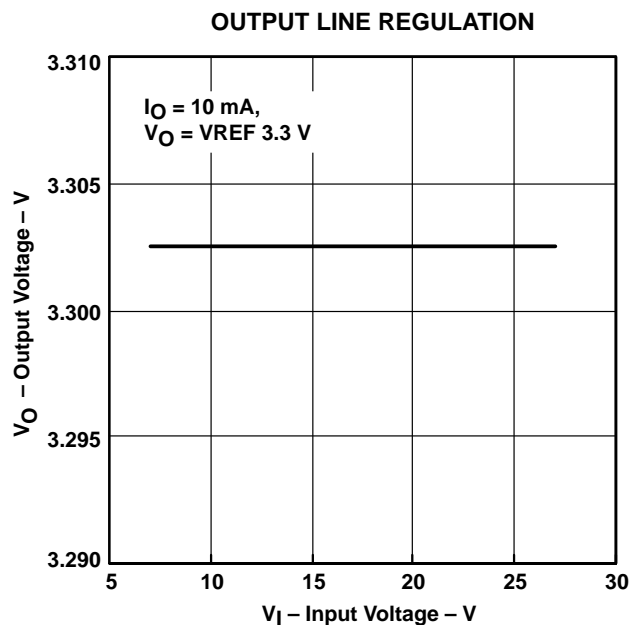


Figure 77

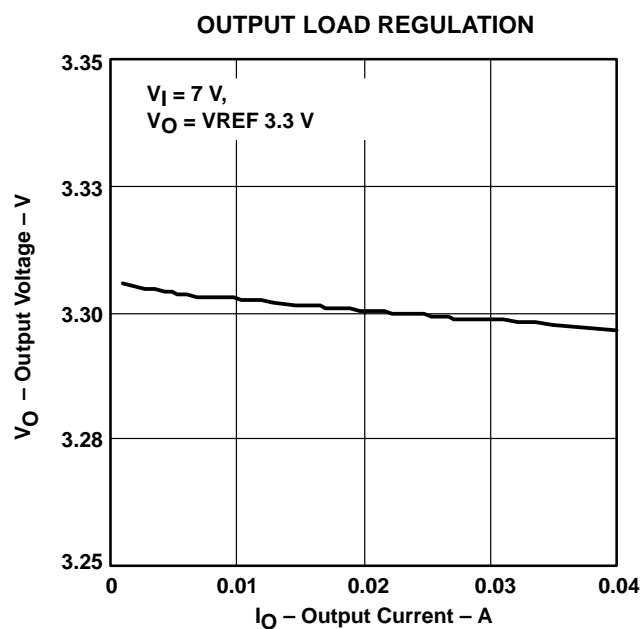


Figure 78

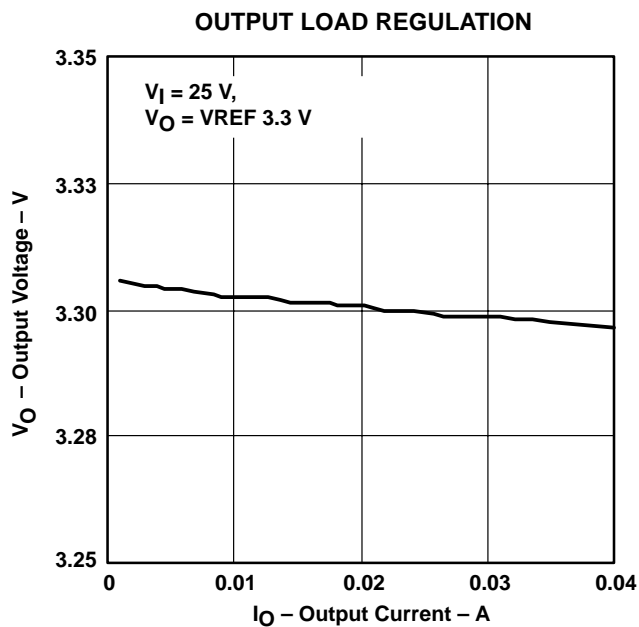


Figure 79

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APPLICATION INFORMATION

2.5 V OUTPUT VOLTAGE RIPPLE

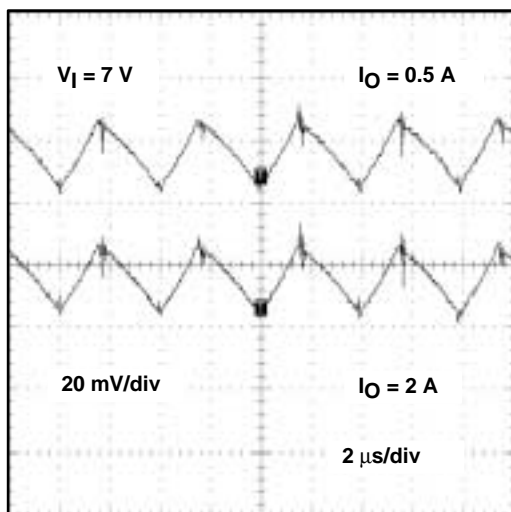


Figure 80

3.3 V OUTPUT VOLTAGE RIPPLE

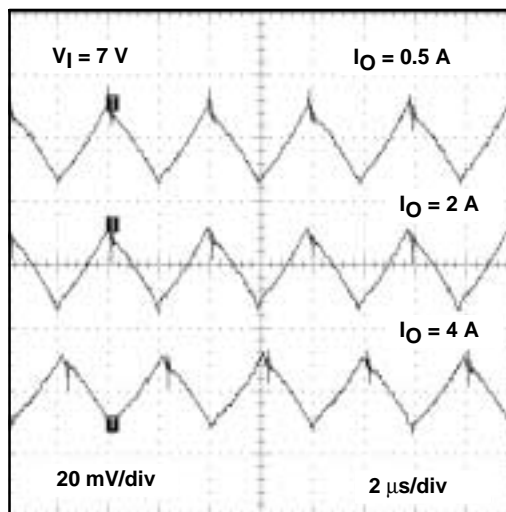


Figure 81

5 V OUTPUT VOLTAGE RIPPLE

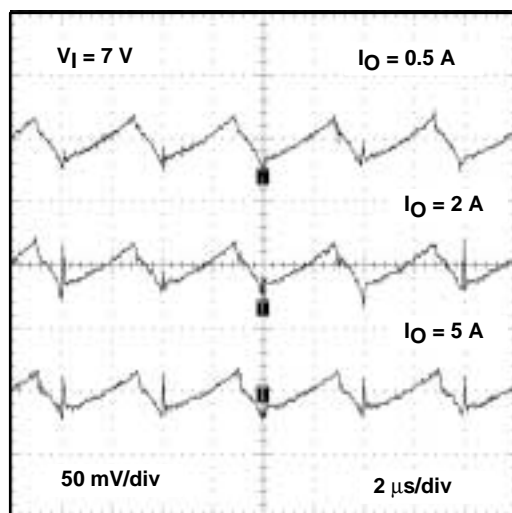


Figure 82

12 V OUTPUT VOLTAGE RIPPLE

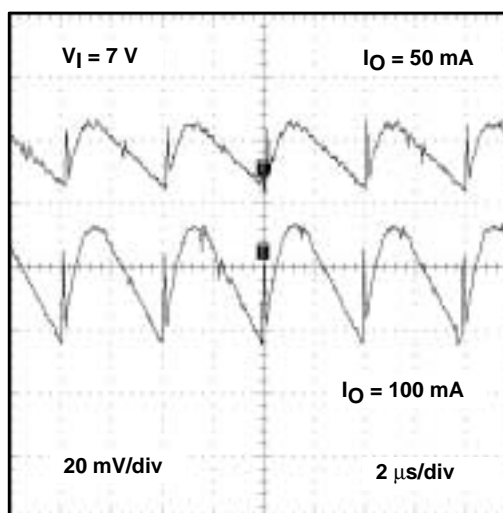


Figure 83

APPLICATION INFORMATION

2.5 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE

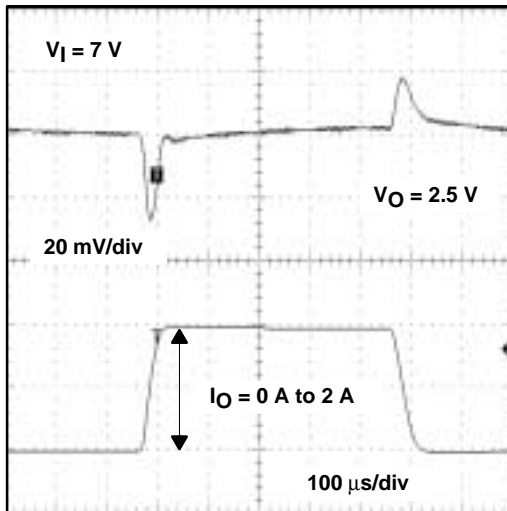


Figure 84

2.5 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE

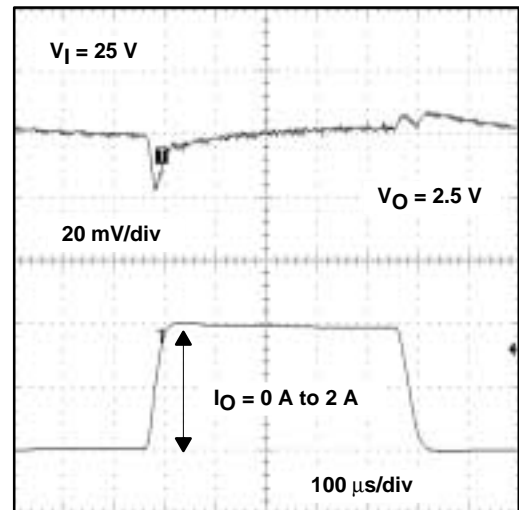


Figure 85

3.3 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE

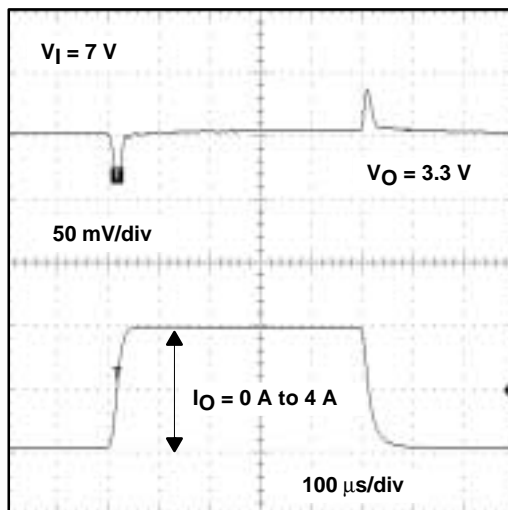


Figure 86

3.3 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE

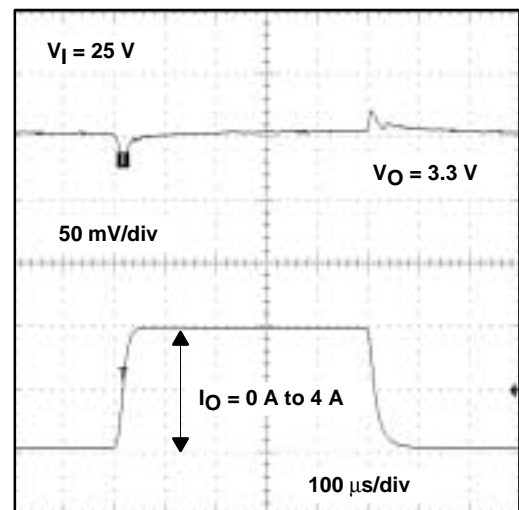


Figure 87

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APPLICATION INFORMATION

**5 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE**

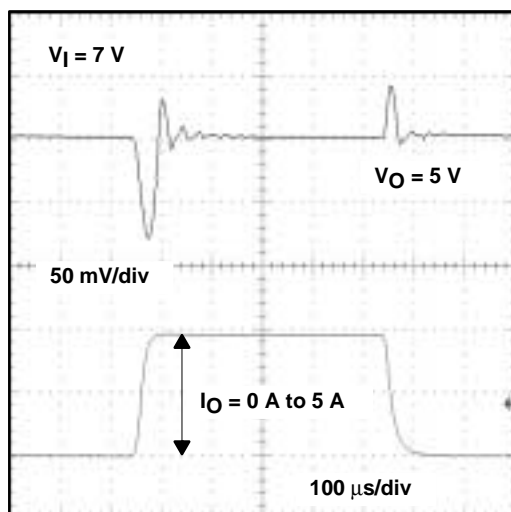


Figure 88

**5 V OUTPUT VOLTAGE
LOAD TRANSIENT RESPONSE**

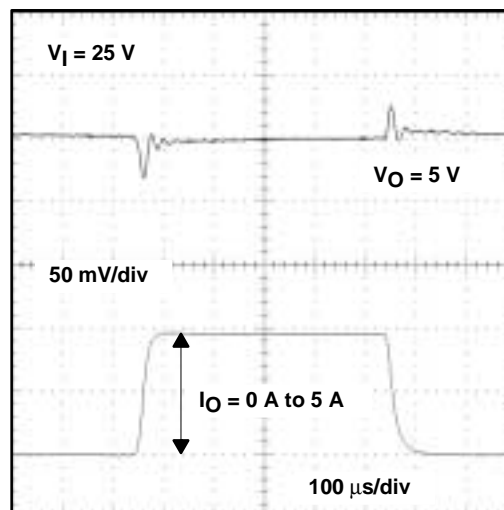


Figure 89

Table 4. Bill of Materials

| REF. | PN | DESCRIPTION | MFG. | SIZE |
|------|-----------------|--|-------|-------------|
| C01 | Open | Capacitor, electrolytic, 330 μ F, 35 V | Sanyo | 10x10 mm |
| C02 | Standard | Capacitor, ceramic, 2200 pF | | 805 |
| C03 | Standard | Capacitor, ceramic, 0.01 μ F | | 805 |
| C04 | Standard | Capacitor, ceramic, 56 pF | | 805 |
| C05 | Standard | Capacitor, ceramic, 0.1 μ F | | 805 |
| C06 | Standard | Capacitor, ceramic, 0.022 μ F | | 805 |
| C07 | Standard | Open | | 805 |
| C08 | Standard | Capacitor, ceramic, 0.01 μ F | | 805 |
| C09 | Standard | Capacitor, ceramic, 2200 pF | | 805 |
| C10 | Standard | Capacitor, ceramic, 1.0 μ F | | 805 |
| C11A | 10TPB220M | Capacitor, POSCAP, 220 μ F, 10 V | Sanyo | 7.3x4.3 mm |
| C11B | Open | Open, Capacitor, POSCAP | Sanyo | 7.3x4.3 mm |
| C12 | Standard | Capacitor, ceramic, 0.1 μ F | | 805 |
| C13 | TMK325BJ475MN-B | Capacitor, ceramic, 4.7 μ F | | 1210 (3225) |
| C14 | Standard | Capacitor, ceramic, 1.0 μ F | | 805 |
| C15A | 6TPB150M | Capacitor, POSCAP, 150 μ F, 6.3 V | Sanyo | 7.3x4.3 mm |
| C15B | 6TPB150M | Capacitor, POSCAP, 150 μ F, 6.3 V | Sanyo | 7.3x4.3 mm |
| C16A | 10TPB220M | Capacitor, POSCAP, 220 μ F, 10 V | Sanyo | 7.3x4.3 mm |
| C16B | Open | Open, Capacitor, POSCAP | Sanyo | 7.3x4.3 mm |

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Table 4. Bill of Materials (Continued)

| REF. | PN | DESCRIPTION | MFG. | SIZE |
|-----------------|----------------|---|-------------|------------|
| C17 | Standard | Capacitor, ceramic, 1.0 μ F | | 805 |
| C18 | Standard | Capacitor, ceramic, 2200 pF | | 805 |
| C19 | Standard | Capacitor, ceramic, 0.01 μ F | | 805 |
| C20 | TMK432BJ106MN | Capacitor, ceramic, 10 μ F, 25 V, X5R | Taiyo Yuden | 1812 (432) |
| C21 | TMK432BJ106MN | Capacitor, ceramic, 10 μ F, 25 V, X5R | Taiyo Yuden | 1812 (432) |
| C22 | Standard | Capacitor, ceramic, 0.01 μ F | | 805 |
| C23 | Standard | Open | | 805 |
| C24 | TMK432BJ106MN | Capacitor, ceramic, 10 μ F, 25 V, X5R | Taiyo Yuden | 1812 (432) |
| C25 | TMK432BJ106MN | Capacitor, ceramic, 10 μ F, 25 V, X5R | Taiyo Yuden | 1812 (432) |
| C26 | TMK432BJ106MN | Capacitor, ceramic, 10 μ F, 25 V, X5R | Taiyo Yuden | 1812 (432) |
| C27 | Standard | Capacitor, ceramic, 8200 pF | | 805 |
| C28 | Standard | Capacitor, ceramic, 8200 pF | | 805 |
| C29 | Standard | Capacitor, ceramic, 6800 pF | | 805 |
| C30 | Standard | Capacitor, ceramic, 0.1 μ F | | 805 |
| C31 | Standard | Capacitor, ceramic, 0.1 μ F | | 805 |
| C32 | Standard | Capacitor, ceramic, 0.1 μ F | | 805 |
| D1 | MBR0540T1 | Diode, Schottky, 40 V, 500 mA | Motorola | 3.7x1.6 mm |
| D2 | MBR0540T1 | Diode, Schottky, 40 V, 500 mA | Motorola | 3.7x1.6 mm |
| D3 | MBR0540T1 | Diode, Schottky, 40 V, 500 mA | Motorola | 3.7x1.6 mm |
| D4 | RB160L-40-TE25 | Diode, Schottky, 40 V, 1 A | Rohm | 4.5x2.6 mm |
| D5 | EC31QS04 | Diode, Schottky, 40 V, 3 A | Nihon Inter | 5.0x2.5 mm |
| D6 | EC31QS04 | Diode, Schottky, 40 V, 3 A | Nihon Inter | 5.0x2.5 mm |
| D7 | EC31QS04 | Diode, Schottky, 40 V, 3 A | Nihon Inter | 5.0x2.5 mm |
| JP00-JP06 | WL-8 | Header, straight, 3-pin | Mac8 | |
| JP8 | WL-8 | Header, straight, 3-pin | Mac8 | |
| JP00-JP06 shunt | JS-1 | Jumper socket | Mac8 | |
| JP8 shunt | JS-1 | Jumper socket | Mac8 | |
| L1 | CDRH127-100 | Inductor, 10 μ H, 5.4 A | Sumida | 12x12 mm |
| L2 | CDRH127-6R1 | Inductor, 6.1 μ H, 6.6 A | Sumida | 12x12 mm |
| L3 | CDRH125-100 | Inductor, 10 μ H, 4.0 A | Sumida | 12x12 mm |
| L4 | CDRH5D28-220 | Inductor, 22 μ H, 0.9 A | Sumida | 5.7x5.7 mm |
| R01A | Standard | Resistor, 15 k Ω , 1% | | 805 |
| R01B | Standard | Resistor, 18 k Ω , 1% | | 805 |
| R02A | Standard | Resistor, 10 k Ω , 1% | | 805 |
| R02B | Standard | Open | | 805 |
| R03 | Standard | Resistor, 470 Ω , 5% | | 805 |
| R04 | Standard | Resistor, 470 Ω , 5% | | 805 |
| R05A | Standard | Resistor, 10 k Ω , 1% | | 805 |
| R05B | Standard | Open | | 805 |
| R06A | Standard | Resistor, 1.8 k Ω , 1% | | 805 |
| R06B | Standard | Resistor, 10 k Ω , 1% | | 805 |
| R07 | Standard | Resistor, 10 k Ω , 1% | | 805 |



TPS5140

FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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APPLICATION INFORMATION

Table 4. Bill of Materials (Continued)

| REF. | PN | DESCRIPTION | MFG. | SIZE |
|---------|----------|--|-----------|------|
| R08 | Standard | Resistor, 24 k Ω , 1% | | 805 |
| R09 | Standard | Resistor, 18 k Ω , 1% | | 805 |
| R10A | Standard | Resistor, 2 k Ω , 1% | | 805 |
| R10B | Standard | Resistor, 16 k Ω , 1% | | 805 |
| R11A | Standard | Resistor, 10 k Ω , 1% | | 805 |
| R11B | Standard | Open | | 805 |
| R12 | Standard | Resistor, 470 Ω , 5% | | 805 |
| R13 | Standard | Resistor, 100 k Ω , 5 % | | 805 |
| R14 | Standard | Open | | 805 |
| R16 | Standard | Resistor, 100 k Ω , 5 % | | 805 |
| R17 | Standard | Open | | 805 |
| R19 | Standard | Resistor, 15 Ω , 5 % | | 805 |
| R22 | Standard | Resistor, 15 Ω , 5 % | | 805 |
| R24 | Standard | Resistor, 15 Ω , 5 % | | 805 |
| R25 | Standard | Resistor, 220 Ω , 5 % | | 805 |
| R26 | Standard | Resistor, 470 Ω , 5 % | | 805 |
| R27 | Standard | Resistor, 100 Ω , 5 % | | 805 |
| Q01–Q06 | FDS6612A | Transistor, MOSFET, N–ch, 30 V, 8.4 A, 26 m Ω | Fairchild | SO–8 |
| U1 | TPS5140 | IC, Quad controller | TI | TQFP |

Table 5. Vendor and Source Information

| MATERIAL | SOURCE | PART NUMBER | DISTRIBUTORS |
|---|---------------|--|--|
| MOSFETS (Q01– Q06) | In EVM design | FDS6612A (Fairchild) | Local Distributor |
| | Second source | IRF9410 (International Rectifier) | |
| MAIN DIODES (D5 – D7) | In EVM design | EC31QS04 (Nihon Inter) | 81–3–3342–5407 |
| CERAMIC CAPACITORS (C20, C21, C24 , C25, C26) | In EVM design | TMK432BJ106MN (Taiyo Yuden) | http://www.t-yuden.com http://www.yuden.co.jp |
| INDUCTORS (L1 – L4) | In EVM design | CDRH125–100 CDRH127–6R1 CDRH127–100 CDRH5D28–220 (Sumida) | http://www.sUmida.com |



EVM Layout



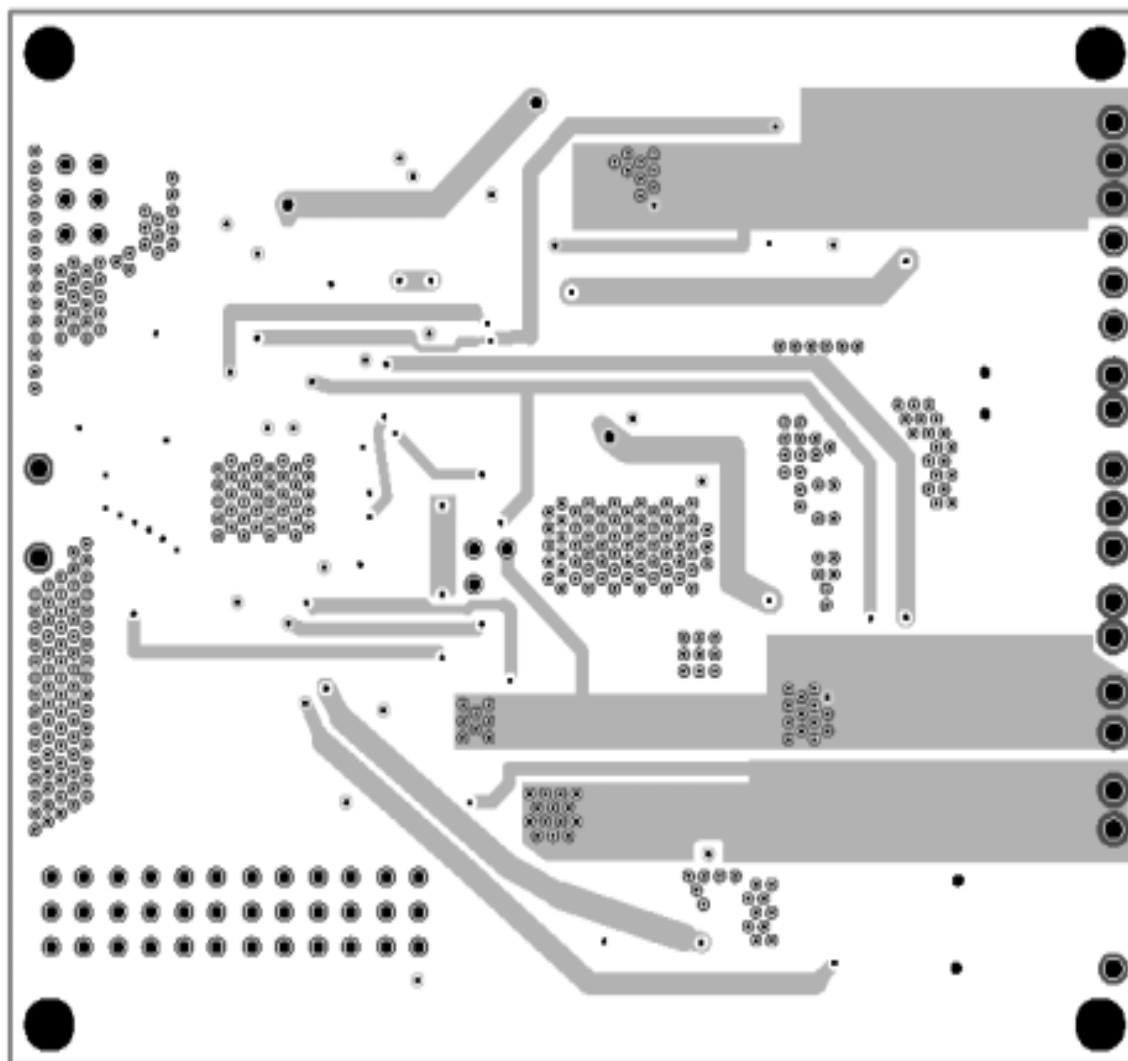
Figure 90. EVM Top Layer

TPS5140 FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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APPLICATION INFORMATION

EVM Layout (continued)

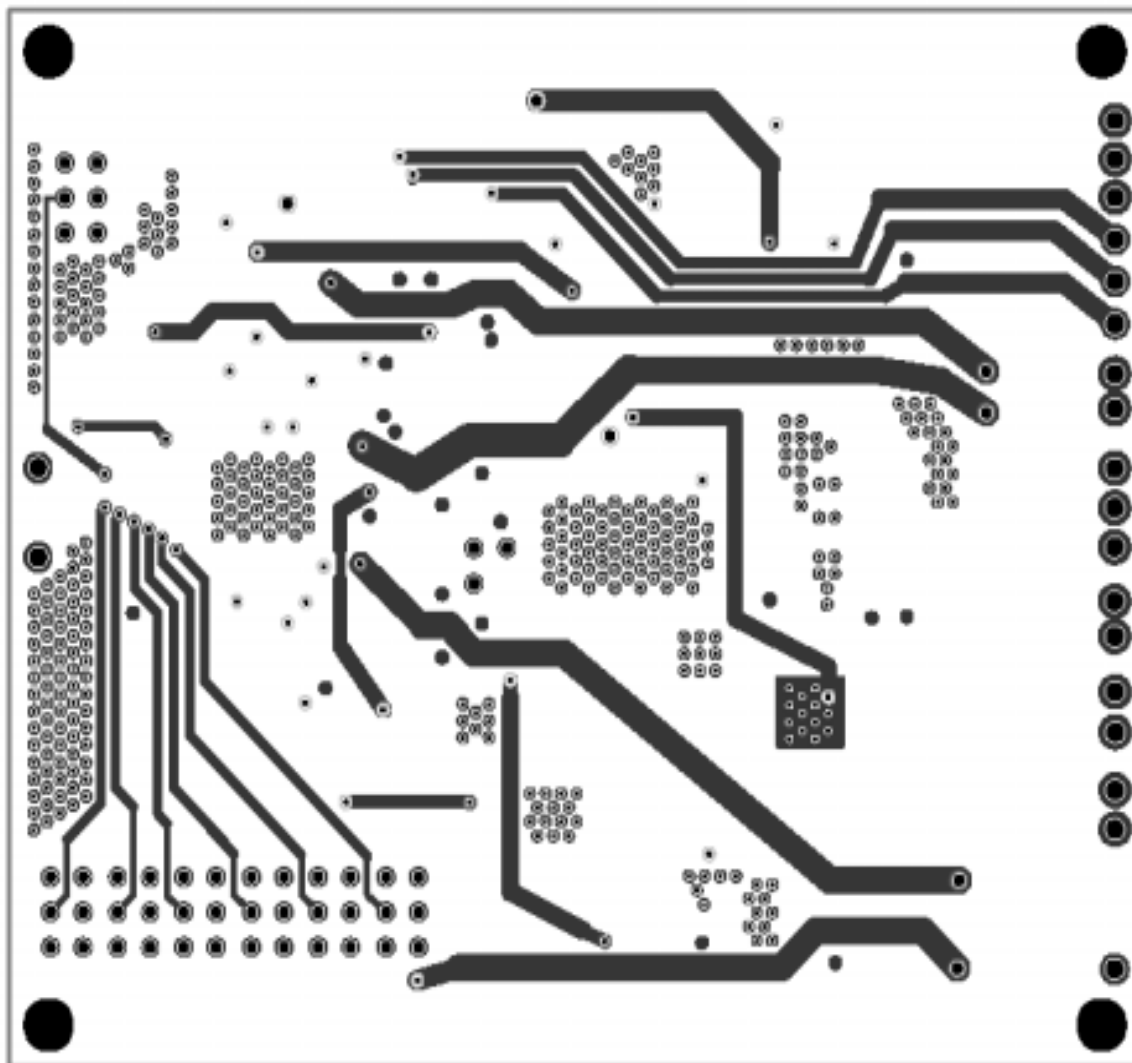


2nd Layer

Figure 91. EVM Second Layer

APPLICATION INFORMATION

EVM Layout (continued)



3rd Layer

Figure 92. EVM Third Layer



TEXAS
INSTRUMENTS

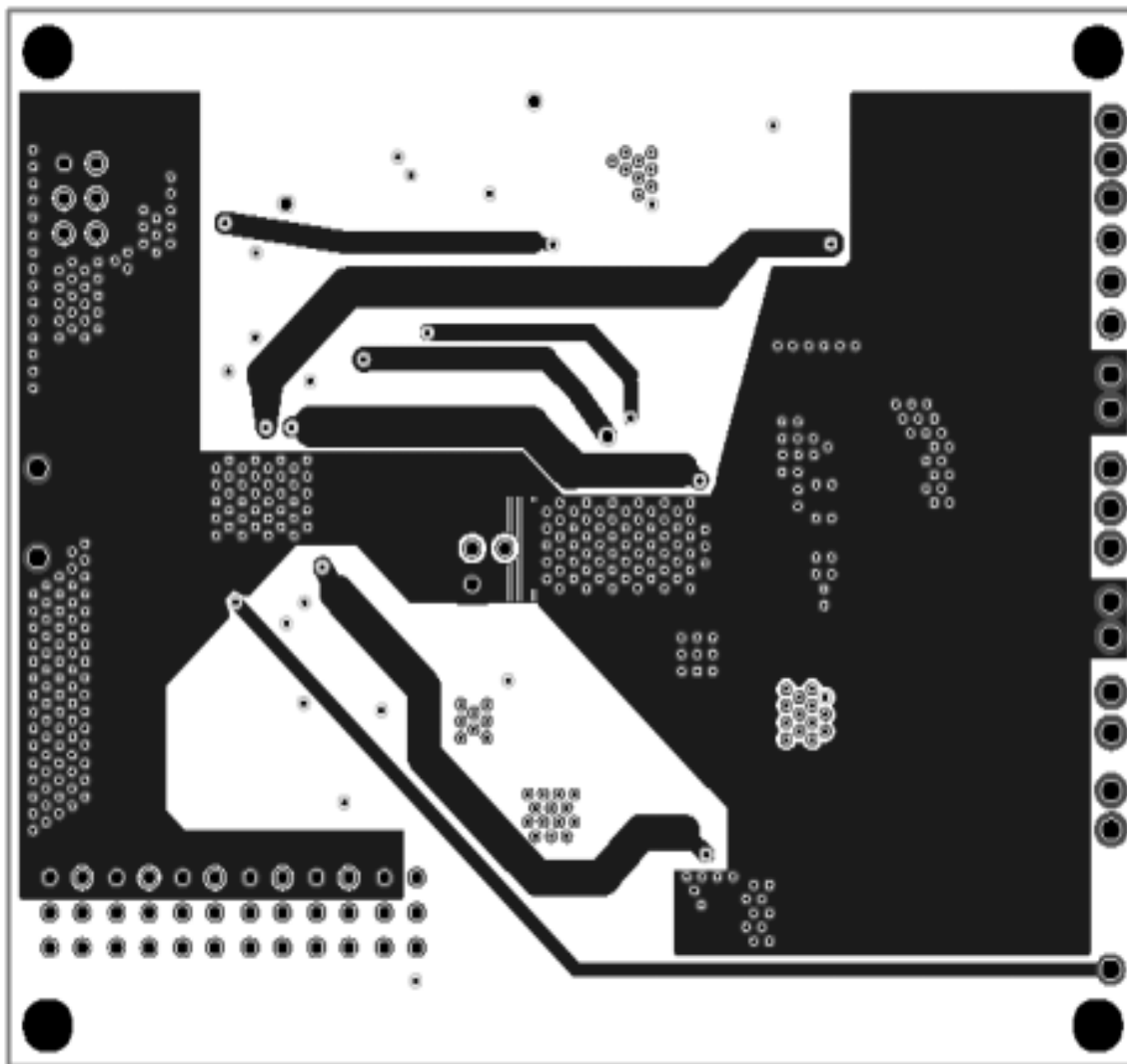
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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APPLICATION INFORMATION

EVM Layout (continued)



Bottom Layer (Top View)

Figure 93. EVM Bottom Layer (Top View)

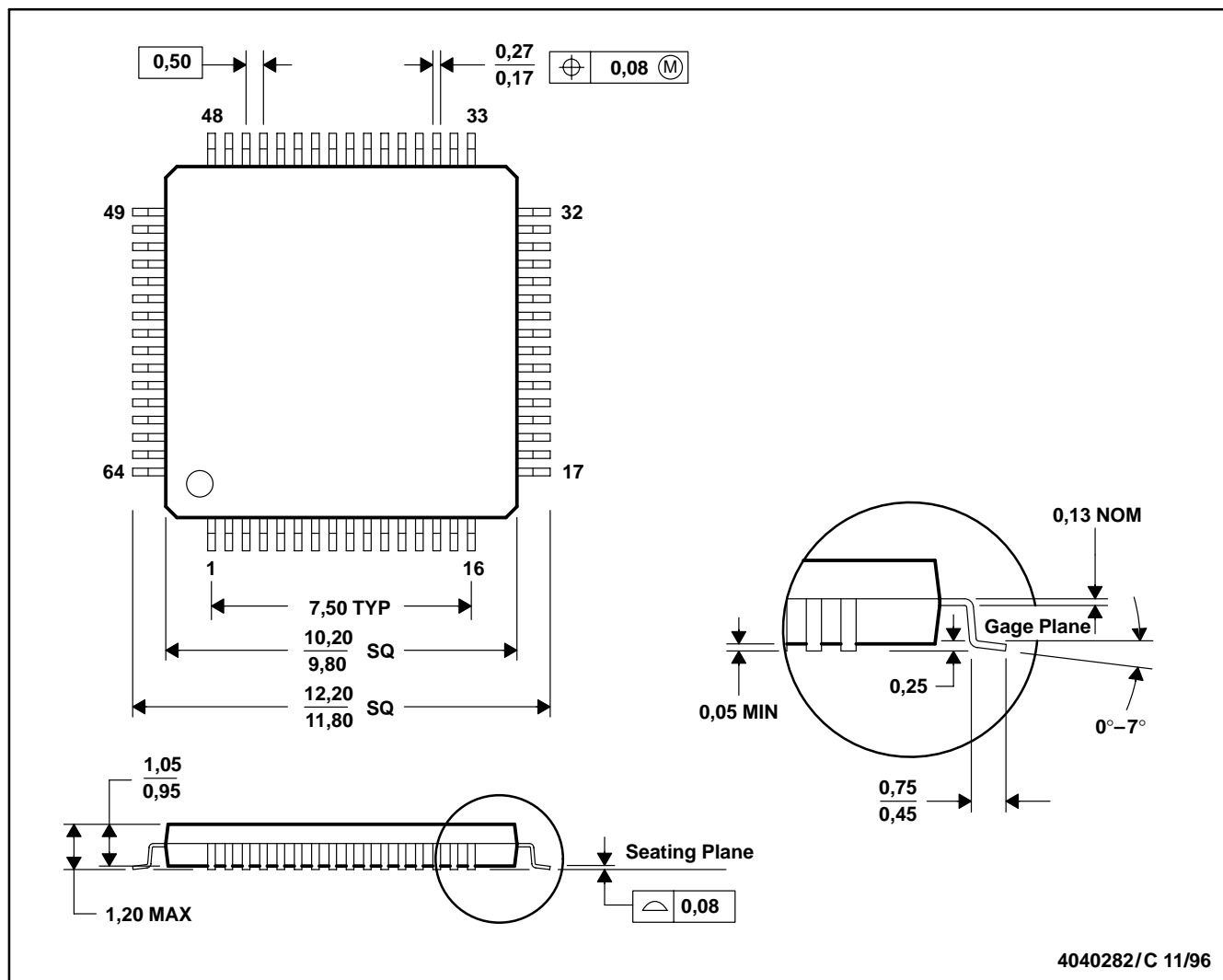
TPS5140 FOUR-CHANNEL DC/DC CONTROLLER FOR NOTEBOOK PC POWER

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MECHANICAL DATA

PAG (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS5140PAGR | Active | Production | TQFP (PAG) 64 | 1500 LARGE T&R | Yes | NIPDAU | Level-4-260C-72 HR | -20 to 85 | TPS5140 |
| TPS5140PAGR.A | Active | Production | TQFP (PAG) 64 | 1500 LARGE T&R | Yes | NIPDAU | Level-4-260C-72 HR | -20 to 85 | TPS5140 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS5140PAGR | TQFP | PAG | 64 | 1500 | 330.0 | 24.4 | 13.0 | 13.0 | 1.5 | 16.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS5140PAGR | TQFP | PAG | 64 | 1500 | 350.0 | 350.0 | 43.0 |

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