TPS6020x Regulated 3.3 V, 100-mA Low-Ripple Charge Pump Low Power DC/DC Converters

1 Features

- Regulated 3.3-V Output Voltage With up to 100-mA Output Current From a 1.8-V to 3.6-V Input Voltage
- Less Than 5-mV (PP) Output Voltage Ripple Achieved With Push-Pull Topology
- Integrated Low-Battery and Power-Good Detector
- Switching Frequency Can Be Synchronized to External Clock Signal
- Extends Battery Usage With up to 90% Efficiency and 35-µA Quiescent Supply Current
- Reliable System Shutdown Because Output Capacitor Is Discharged When Device Is Disabled
- Easy-to-Design, Low-Cost, Low-EMI Power Supply Since No Inductors Are Used
- 0.05-µA Shutdown Current, Battery Is Isolated From Load in Shutdown Mode
- Compact Converter Solution in UltraSmall 10-pin MSOP With Only Four External Capacitors Required
- Evaluation Module Available (TPS60200EVM-145)

2 Applications

- Two Battery Cells to 3.3-V Conversion
- MP3 Portable Audio Players
- Battery-Powered Microprocessor Systems
- Backup-Battery Boost Converters
- PDAs, Organizers, and Cordless Phones
- Handheld Instrumentation
- Glucose Meters and Other Medical Instruments

3 Description

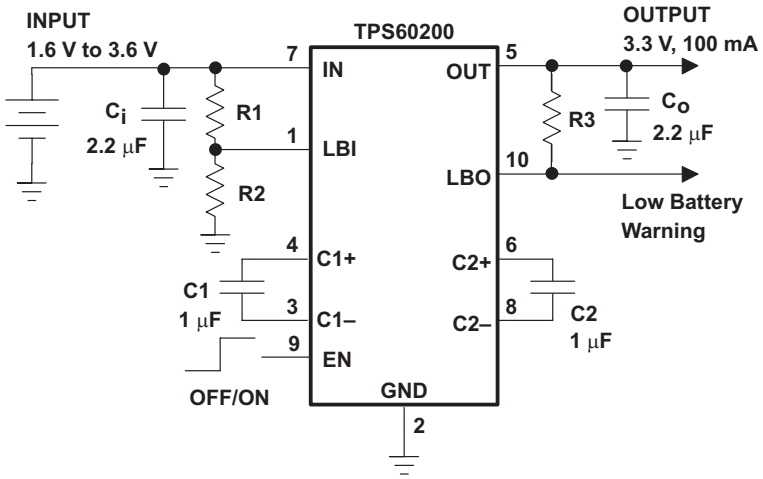
The TPS6020x step-up, regulated charge pumps generate a 3.3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage. The devices are typically powered by two Alkaline, NiCd or NiMH battery cells and operate down to a minimum supply voltage of 1.6 V. Continuous output current is a minimum of 100 mA for the TPS60200 and TPS60201 and 50 mA for the TPS60202 and TPS60203, all from a 2-V input. Only four external capacitors are needed to build a complete low-ripple DC/DC converter. The push-pull operating mode of two single-ended charge pumps assures the low output voltage ripple as current is continuously transferred to the output.

Device Information(1)

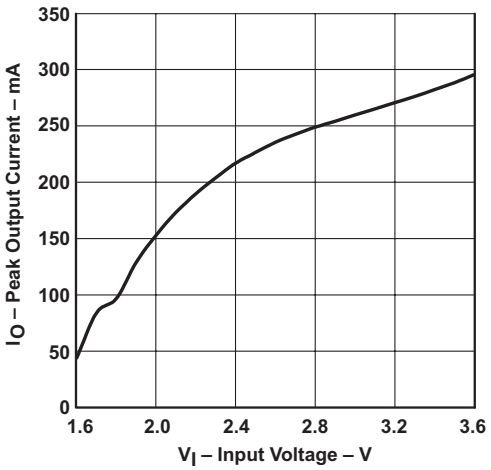
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6020x	MSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application with Low-Battery Warning



TPS60200 Peak Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2000) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison Tables

Table 1. Available Options

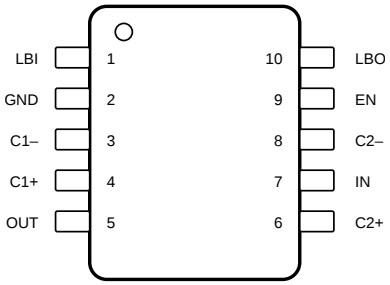
PART NUMBER	DEVICE FEATURES	OUTPUT CURRENT (mA)	OUTPUT VOLTAGE (V)	T_A
TPS60200	Low-battery detector	100	3.3	–40°C to 85°C
TPS60201	Power-good detector	100	3.3	–40°C to 85°C
TPS60202	Low-battery detector	50	3.3	–40°C to 85°C
TPS60203	Power-good detector	50	3.3	–40°C to 85°C

Table 2. Other Charge Pump DC/DC Converters

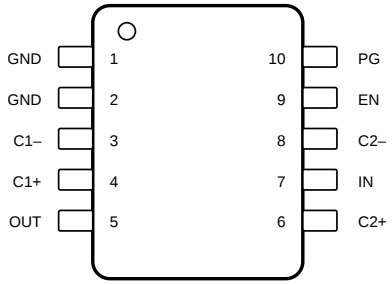
PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3 V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3 V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5 V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5 V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3 V, 200-mA high-efficiency charge pump with low battery comparator
TPS60121	2-cell to regulated 3.3 V, 200-mA high-efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3 V, 100-mA high-efficiency charge pump with low battery comparator
TPS60123	2-cell to regulated 3.3 V, 100-mA high-efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5 V, 300-mA high-efficiency charge pump with low battery comparator
TPS60131	3-cell to regulated 5 V, 300-mA high-efficiency charge pump with power-good comparator
TPS60132	3-cell to regulated 5 V, 150-mA high-efficiency charge pump with low battery comparator
TPS60133	3-cell to regulated 5 V, 150-mA high-efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5 V, 100-mA charge pump voltage tripler with low battery comparator
TPS60141	2-cell to regulated 5 V, 100-mA charge pump voltage tripler with power-good comparator

6 Pin Configuration and Functions

TPS60200 and TPS60202 DGS Package
10-Pin MSOP
Top View



TPS60201 and TPS60203 DGS Package
10-Pin MSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS60200, TPS60202	TPS60201, TPS60203		
C1+	4	4	—	Positive terminal of the flying capacitor C1
C1–	3	3	—	Negative terminal of the flying capacitor C1
C2+	6	6	—	Positive terminal of the flying capacitor C2
C2–	8	8	—	Negative terminal of the flying capacitor C2
EN	9	9	I	Device-enable input. Three operating modes can be programmed with the EN pin. EN = Low disables the device. Output and input are isolated in the shutdown mode and the output capacitor is automatically discharged. EN = High lets the device run from the internal oscillator. If an external clock signal is applied to the EN pin, the device is in Sync–Mode and runs synchronized at the frequency of the external clock signal.
GND	2	1, 2		Ground
IN	7	7	I	Supply input. Bypass IN to GND with a capacitor of the same size as C_O.
LBI	1	—	I	Low-battery detector input for TPS60200 and TPS60202. A low-battery warning is generated at the LBO pin when the voltage on LBI drops below the threshold of 1.18 V. Connect LBI to GND if the low-battery detector function is not used. For the devices TPS60201 and TPS60203, this pin has to be connected to ground (GND pin).
LBO	10	—	O	Open-drain low-battery detector output for TPS60200 and TPS60202. This pin is pulled low if the voltage on LBI drops below the threshold of 1.18 V. A pullup resistor should be connected between LBO and OUT or any other logic supply rail that is lower than 3.6 V.
OUT	5	5	O	Regulated 3.3-V power output. Bypass OUT to GND with the output filter capacitor C_O.
PG	—	10	O	Open-drain power-good detector output for TPS60201 and TPS60203. As soon as the voltage on OUT reaches about 90% of it is nominal value this pin goes active high. A pullup resistor should be connected between PG and OUT or any other logic supply rail that is lower than 3.6 V.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN, OUT, EN, LBI, LBO, PG to GND	–0.3	3.6	V
	C1+, C2+ to GND	–0.3	V_O + 0.3	
	C1–, C2– to GND	–0.3	V_I + 0.3	
Continuous total power dissipation	T_A ≤ 25°C power rating		424	mW
	T_A = 70°C power rating		187	
	T_A = 85°C power rating		136	
Continuous output current	TPS60200, TPS60201		150	mA
	TPS60202, TPS60203		75	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	1.6		3.6	V
C_i	Input capacitor		2.2		µF
C1, C2	Flying capacitors		1		µF
C_O	Output capacitor		2.2		µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS6020x DGS (MSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

C_i = 2.2 µF, C1 = C2 = 1 µF, C_O = 2.2 µF, T_A = –40°C to 85°C, V_I = 2.4 V, and EN = V_I (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(MAX)}$	Maximum continuous output current	TPS60200 and TPS60201, V_I = 2 V	100			mA
		TPS60202 and TPS60203, V_I = 2 V	50			
V_O	Output voltage	1.6 V < V_I < 1.8 V, 0 < I_O < 0.25 × $I_{O(MAX)}$	3			V
		1.8 V < V_I < 2 V, 0 < I_O < 0.5 × $I_{O(MAX)}$	3.17		3.43	
		2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	
		3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	
V_{PP}	Output voltage ripple	I_O = $I_{O(MAX)}$		5		mV_{PP}
$I_{(Q)}$	Quiescent current (no-load input current)	I_O = 0 mA, V_I = 1.8 V to 3.6 V		35	70	µA
$I_{(SD)}$	Shutdown supply current	EN = 0 V		0.05	1	µA
$f_{(OSC)}$	Internal switching frequency		200	300	400	kHz
$f_{(SYNC)}$	External clock signal frequency		400	600	800	kHz
	External clock signal duty cycle		30%		70%	
V_{IL}	EN input low voltage	V_I = 1.6 V to 3.6 V			0.3 × V_I	V
V_{IH}	EN input leakage current	V_I = 1.6 V to 3.6 V	0.7 × V_I			V
$I_{lkg(EN)}$	EN input leakage current	EN = 0 V or V_I		0.01	0.1	µA
	Output capacitor auto discharge time	EN is set from V_I to GND, time until V_O < 0.5 V		0.6		ms
	Output resistance in shutdown	EN = 0 V		70		Ω
	LinSkip threshold	V_I = 2.2 V		7		mA
	Output load regulation	10 mA < I_O< $I_{O(MAX)}$, T_A = 25°C		0.01%		mA
	Output line regulation	2 V < V_I < 3.3 V, I_O = 0.5 × $I_{O(MAX)}$, T_A = 25°C		0.6%		V
$I_{(SC)}$	Short-circuit current	V_I = 2.4 V, V_O = 0 V		60		mA

7.6 Electrical Characteristics – Low-Battery Comparator

TPS60200 and TPS60202 devices only at T_A = –40°C to 85°C, V_I = 2.4 V, and EN = V_I (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LBI)}$	LBI trip voltage	V_I = 1.6 V to 2.2 V, T_C = 0°C to 70°C	1.13	1.18	1.23	V
	LBI trip voltage hysteresis	For rising voltage at LBI		10		mV
$I_{I(LBI)}$	LBI input current	$V_{(LBI)}$ = 1.3 V		2	50	nA
$V_{O(LBO)}$	LBO output voltage low	$V_{(LBI)}$ = 0 V, $I_{(LBO)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	µA

(1) During start-up of the converter, the LBO output signal is invalid for the first 500 µs.

7.7 Electrical Characteristics – Power-Good Comparator

TPS60201 and TPS60203 devices only at T_A = –40°C to 85°C, V_I = 2.4 V, and EN = V_I (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage	T_C = 0°C to 70°C	0.87 × V_O	0.91 × V_O	0.95 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	V_O decreasing, T_C = 0°C to 70°C		1%		
$V_{O(PG)}$	Power-good output voltage low	V_O = 0 V, $I_{(PG)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	µA

(1) During start-up of the converter, the PG output signal is invalid for the first 500 µs.

7.8 Typical Characteristic

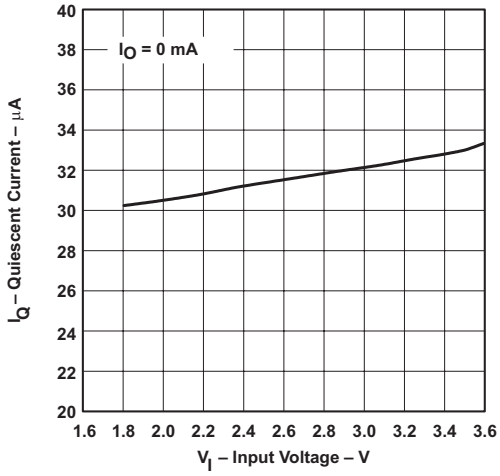


Figure 1. Quiescent Supply Current vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS6020x charge pumps provide a regulated 3.3-V output from a 1.8-V to 3.6-V input. They deliver up to 100-mA load current while maintaining the output at 3.3 V ± 4%. Designed specifically for space-critical, battery-powered applications, the complete converter requires only four external capacitors. The device is using the push-pull topology to achieve lowest output voltage ripple. The converter is also optimized for smallest board space. It makes use of small-sized capacitors, with the highest output current rating per output capacitance and package size.

The TPS6020x circuits consist of an oscillator, a 1.18-V voltage reference, an internal resistive feedback circuit, an error amplifier, two charge pump power stages with high current MOSFET switches, a shutdown and start-up circuit, a control circuit, and an auto-discharge transistor (see *Functional Block Diagrams*).

8.2 Functional Block Diagrams

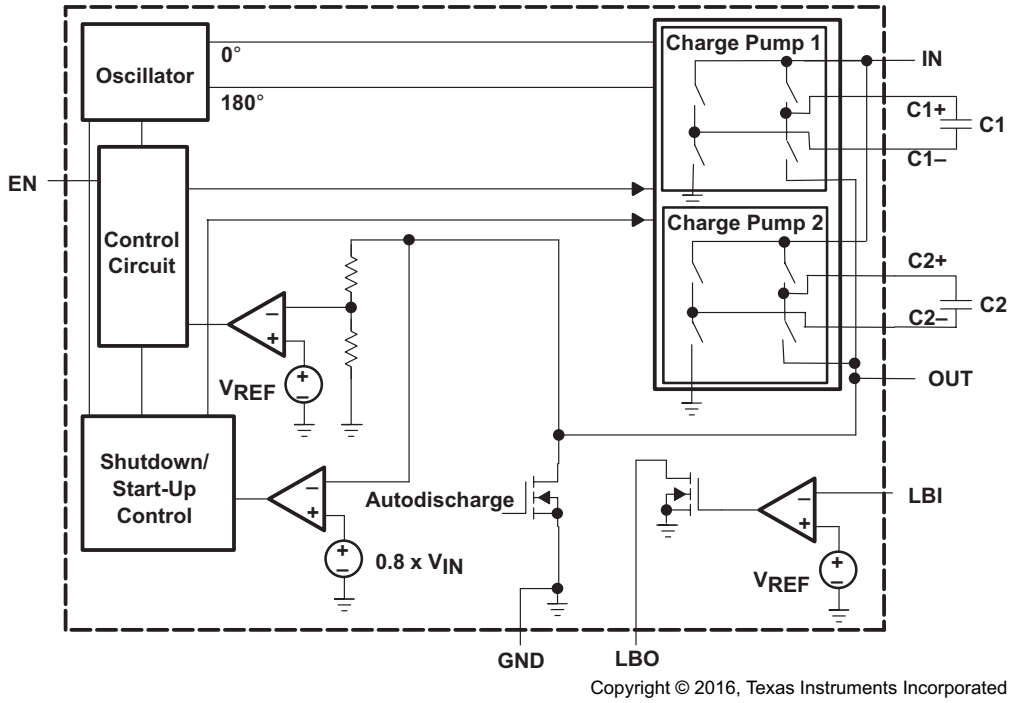


Figure 2. TPS60200 and TPS60202 With Low-Battery Detector

Functional Block Diagrams (continued)

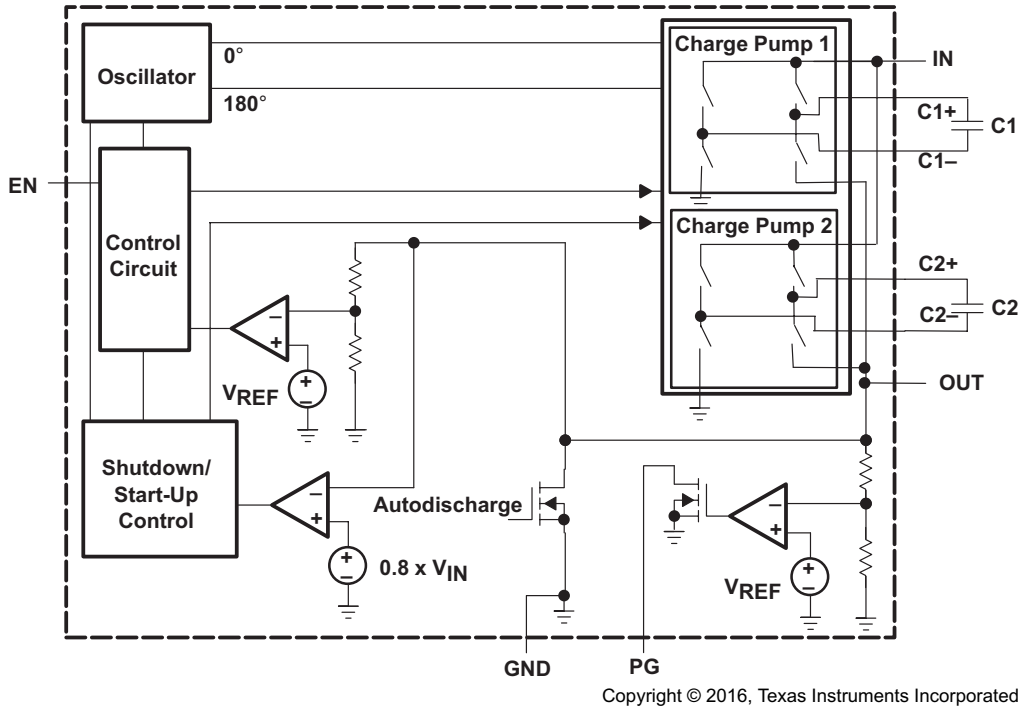


Figure 3. TPS60201 and TPS60203 With Power-Good Detector

8.3 Feature Description

8.3.1 Start-Up, Shutdown, and Auto-Discharge

During start-up, that is when EN is set from logic low to logic high, the output capacitor is directly connected to IN and charged up with a limited current until the output voltage V_O reaches 0.8 × V_I. When the start-up comparator detects this limit, the converter begins switching. This precharging of the output capacitor guarantees a short start-up time. In addition, the inrush current into an empty output capacitor is limited. The converter can start into a full load, which is defined by a 33-Ω or 66-Ω resistor, respectively.

Driving EN low disables the converter. This disables all internal circuits and reduces the supply current to only 0.05 µA. The device exits shutdown once EN is set high. When the device is disabled, the load is isolated from the input. This is an important feature in battery-operated products because it extends the products shelf life.

Additionally, the output capacitor will automatically be discharged after EN is taken low. This ensures that the system, when switched off, is in a stable and reliable condition because the supply voltage is removed from the supply pins.

8.3.2 Synchronization to an External Clock Signal

The operating frequency of the charge pump is limited to 400 kHz to avoid interference in the sensitive 455-kHz IF band. The device can either run from the integrated oscillator, or an external clock signal can be used to drive the charge pump. The maximum frequency of the external clock signal is 800 kHz. The switching frequency used internally to drive the charge pump power stages is half of the external clock frequency. The external clock signal is applied to the EN pin. The device will switch off if the signal on EN is hold low for more than 10 µs.

When the load current drops below the LinSkip current threshold, the devices will enter the pulse-skip mode but stay synchronized to the external clock signal.

Feature Description (continued)

8.3.3 Power-Good Detector

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected.

8.4 Device Functional Modes

8.4.1 Push-Pull Operating Mode

The two single-ended charge pump power stages operate in the so-called push-pull operating mode, that is they operate with a 180°C phase shift. Each single-ended charge pump transfers charge into its transfer capacitor (C1 or C2) in one half of the period. During the other half of the period (transfer phase), the transfer capacitor is placed in series with the input to transfer its charge to C_O. While one single-ended charge pump is in the charge phase, the other one is in the transfer phase. This operation assures an almost constant output current which ensures a low output ripple.

If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name voltage doubler). To provide a regulated fixed output voltage of 3.3 V, the TPS6020x devices use either pulse-skip or constant-frequency linear-regulation control mode. The mode is automatically selected based on the output current. If the load current is below the LinSkip current threshold, it switches into the power-saving pulse-skip mode to boost efficiency at low output power.

8.4.2 Constant-Frequency Mode

When the output current is higher then the LinSkip current threshold, the charge pump runs continuously at the switching frequency $f_{(OSC)}$. The control circuit, fed from the error amplifier, controls the charge on C1 and C2 by controlling the gates and hence the $r_{DS(ON)}$ of the integrated MOSFETs. When the output voltage decreases, the gate drive increases, resulting in a larger voltage across C1 and C2. This regulation scheme minimizes output ripple. Since the device switches continuously, the output signal contains well-defined frequency components, and the circuit requires smaller external capacitors for a given output ripple. However, constant-frequency mode, due to higher operating current, is less efficient at light loads. For this reason, the device switches seamlessly into the pulse-skip mode when the output current drops below the LinSkip current threshold.

8.4.3 Pulse-Skip Mode

The regulator enters the pulse-skip mode when the output current is lower than the LinSkip current threshold of 7 mA. In the pulse-skip mode, the error amplifier disables switching of the power stages when it detects an output voltage higher than 3.3 V. The controller skips switching cycles until the output voltage drops below 3.3 V. Then the error amplifier reactivates the oscillator and switching of the power stages starts again. A 30-mV output voltage offset is introduced in this mode.

The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except the voltage reference and error amplifier when the output is higher than 3.3 V. Even in pulse-skip mode the $r_{DS(ON)}$ of the MOSFETs is controlled. This way the energy per switching cycle that is transferred by the charge pump from the input to the output is limited to the minimum that is necessary to sustain a regulated output voltage, with the benefit that the output ripple is kept to a minimum. When switching is disabled from the error amplifier, the load is also isolated from the input.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The power-good output is an open-drain output that pulls low when the output is out of regulation. When the output rises to within 90% of its nominal voltage, the power-good output is released. Power-good is high impedance in shutdown. In normal operation, an external pullup resistor must be connected between PG and OUT, or any other voltage rail in the appropriate range. The resistor should be in the 100-k Ω to 1-M Ω range. If the PG output is not used, it should remain unconnected)

9.1.1 Capacitor Selection

The TPS6020x devices require only four external capacitors to achieve a very low output voltage ripple. The capacitor values are closely linked to the required output current. Low ESR (<0.1 Ω) capacitors should be used at input and output. In general, the transfer capacitors (C1 and C2) will be the smallest, a 1-µF value is recommended for maximum load operation. With smaller capacitor values, the maximum possible load current is reduced and the LinSkip threshold is lowered.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. TI recommends Ci be about two to four times as large as the flying capacitors C1 and C2.

The output capacitor (Co) should be at minimum the size of the input capacitor. The minimum required capacitance is 2.2 µF. Larger values will improve the load transient performance and will reduce the maximum output ripple voltage.

Only ceramic capacitors are recommended for input, output, and flying capacitors. Depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U- or Y5V-type capacitors will decrease in capacitance. Table 3 lists the recommended capacitor values.

Table 3. Recommended Capacitors Values (Ceramic X5R and X7R)

LOAD CURRENT, I_L (mA)	FLYING CAPACITORS, C1/C2 (µF)	INPU CAPACITOR, C_i (µF)	OUTPUT CAPACITOR, C_o (µF)	OUTPUT VOLTAGE RIPPLE IN LINEAR MODE, $V_{(P-P)}$ (mV)	OUTPUT VOLTAGE RIPPLE IN SKIP MODE, $V_{(P-P)}$ (mV)
0 to 100	1	2.2	2.2	3	20
0 to 100	1	4.7	4.7	3	10
0 to 100	1	2.2	10	3	7
0 to 100	2.2	4.7	4.7	3	10
0 to 50	0.47	2.2	2.2	3	20
0 to 25	0.22	2.2	2.2	5	15
0 to 10	0.1	2.2	2.2	5	15

9.2 Typical Applications

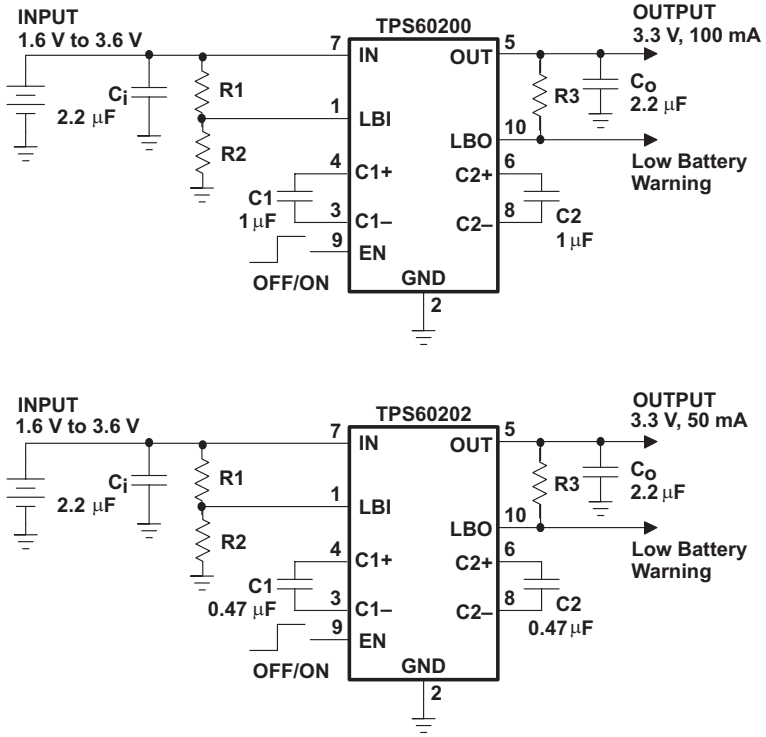


Figure 4. Typical Operating Circuit TPS60200 and TPS60202 With Low-Battery-Detector

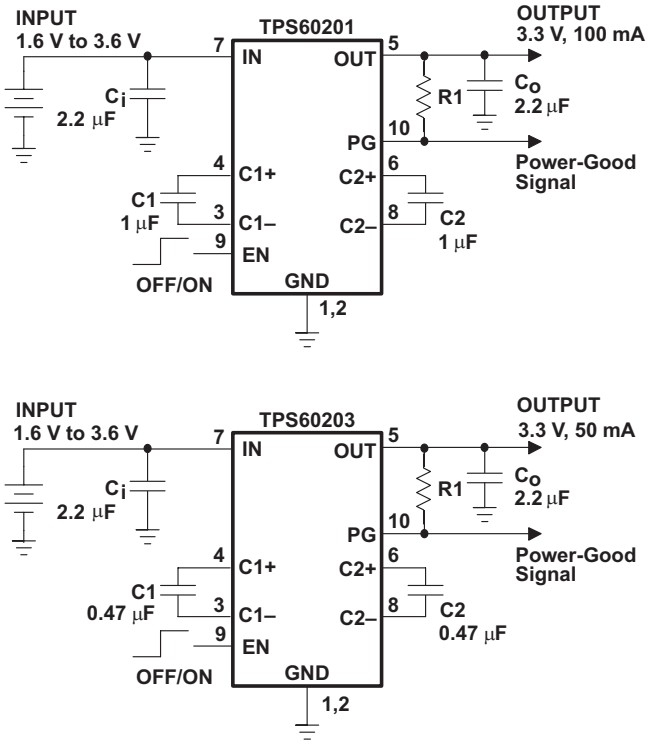


Figure 5. Typical Operating Circuit TPS60201 and TPS60203 With Power-Good-Detector

Typical Applications (continued)

9.2.1 Design Requirements

Table 4 lists the capacitor selections to operate the device in the recommended operating conditions.

Table 4. Recommended Capacitor Types

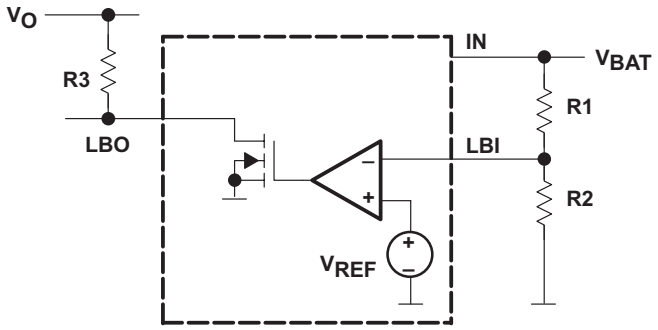
MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
Taiyo Yuden	EMK212BJ224MG	0805	0.22 µF	Ceramic
Taiyo Yuden	EMK212BJ474MG	0805	0.47 µF	Ceramic
Taiyo Yuden	LMK212BJ105KG	0805	1 µF	Ceramic
Taiyo Yuden	LMK212BJ225MG	0805	2.2 µF	Ceramic
Taiyo Yuden	EMK316BJ225KL	1206	2.2 µF	Ceramic
Taiyo Yuden	LMK316BJ475KL	1206	4.7 µF	Ceramic
Taiyo Yuden	JMK316BJ106ML	1206	10 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
AVX	1206ZC225KAT2A	1206	2.2 µF	Ceramic

9.2.2 Detailed Design Procedure

9.2.2.1 Low-Battery Detector (TPS60200 and TPS60202)

The low-battery comparator trips at 1.18 V ±4% when the voltage on pin LBI ramps down. The voltage V (TRIP) at which the low-battery warning is issued can be adjusted with a resistive divider as shown in Figure 4. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range. When choosing R1 and R2, be aware of the input leakage current into the LBI pin.

LBO is an open-drain output. TI recommends an external pullup resistor to OUT, or any other voltage rail in the appropriate range, in the 100-kΩ to 1-MΩ range. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected. The low-battery detector is disabled when the device is switched off.



$$V_{(TRIP)} = 1.18\ V\left(1 + \frac{R1}{R2}\right)$$

Figure 6. Programming of the Low-Battery Comparator Trip Voltage

A 100-nF ceramic capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO pin.

Formulas to calculate the resistive divider for low-battery detection, with V LBI = 1.13 V to 1.23 V and the sum of resistors R1 and R2 equal 1 MΩ.

$$R2 = 1\,M\Omega \times \frac{V_{LBI}}{V_{Bat}} \quad (1)$$

$$R1 = 1\,M\Omega - R2 \quad (2)$$

Formulas to calculate the minimum and maximum battery voltage.

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}} \quad (3)$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}} \quad (4)$$

Table 5. Recommended Values for the Resistive Divider From the E96 Series (±1%)

$V_{(IN)}$/V	R1/kΩ	R2/kΩ	$V_{TRIP(MIN)}$/V	$V_{TRIP(MAX)}$/V
1.6	267	750	1.524	1.677
1.7	301	681	1.62	1.785
1.8	340	649	1.71	1.887
1.9	374	619	1.799	1.988
2	402	576	1.903	2.106

9.2.3 Application Curves

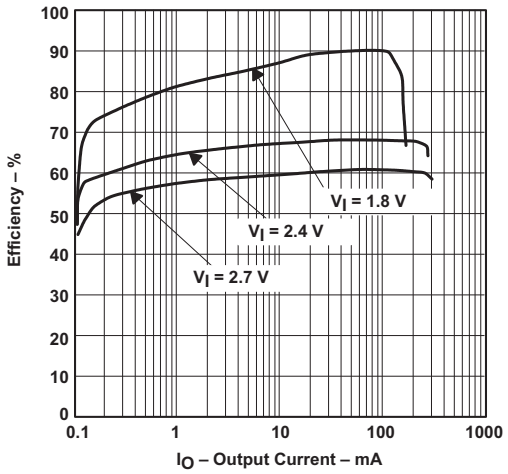


Figure 7. TPS60200 Efficiency vs Output Current

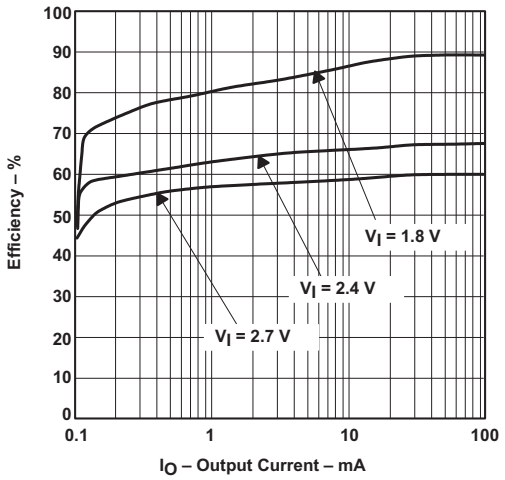


Figure 8. TPS60202 Efficiency vs Output Current

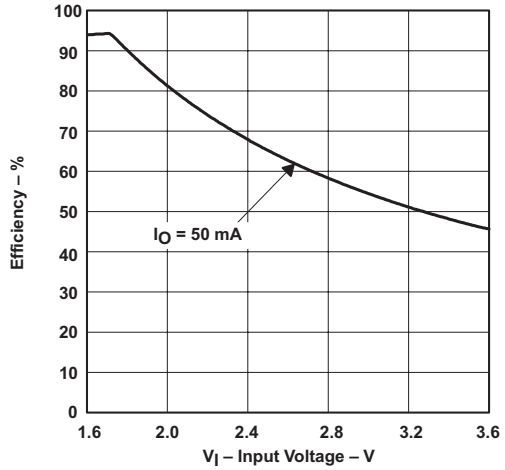


Figure 9. TPS60200 Efficiency vs Input Voltage

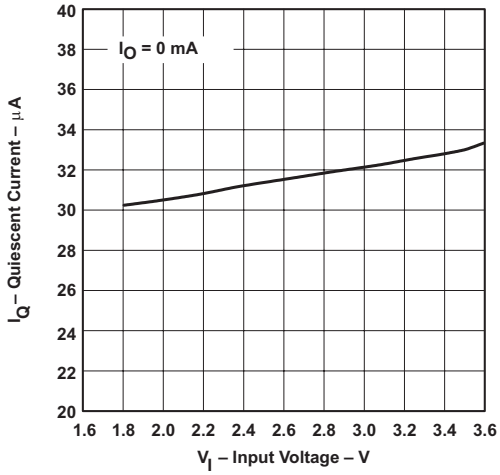


Figure 10. Quiescent Supply Current vs Input Voltage

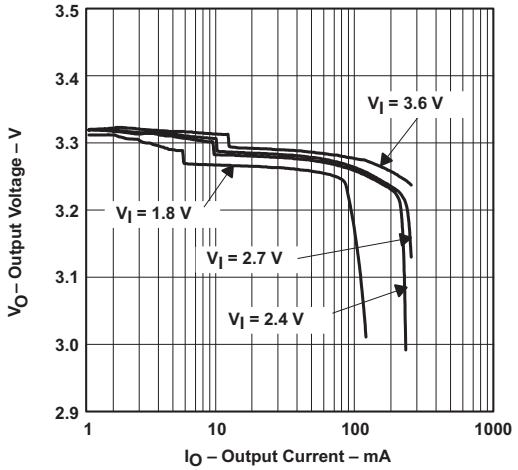


Figure 11. TPS60200 Output Voltage vs Output Current

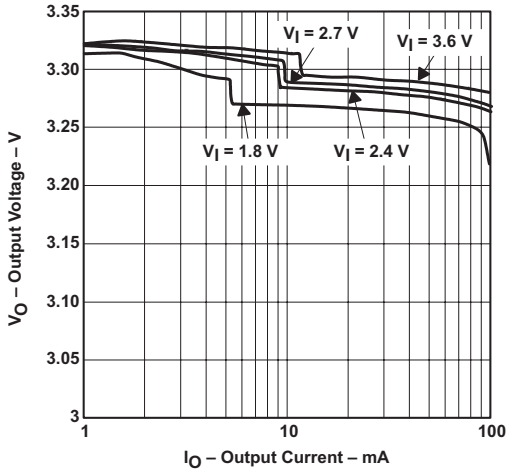


Figure 12. TPS60202 Output Voltage vs Output Current

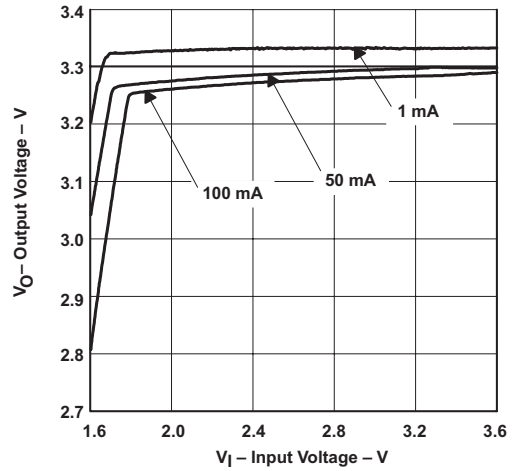


Figure 13. TPS60200 Output Voltage vs Input Voltage

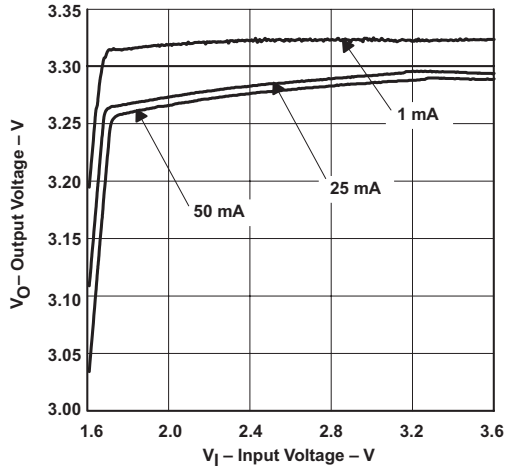


Figure 14. TPS60202 Output Voltage vs Input Voltage

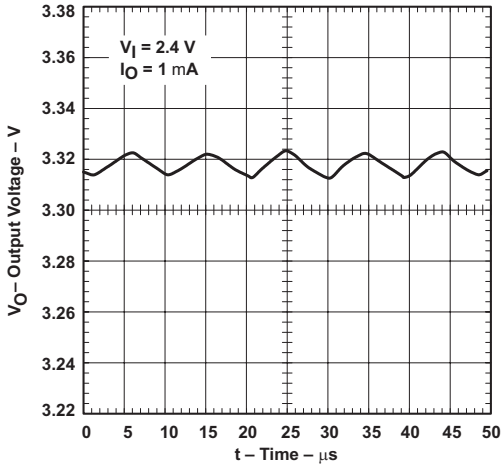


Figure 15. TPS60200 Output Voltage Ripple

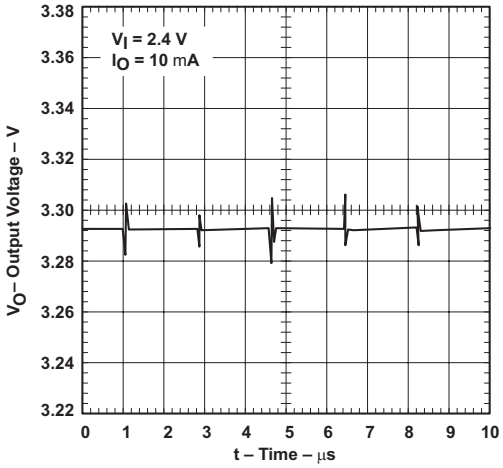


Figure 16. TPS60200 Output Voltage Ripple

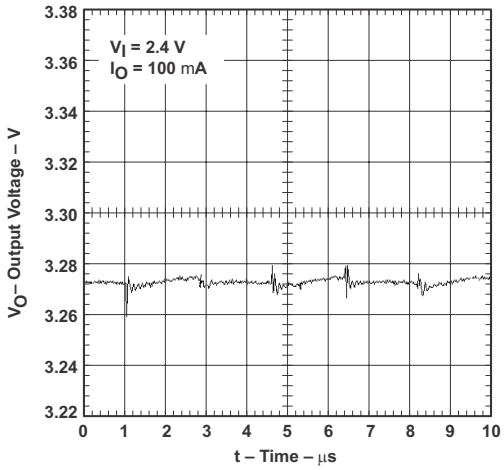


Figure 17. TPS60200 Output Voltage Ripple

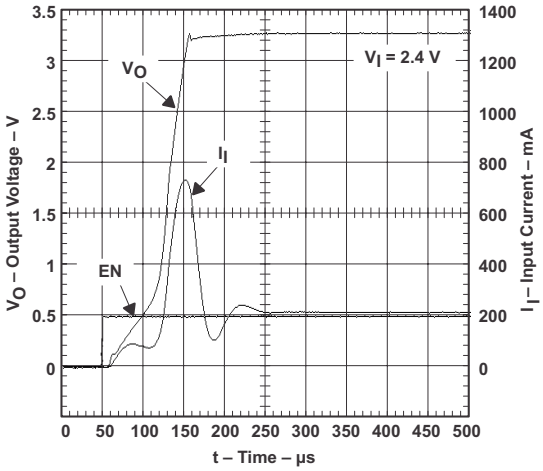


Figure 18. Start-Up Timing

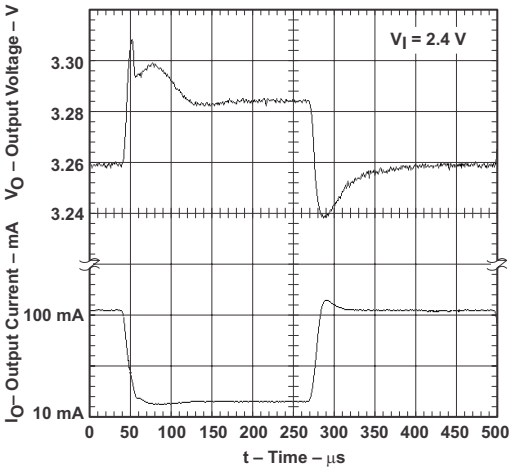


Figure 19. TPS60200 Load Transient Response

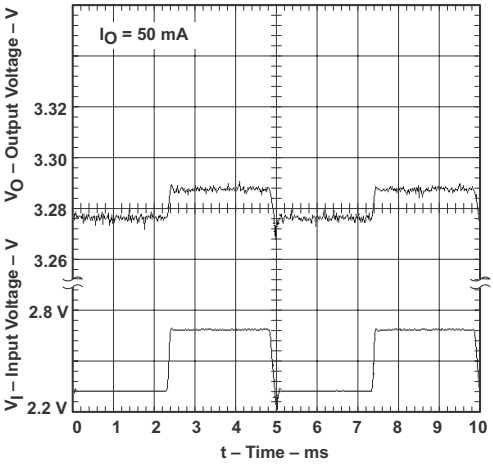


Figure 20. TPS60200 Line Transient Response

10 Power Supply Recommendations

The TPS6020x are designed to operate from a 1.6-V to 3.6-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be placed in close proximity to the device. A PCB layout proposal for a one-layer board is given in Figure 21.

An evaluation module for the TPS60200 is available and can be ordered under product code TPS60200EVM–145. The EVM uses the layout shown in Figure 21. All components including the pins are shown. The EVM is built so that it can be connected to a 14-pin dual inline socket; therefore, the space needed for the IC, the external parts, and 8 pins is 17.9 mm × 10.2 mm = 182.6 mm^2.

11.2 Layout Example

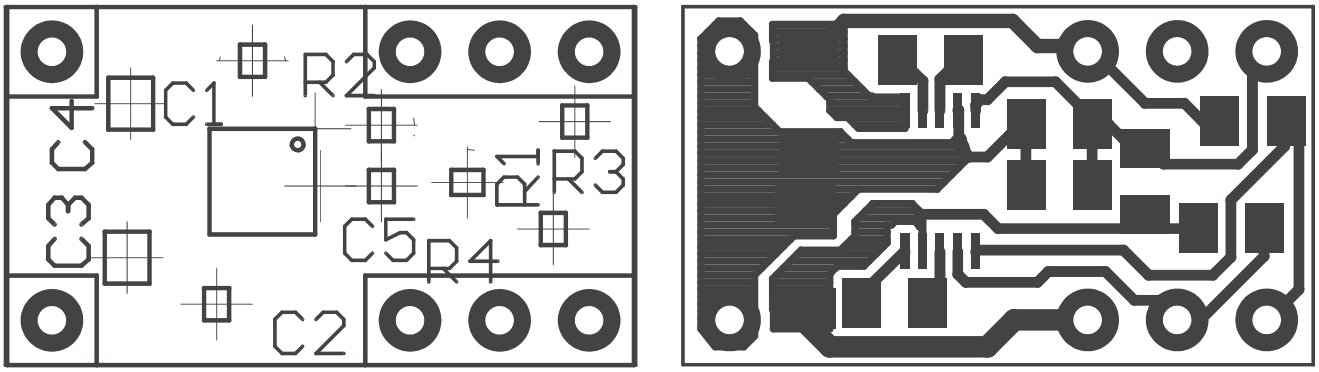


Figure 21. TPS6020x EVM Board Layout

Table 6. Component Identification

IC1	TPS60200
C1, C2	Flying capacitors
C3	Input capacitors
C4	Output capacitors
C5(1)	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO
R4	Pullup resistor for EN

(1) Capacitor C5 should be included if large line transients are expected. This capacitor suppresses toggling of the LBO due to these line changes.

11.3 Power Dissipation

The power dissipated in the TPS6020x devices depends mainly on input voltage and output current and is approximated with Equation 5.

$$P_{(DISS)} = I_O \times (2 \times V_I - V_O) \quad \text{for } I_{(Q)} << I_O \tag{5}$$

By observing Equation 5, it can be seen that the power dissipation is worst for highest input voltage V_I and highest output current I_O. For an input voltage of 3.6 V and an output current of 100 mA the calculated power dissipation $P_{(DISS)}$ is 390 mW. This is also the point where the charge pump operates with its lowest efficiency.

With the recommended maximum junction temperature of 125°C and an assumed maximum ambient operating temperature of 85°C, the maximum allowed thermal resistance junction to ambient of the system is calculated with Equation 6.

$$R_{\theta JA(max)} = \frac{T_{J(MAX)} - T_A}{P_{DISS(max)}} = \frac{125°C - 85°C}{390\ mW} = 102°C / W \tag{6}$$

P_{DISS} must be less than that allowed by the package rating. The thermal resistance junction to ambient of the used 10-pin MSOP is 294°C/W for an unsoldered package. The thermal resistance junction to ambient with the IC soldered to a printed circuit using a board layout as described in *Application Information*, the $R_{\theta JA}$ is typically 200°C/W, which is higher than the maximum value calculated above. However in a battery-powered application, both V_I and T_A will typically be lower than the worst-case ratings used in Equation 6, and power dissipation should not be a problem in most applications.

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS60200DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AEX	Samples
TPS60200DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AEX	Samples
TPS60201DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEY	Samples
TPS60202DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEZ	Samples
TPS60202DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AEZ	Samples
TPS60203DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFA	Samples
TPS60203DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AFA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

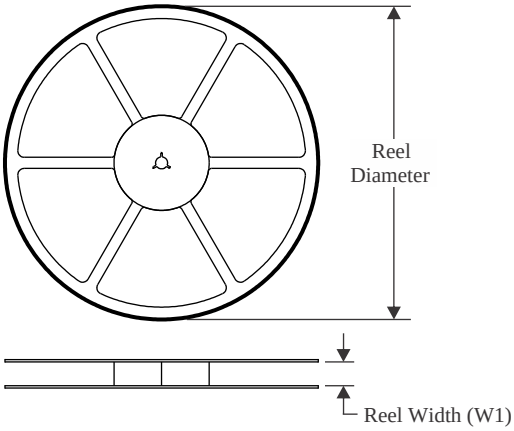
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

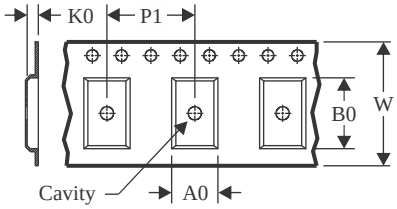
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

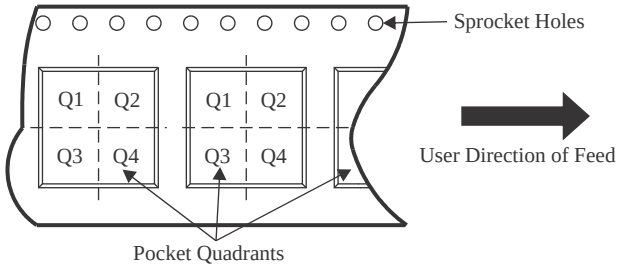


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

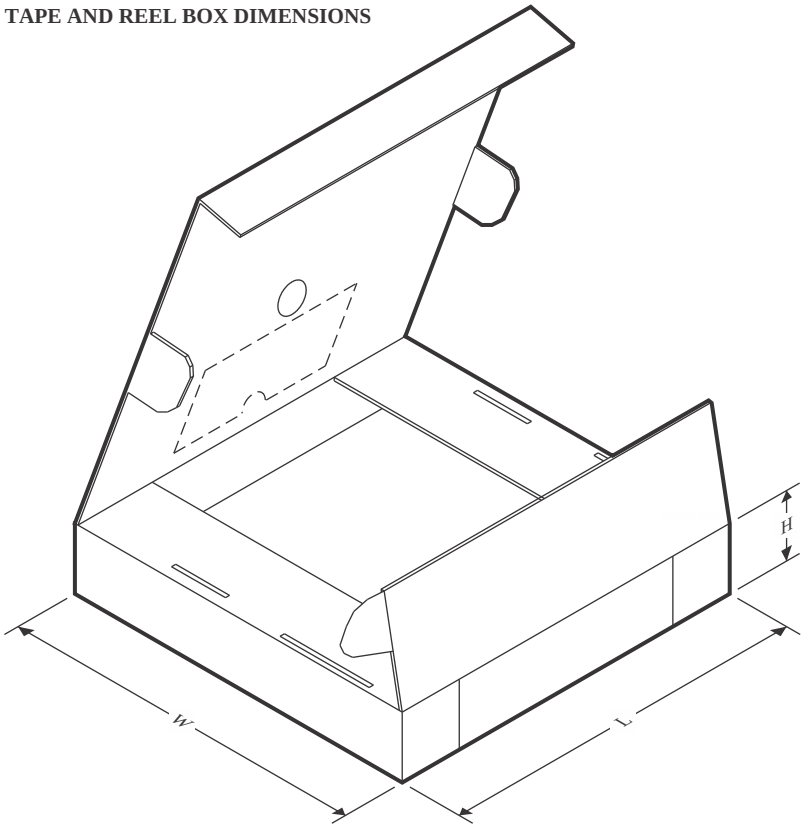
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60200DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60202DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60203DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

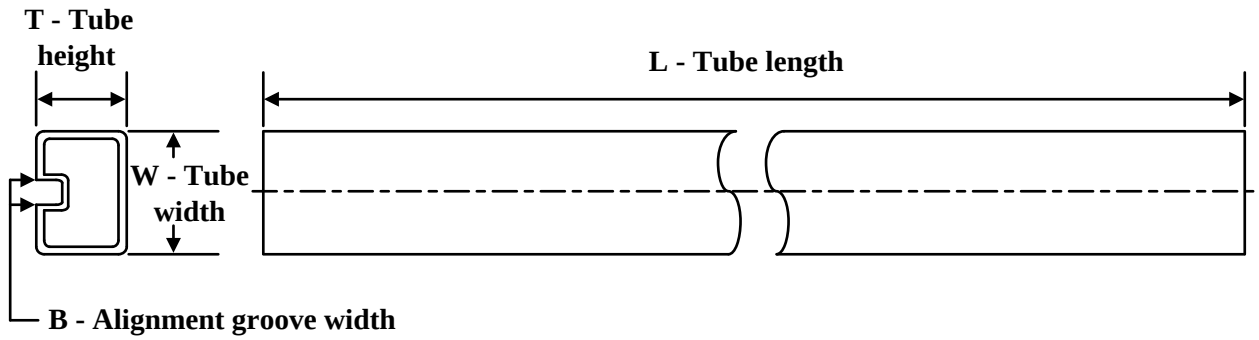
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60200DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60202DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60203DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

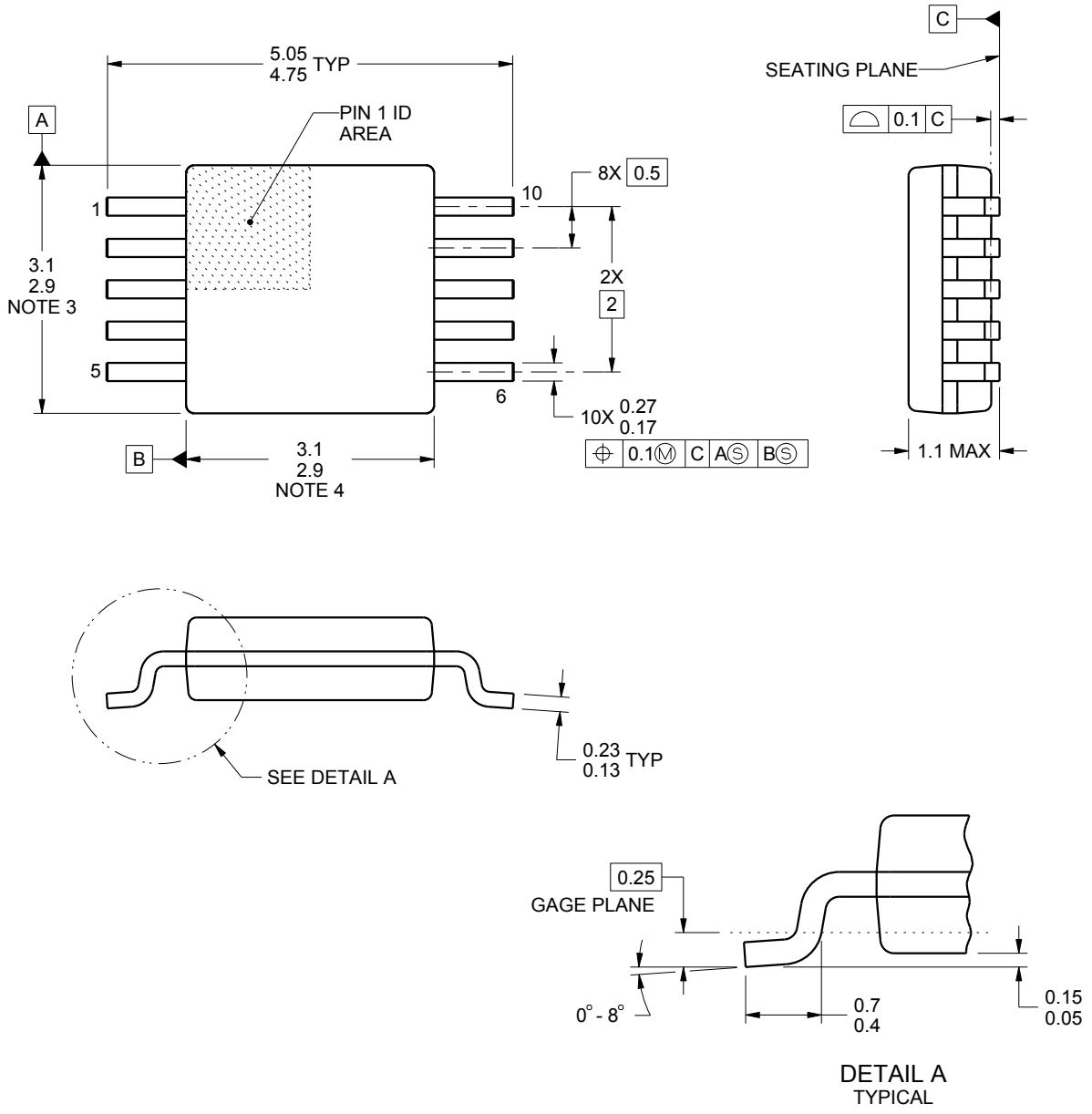
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60200DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60201DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60202DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60203DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

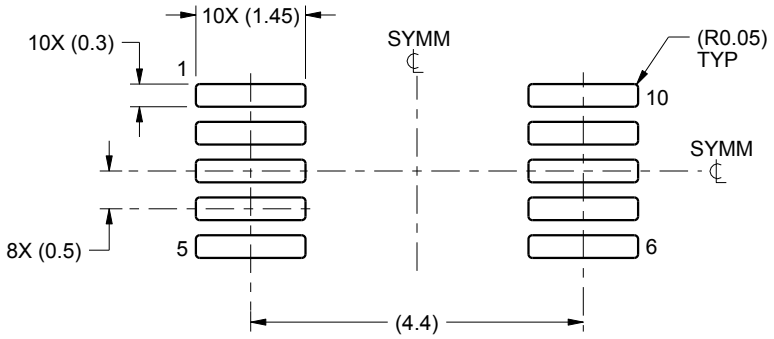
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

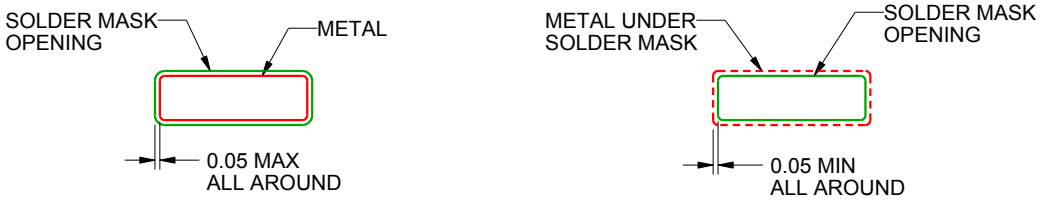


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

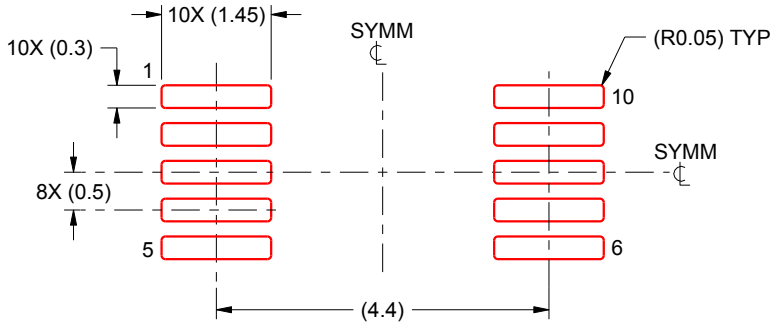


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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