TPS65131-Q1 Positive- and Negative-Output DC-DC Converter

1 Features

- Qualified for automotive applications
- AEC-Q100 test guidance with the following results:
  - Device temperature grade 2: –40°C to 105°C ambient operating temperature range
  - Electrical characteristics tested over –40°C to 125°C junction temperature range
  - Device HBM ESD classification level H1C
  - Device CDM ESD classification level C4B
- Dual adjustable output voltages up to 15V and down to –15V
- 2A typical switch-current limit for boost and inverter main switches
- High conversion efficiency
  - Up to 91% at positive output rail
  - Up to 85% at negative output rail
  - Power-save mode at low load
- Independent enable inputs for power-up and power-down Sequencing
- Control output for external PFET to support complete supply Disconnect When Shut Down
- 2.7V to 5.5V input-voltage range
- Minimum 1.25MHz fixed-frequency PWM operation
- Thermal shutdown
- Overvoltage protection on both outputs
- 0.2µA typical shutdown current
- Small 4mm × 4mm QFN-24 package (RGE) with wettable flanks

2 Applications

- Small-to-medium size OLED displays
- (TFT) LCD, CCD bias supply

3 Description

The TPS65131-Q1 device is dual-output dc-dc converter generating a positive output voltage up to 15V and a negative output voltage down to –15V with output currents of typically 200mA, depending on input-voltage to output-voltage ratio. With a total efficiency up to 85%, the device is ideal for portable battery-powered equipment. The input-voltage range of 2.7V to 5.5V allows, for example, 3.3V and 5V rails to power the TPS65131-Q1 device. The TPS65131-Q1 device comes in a QFN-24 package with thermal pad and wettable flanks. Requiring few and small external components, the overall solution size can be small.

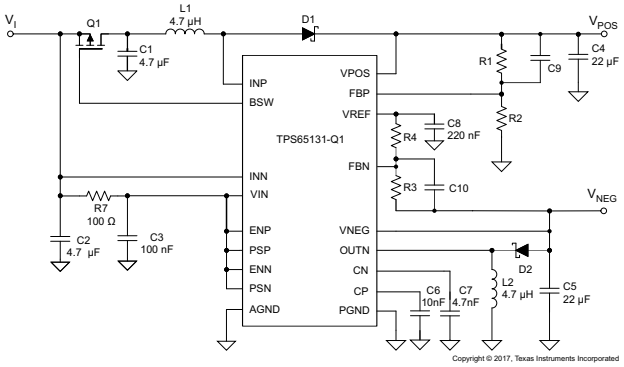
The converter operates with a fixed-frequency PWM control topology and, with power-save mode enabled, uses a pulse-skipping mode at light load currents. In operation, the typical overall device quiescent current is only 500µA. In shutdown, the device draws typically 0.2µA. Independent enable pins allow power-up and power-down sequencing for both outputs. The device has an internal current limit, overvoltage protection, and a thermal shutdown for highest reliability under fault conditions.

The TPS65131-Q1 device is qualified for automotive applications, according to AEC-Q100 temperature grade 2. The electrical characteristics are tested over –40°C to 125°C device junction temperature. This, combined with lowest shutdown currents, small solution size, package with thermal pad, plus good efficiency and protection features, targets automotive and industrial applications.

Package Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65131-Q1	VQFN (24)	4mm × 4mm

(1) For all available packages, see the orderable addendum.



Application Schematic

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4 Device Comparison

Table 4-1. Device Comparison Table

Part Number	Package	Wettable Flanks
TPS65131TRGERQ1	VQFN (24)	No
TPS65131WTRGERQ1	VQFN (24)	Yes

5 Pin Configuration and Functions

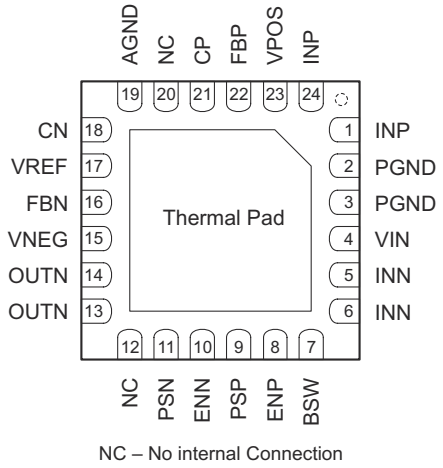


Figure 5-1. 24-pin VQFN Bottom View

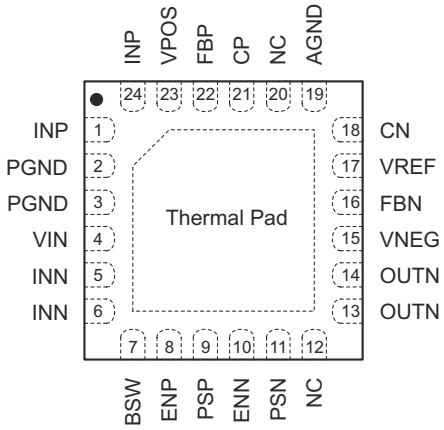


Figure 5-2. 24-pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	19	—	Analog ground pin
BSW	7	O	Gate-control pin for external battery switch. This pin goes low when ENP is set high.
CN	18	I/O	Compensation pin for inverting converter control
CP	21	I/O	Compensation pin for boost converter control
ENN	10	I	Enable pin for the negative-output voltage (0V: disabled, VIN: enabled)
ENP	8	I	Enable pin for the positive-output voltage (0V: disabled, VIN: enabled)
FBN	16	I	Feedback pin for the negative-output voltage divider
FBP	22	I	Feedback pin for the positive-output voltage divider
INN	5, 6	O	Inverting converter switch pin
INP	1, 24	O	Boost converter switch pin
NC(1)	12, 20	—	Not connected
OUTN	13, 14	I/O	Inverting converter switch output
PGND	2, 3	—	Power ground pin
PSN	11	I	Power-save mode enable for inverter stage (0V: disabled, VIN: enabled)
PSP	9	I	Power-save mode enable for boost converter stage (0V: disabled, VIN: enabled)
VIN	4	I	Control supply input
VNEG	15	I	Negative-output voltage-sense input
VPOS	23	I	Positive-output voltage-sense input
VREF	17	O	Reference output voltage. Bypass this pin with a 220nF capacitor to ground. Connect the lower resistor of the negative-output voltage divider to this pin.
Thermal pad			Thermal pad for thermal performance, connect to PGND

(1) NC - No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature, unless otherwise noted (1)

		VALUE		UNIT
		MIN	MAX	
	Input voltage range at pins VIN, INN (2)	–0.3	6	V
	Voltage at pin VPOS (2)	–0.3	17	V
	Voltage at pin VNEG (2)	–17	$V_{(VIN)}$ + 0.3	V
	Voltage at pins ENN, ENP, FBP, FBN, CN, CP, PSP, PSN, BSW (2)	–0.3	$V_{(VIN)}$ + 0.3	V
	Input voltage at pin INP (2)	–0.3	17	V
	Differential voltage between pins OUTN to INN (2)	–0.3	24	V
	Thermal pad(2)	–0.3	0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±1000	V
		Charged device model (CDM), per AEC Q100-011	±750	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature, unless otherwise noted

		MIN	MAX	UNIT
V_I , $V_{(VIN)}$, $V_{(INN)}$	Application input voltage range, input voltage range at VIN and INN pins	2.7	5.5	V
V_{POS}	Adjustable output voltage range for the boost converter	V_I + 0.5	15	V
V_{NEG}	Adjustable output voltage range for the inverting converter	–15	–2	V
$V_{(ENN)}$, $V_{(ENP)}$	Enable signals voltage	0	5.5	V
$V_{(PSN)}$, $V_{(PSP)}$	Power-save mode enable signals voltage	0	5.5	V
T_A	Operating free-air temperature range(1)	–40	105	°C
T_J	Operating junction temperature range	–40	125	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may require derating. See *Thermal Information* for details.

6.4 Thermal Information

THERMAL METRIC		TPS65131-Q1 RGE PACKAGE 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	36.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

6.5 Electrical Characteristics

This specification applies over the full recommended input voltage range V_I = 2.7V to 5.5V and over the temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6V and T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE ($V_{(VPOS)}$, $V_{(VNEG)}$)							
V_{ref}	Reference voltage		I_{ref} = 10µA	1.2	1.213	1.225	V
$I_{(FBP)}$	Positive feedback input bias current		$V_{(FBP)} = V_{ref}$		50		nA
$I_{(FBN)}$	Negative feedback input bias current		$V_{(FBN)} = 0.1V_{ref}$		50		nA
$V_{(FBP)}$	Positive feedback regulation voltage			1.189	1.213	1.237	V
$V_{(FBN)}$	Negative feedback regulation voltage			–0.024	0	0.024	V
	Total output dc accuracy				3%		
$r_{DS(on)(N)}$	Inverter switch on-resistance		$V_{(VIN)}$ = 3.6V		440	620	mΩ
			$V_{(VIN)}$ = 5V		330	530	
$I_{(L\ IM-N)}$	Inverter switch current limit		$V_{(VIN)}$ = 3.6V	1700	1950	2200	mA
$r_{DS(on)(P)}$	Boost switch on-resistance		$V_{(POS)}$ = 5V		230	390	mΩ
			$V_{(POS)}$ = 10V		170	230	
$I_{(LIM-P)}$	Boost switch current limit		$V_{(VIN)}$ = 3.6V, $V_{(POS)}$ = 8V	1700	1950	2250	mA
CONTROL STAGE							
V_{IH}	High-level input voltage, ENP, ENN, PSP, PSN			1.4			V
V_{IL}	Low-level input voltage, ENP, ENN, PSP, PSN					0.4	V
	Input current, ENP, ENN, PSP, PSN		ENP, ENN, PSP, PSN connected to GND or VIN		0.01	0.1	µA
$R_{(BSW)}$	Output resistance				27		kΩ
I_Q	Quiescent current	VIN	$V_{(VIN)}$ = 3.6V, $I_{(POS)}$ = $I_{(NEG)}$ = 0, ENP = ENN = PSP = PSN = $V_{(VIN)}$, $V_{(POS)}$ = 8V, $V_{(NEG)}$ = –5V		300	500	µA
		VPOS			100	120	
		VNEG			100	120	
I_{SD}	Shutdown supply current		ENN = ENP = LOW, T_A = –40°C to 85°C		0.2	1.5	µA
$V_{(UVLO)}$	Undervoltage lockout threshold			2.1	2.35	2.7	V
$T_{(TS)}$	Thermal shutdown				150		°C
$T_{(TS-HYS)}$	Thermal shutdown hysteresis		Junction temperature decreasing		5		°C

6.6 Switching Characteristics

The specification applies over the full recommended input voltage range V_I = 2.7V to 5.5V and over the temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY						
f	Oscillator frequency		1150	1380	1500	kHz
DUTY CYCLE						
$D_{(MAX-P)}$	Maximum-duty-cycle, boost converter			87.5%		
$D_{(MAX-N)}$	Maximum-duty-cycle, inverting converter			87.5%		
$D_{(MIN-P)}$	Minimum-duty-cycle, boost converter			12.5%		
$D_{(MIN-N)}$	Minimum-duty-cycle, inverting converter			12.5%		

6.7 Typical Characteristics

At 25°C, unless otherwise noted.

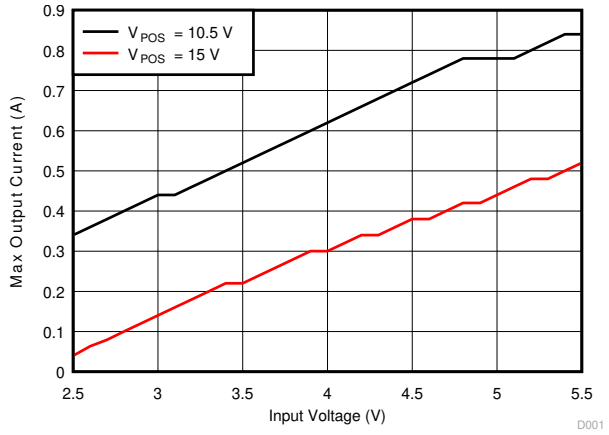


Figure 6-1. Boost Converter (V_{POS}) Maximum Output Current vs Input Voltage

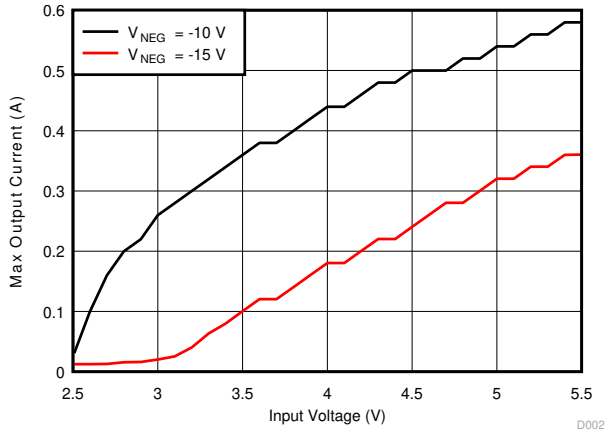


Figure 6-2. Inverting Converter (V_{POS}) Output Current vs Input Voltage

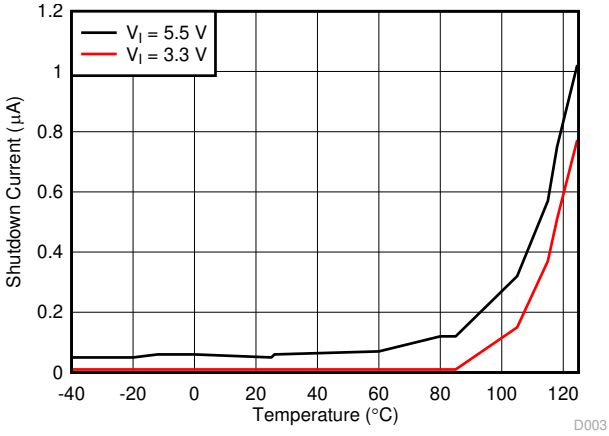
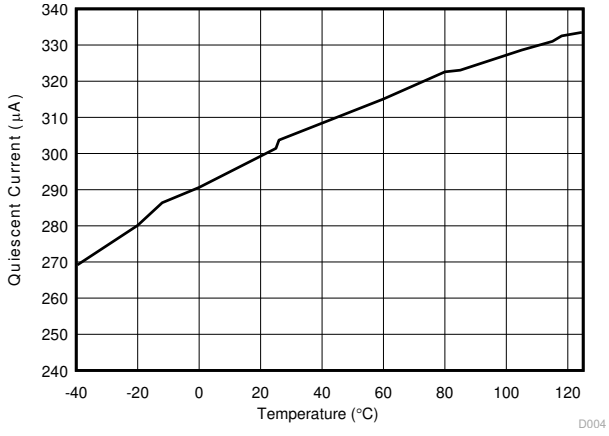


Figure 6-3. Shutdown Current (Into VIN and INN) Over Input Voltage



V_I = 3.6V

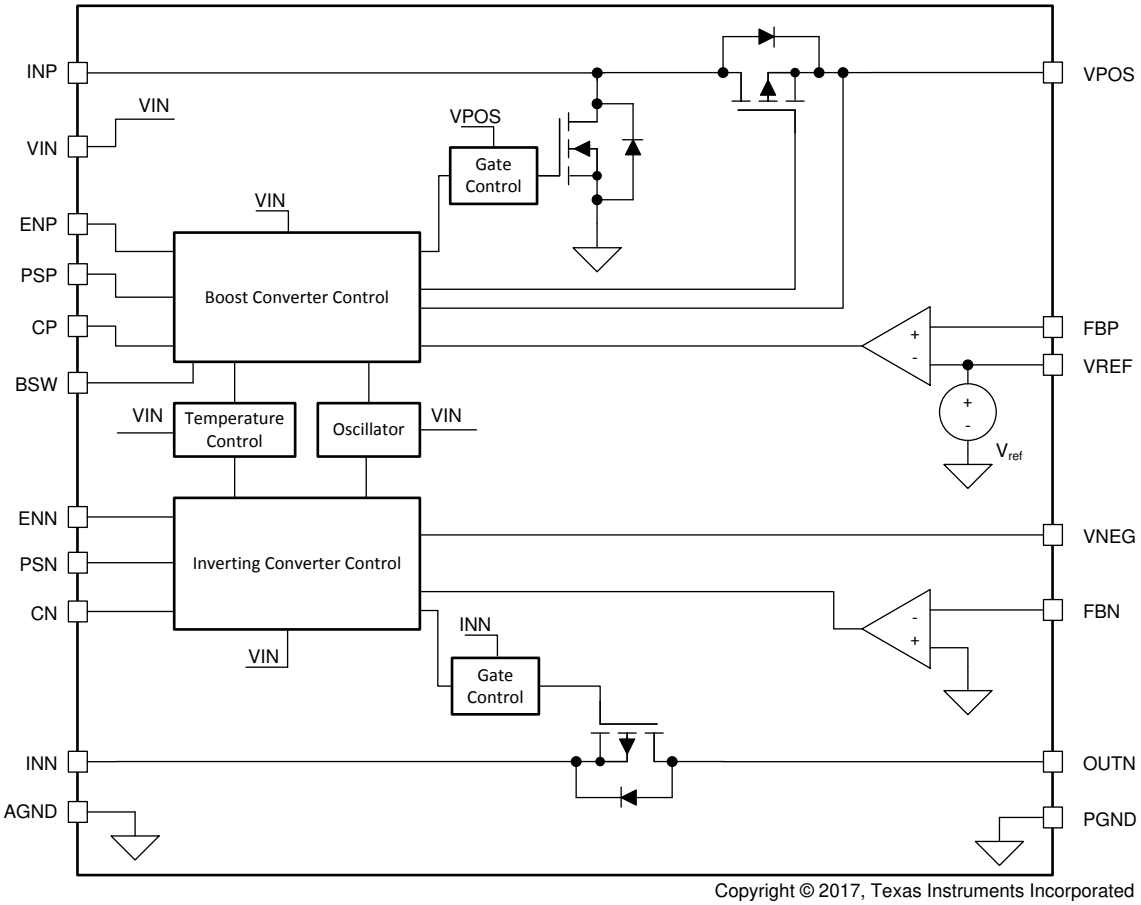
Figure 6-4. Quiescent Current (Into VIN and INN) Over Input Voltage

7 Detailed Description

7.1 Overview

The TPS65131-Q1 is a dual-output dc-dc converter that generates two adjustable output voltages. One output voltage is positive (boost converter), the other is negative (inverting converter). The positive output is adjustable up to 15V, the negative output is adjustable down to –15V. The device operates with an input voltage range of 2.7V to 5.5V. Both converters (positive and negative output) work independently of each other. They share a common clock and a common voltage reference. A fixed-frequency, pulse-width-modulated (PWM) regulator controls both outputs separately. In general, each converter operates in continuous-conduction mode (CCM). To improve efficiency at light loads, the converters can operate in discontinuous-conduction mode (DCM). When the power-save mode is enabled, the converters automatically transition between CCM and DCM operation: As the load current decreases, the converter enters DCM mode. Power-save mode is individually configurable for both outputs. The transition as a function of the load current works independently for each converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Conversion

Both converters operate in a fixed-frequency, PWM control scheme. The on-time of the internal switches varies depending on the input-to-output voltage ratio and the load. During the on-time, the inductors connected to the converters charge with current. In the remaining time, the off-time with a time period set by the fixed operating frequency, the inductors discharge into the output capacitors through the rectifier diodes. Usually at higher loads, the inductor currents are continuous. At lighter loads, the boost converter uses an additional internal switch to allow current to flow back to the input. This avoids inductor current becoming discontinuous in the boost converter. At the inverting converter, during light loads, the inductor current can become discontinuous. In this case, the control circuit of the inverting controller output automatically takes care of these changing conditions to operate always with an optimum control setup.

7.3.2 Control

The controller circuits of both converters employ a fixed-frequency, multiple-feedforward controller topology. These circuits monitor input voltage, output voltage, and voltage drop across the switches. Changes in the operating conditions of the converters directly affect the duty cycle and must not take the indirect and slow way through the output voltage-control loops. A self-learning control corrects measurement errors in this feedforward system. An external capacitor damps the output to avoid output-voltage steps due to output changes of this self-learning control system.

The voltage loops, determined by the error amplifiers, must only handle small signal errors. The error amplifiers feature internal compensation. Their inputs are the feedback voltages on the FBP and FBN pins. The device uses a comparison of these voltages with the internal reference voltage to generate an accurate and stable output voltage.

7.3.3 Output Rails Enable or Disable

Both converters can be enabled or disabled individually. Applying a logic HIGH signal at the enable pins (ENP for the boost converter, ENN for the inverting converter) enables the corresponding output. After enabling, internal circuitry, necessary to operate the specific converter, then turns on, followed by the *Soft Start* .

Applying a low signal at the enable ENP or ENN pin shuts down the corresponding converter. When both enable pins are low, the device enters shutdown mode, where all internal circuitry turns off. The device now consumes shutdown current flowing into the VIN pin. The output loads of the converters can be disconnected from the input, see *Load Disconnect* .

7.3.4 Load Disconnect

The device supports completely disconnecting the load when the converters are disabled. For the inverting converter, the device turns off the internal PMOS switch. If the inverting converter is turned off, no dc current path remains which could discharge the battery or supply.

This is different for the boost converter. The external rectifying diode, together with the boost inductor, form a dc current path which could discharge the battery or supply if any load connects to the output. The device has no internal switch to prevent current from flowing. For this reason, the device offers a PMOS gate control output (BSW) to enable and disable a PMOS switch in this dc current path, ideally directly between the boost inductor and battery. To be able to fully disconnect the battery, the forward direction of the parasitic backgate diode of this switch must point to the battery or supply. The external PMOS switch, which connects to BSW, turns on when the boost converter is enabled and turns off when the boost converter is disabled.

7.3.5 Soft Start

Both converters have implemented soft-start functions. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in typically 1ms. The device includes this function to limit the input current during start-up to avoid high peak input currents, which could interfere with other systems connected to the same battery or supply.

If the application includes the *Load Disconnect* PMOS switch, a current flows from the input to the output of the boost converter at the moment the PMOS switch becomes conducting.

7.3.6 Overvoltage Protection

Both built-in converters (boost and inverter) have implemented individual overvoltage protection. If the feedback voltage under normal operation exceeds the nominal value by typically 5%, the corresponding converter shuts down immediately to protect any connected circuitry from possible damage.

7.3.7 Undervoltage Lockout

An undervoltage lockout prevents the device from starting up and operating if the supply voltage at the VIN pin is lower than the undervoltage lockout threshold. For this case, the device automatically shuts down both converters when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown using EN inputs. The device includes the undervoltage lockout function to prevent device malfunction.

7.3.8 Overtemperature Shutdown

The device automatically shuts down both converters if the implemented internal temperature sensor detects a chip temperature above the thermal shutdown temperature. It automatically starts operating again when the chip temperature falls below this threshold plus hysteresis threshold. The built-in hysteresis avoids undefined operation caused by ringing from shutdown and prevents operating at a temperature close to the overtemperature shutdown threshold.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The power-save mode can improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage falls below an device internally set threshold voltage. The converter ramps up the output voltage with one or several operating pulses and goes again into power-save mode once the inductor current becomes discontinuous.

The PSN and PSP logic level selects between power-save mode and continuous-conduction mode. If the specific pins (PSP for the boost converter, PSN for the inverting converter) are HIGH, the power-save mode for the corresponding converter operates at light loads. Similary, a LOW on the PSP pin or PSN pin disables the power-save mode for the corresponding converter.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS656131-Q1 boost converter output voltage, V_{POS}, and the inverting converter output voltage, V_{NEG}, require external components to set the required output voltages. The valid output voltage ranges are as shown in *Recommended Operating Conditions*). The passages below show typical application examples with different output voltage settings and guidance for external component choices.

8.2 Typical Applications

8.2.1 TPS65131-Q1 With V_{POS} = 10.5V, V_{NEG} = –10V

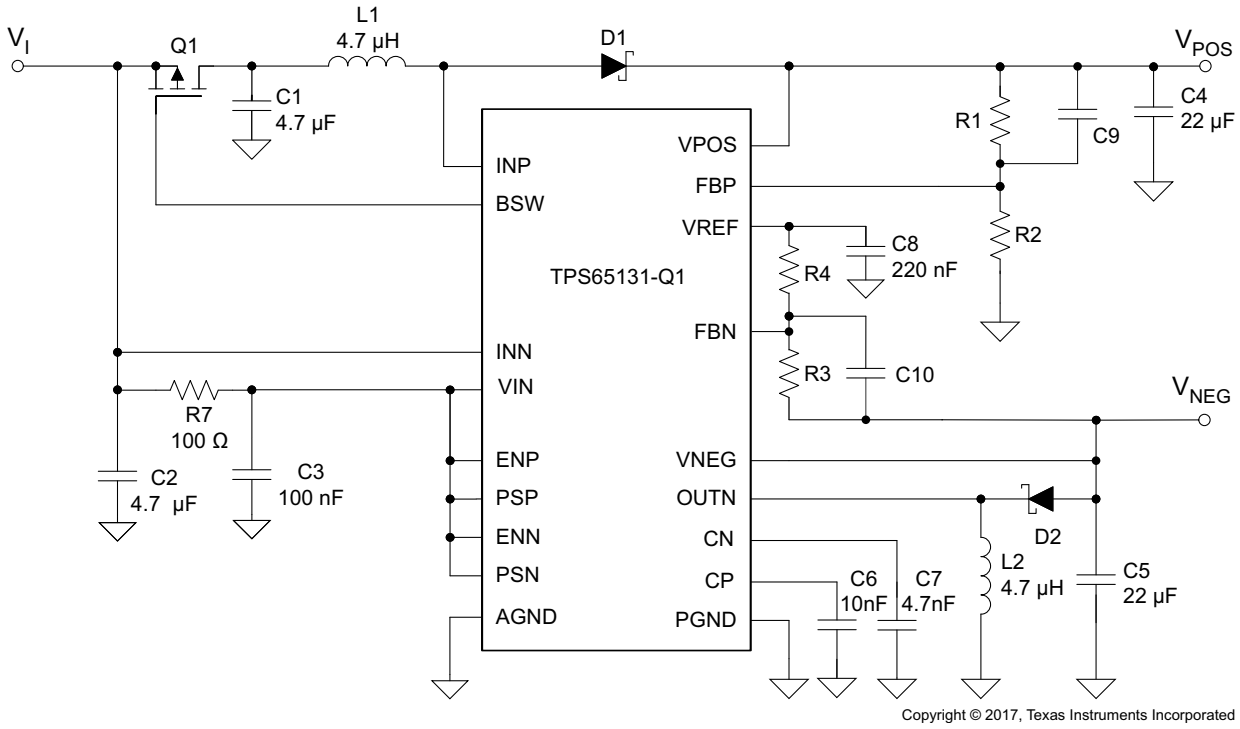


Figure 8-1. Typical Application Schematic With V_{POS} = 10.5V, V_{NEG} = –10V

8.2.2 Design Requirements

The design procedure for this setup is similar to the first example, see *Detailed Design Procedure* . Change the feedback dividers to set the output voltage, see *Programming the Output Voltage* . Further, choose the feed-forward capacitors according to *Feedforward Capacitors* . Table 8-1 shows the components being changed. See Figure 8-1.

Table 8-1. Design Parameters

Design Parameter	Example Value	
Input voltage range	2.7V to 5.5V	
Boost converter output voltage, V_{POS}	R1 = 1MΩ R2 = 130kΩ C9 = 6.8pF	10.5V
Inverting converter output voltage, V_{NEG}	R3 = 1MΩ R4 = 121.2kΩ C10 = 7.5pF	–10V

In this example, the converters are operated with power-save mode both enabled and disabled (see *Power-Save Mode*).

8.2.3 Detailed Design Procedure

8.2.3.1 Programming the Output Voltage

8.2.3.1.1 Boost Converter

An external resistor divider adjusts the output voltage of the TPS65131-Q1 boost converter stage. Connect this divider to the FBP pin. The typical value of the voltage at the FBP pin is the reference voltage, which is 1.213V. The maximum recommended output voltage at the boost converter is 15V. To achieve appropriate accuracy, the current through the feedback divider should be about 100 times higher than the current into the FBP pin. Typical current into the FBP pin is 0.05µA, and the voltage across R2 is 1.213V. Based on those values, the recommended value for R2 should be lower than 200kΩ in order to set the divider current at 5µA or higher.

Calculate the value of resistor R1, as a function of the needed output voltage (V_{POS}), with Equation 1:

$$R1 = R2 \times \left(\frac{V_{POS}}{V_{ref}} - 1 \right) \tag{1}$$

In this example, with R2 = 130kΩ, choose R1 = 1MΩ to set V_{POS} = 10.5V.

8.2.3.1.2 Inverting Converter

An external resistor divider adjusts the output voltage of the TPS65131-Q1 inverting converter stage. Connect this divider to the FBN pin. Unlike the feedback divider at the boost converter, the reference point of the feedback divider is not GND, but V_{ref}. So the typical value of the voltage at the FBN pin is 0V. The minimum recommended output voltage at the inverting converter is –15V. Feedback divider current considerations are similar to the considerations for the boost converter. For the same reasons, the feedback divider current should be in the range of 5µA or higher. The voltage across R4 is 1.213V. Based on those values, the recommended value for R4 should be lower than 200kΩ in order to set the divider current at the required value.

Calculate the value of resistor R3, as a function of the needed output voltage (V_{NEG}), with Equation 2:

$$R3 = -R4 \times \left(\frac{V_{NEG}}{V_{ref}} \right) \tag{2}$$

In this example, with R4 = 121.2kΩ, choose R3 = 1MΩ to set V_{NEG} = –10V.

8.2.3.1.3 Inductor Selection

An inductive converter normally requires two main passive components to store energy during the conversion. Therefore, each converter requires an inductor and a storage capacitor. To select the right inductor, it is recommended to keep the possible peak inductor current below the current-limit threshold of the power switch in the chosen configuration. For example, the current-limit threshold of the switch for the boost converter and for the inverting converters is nominally 1950mA. The highest peak current through the switches and the inductor depends on the output load (I_{POS}, I_{NEG}), the input voltage (V_I), and the output voltages (V_{POS}, V_{NEG}). Use Equation 3 to estimate the peak inductor current in the boost converter, $I_{(L-P)}$. Equation 4 shows the corresponding formula for the inverting converter, $I_{(L-N)}$.

$$I_{(L-P)} = \frac{V_{POS}}{V_I \times 0.64} \times I_{POS} \tag{3}$$

$$I_{(L-N)} = \frac{V_I - V_{NEG}}{V_I \times 0.64} \times I_{NEG} \tag{4}$$

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, output voltage regulation gets slower, causing higher voltage changes during fast load changes. In addition, a larger inductor usually increases the total system cost. Keep those parameters in mind and calculate the possible inductor value with Equation 5 for the boost converter (L1) and Equation 6 for the inverting converter (L2).

$$L1 = \frac{V_I \times (V_{POS} - V_I)}{\Delta I_{(L-P)} \times f \times V_{POS}} \tag{5}$$

$$L2 = \frac{V_I \times V_{NEG}}{\Delta I_{(L-N)} \times f \times (V_{NEG} - V_I)} \tag{6}$$

The parameter f is the switching frequency. For the boost converter, $\Delta I_{(L-P)}$ is the ripple current in the inductor, that is, 20% of $I_{(L-P)}$. Accordingly, for the inverting converter, $\Delta I_{(L-N)}$ is the ripple current in the inductor, that is, 20% of $I_{(L-N)}$. V_I is the input voltage, which is 3.3V in this example. So, the calculated inductance value for the boost inductor is 5.1µH and for the inverting converter inductor is 5.1µH. With these calculated values and the calculated currents, it is possible to choose a suitable inductor.

In typical applications, the recommendation is to choose a 4.7µH inductor. The device is optimized to work with inductance values between 3.3µH and 6.8µH. Nevertheless, operation with higher inductance values may be possible in some applications. Perform detailed stability analysis in this case. Be aware of the possibility that load transients and losses in the circuit can lead to higher currents than estimated in Equation 3 and Equation 4. Also, the losses caused by magnetic hysteresis and conductor resistance are a major parameter for total circuit efficiency.

The following table shows inductors from different suppliers used with the TPS65131-Q1 converter:

Table 8-2. List of Inductors

VENDOR(1)	INDUCTOR SERIES
EPCOS	B8246284-G4
Wurth Elektronik	7447789XXX
	744031XXX
TDK	VLF3010
	VLF4012
Cooper Electronics Technologies	SD12

(1) See *Section 9.3*

8.2.3.2 Capacitor Selection

8.2.3.2.1 Input Capacitor

As a recommendation, choose an input capacitors of at least 4.7µF for the input of the boost converter (INP) and accordingly for the input of the inverting converter (INN). This improves transient behavior of the regulators and EMI behavior of the total power-supply circuit. Choose a ceramic capacitor or a tantalum capacitor. For the use of a tantalum capcitor, an additonal, smaller ceramic capacitor (100nF) in parallel is required. Place the input capacitor(s) close to the input pins.

8.2.3.2.2 Output Capacitors

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. Two parameters, which are the capacitance and the equivalent series resitance (ESR), affect this ripple. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero. Use Equation 7 for the boost-converter output capacitor (C4min) and Equation 8 for the inverting-converter output capacitor (C5min).

$$C4\,min = \frac{I_{POS} \times (V_{POS} - V_I)}{f \times \Delta V_{POS} \times V_{POS}} \tag{7}$$

$$C5\,min = \frac{I_{NEG} \times V_{NEG}}{f \times \Delta V_{NEG} \times (V_{NEG} - V_I)} \tag{8}$$

The parameter f is the switching frequency. ΔV_{POS} and ΔV_{NEG} are the maximum allowed ripple voltages for each converter.

Choosing a ripple voltage in the range of 10mV requires a minimum capacitance of 12µF. The total ripple is larger due to the ESR of the output capacitor. Use Equation 9 for the boost converter and Equation 10 for the inverting converter to calculate this additional ripple component.

$$\Delta V_{(ESR-P)} = I_{POS} \times R_{(ESR-C4)} \tag{9}$$

$$\Delta V_{(ESR-N)} = I_{NEG} \times R_{(ESR-C5)} \tag{10}$$

In this example, an additional ripple of 2mV is the result of using a typical ceramic capacitor with an ESR in the 10mΩ range. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 10mV.

Load transients can create additional ripple. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current increases by the control loop which sets a higher on-time (duty cycle) of the main switch. The higher duty cycle results in longer inductor charging periods. The inductance itself also limits the rate of increase of the inductor current. When the load current decreases rapidly, the output capacitor must store the excess energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. The recommendation is to use higher capacitance values, as the foregoing calculations show.

8.2.3.3 Rectifier Diode Selection

Both converters (the boost and inverting converter) require rectifier diodes, D1 and D2. As a recommendation, to reduce losses, use Schottky diodes. The forward current rating needed is equal to the maximum output current. Consider that the maximum currents, I_{POS}max and I_{NEG}max, might differ for V_{POS} and V_{NEG} when choosing the diodes.

8.2.3.4 External P-MOSFET Selection

During shutdown, when connected to a power supply, a path from the power supply to the positive output conducts through the inductor and an external diode. Optionally, in oder to fully disconnect the positive output V_{POS} during shutdown, add an external p-MOSFET (Q1). The BSW pin controls the gate of the p-MOSFET. When choosing a proper p-MOSFET, the V_{GS} and V_{GD} voltage ratings must cover the input voltage range, the drain current rating must not be lower than the maximum input current flowing into the application, and conditions of the p-MOSFET operating area must fit.

If there is no intention to use an external p-MOSFET, leave the BSW pin floating.

8.2.3.5 Stabilizing the Control Loop

8.2.3.5.1 Feedforward Capacitors

As a recommendation, to speed up the control loop, place feedforward capacitors in the feedback divider, parallel to R1 (boost converter) and R3 (inverting converter). Equation 11 shows how to calculate the appropriate value for the boost converter, and Equation 12 for the inverting converter.

$$C9 = \frac{6.8\ \mu s}{R1} \tag{11}$$

$$C10 = \frac{7.5\ \mu s}{R3} \tag{12}$$

In this application example, C9 = 6.8pF and C10 = 7.5pF match the choices of R1 and R3.

To avoid coupling noise into the control loop from the feedforward capacitors, it is possible to place a series resistor to limit the bandwidth of the feedforward effect. Any value between 10kΩ and 100kΩ is suitable. The higher the resistance, the lower the noise coupled into the control loop system.

8.2.3.5.2 Compensation Capacitors

The device features completely internally compensated control loops for both converters. The internal feedforward system has built-in error correction which requires external capacitors. As a recommendation, use a 10nF capacitor at the CP pin of the boost converter and a 4.7nF capacitor at the CN pin of the inverting converter.

8.2.4 Analog Supply Input Filter

To ensure a noise free voltage supply of the IC, it is recommended to add an RC or LC filter between IIN and VIN pins.

8.2.4.1 RC-Filter

For most applications an RC filter can be used with a resistance value of 100Ω minimum and capacitor value of 0.1µF as in the application example Figure 8-1.

8.2.4.2 LC-Filter

For applications where input voltages V_I with a fast rising edge (slew rate ≥ 275mV/µs) are expected, it is recommended to replace the resistor R7 with a ferrite bead to minimize the delay between the signals on IIN and VIN. A ferrite bead with the lowest possible DCR and a proper current rating should be selected - BLM18KG101TN1 for example. A conservative approach for the current rating specification is to set it at 1.5 times or twice the maximum input current.

Table 8-3. List of Ferrite Beads

VENDOR	FERRITE BEAD SERIES
Murata	BLMxKG

8.2.5 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heatsinks and convection surfaces, and the presence of heat-generating components affect the power-dissipation limits of a given component.

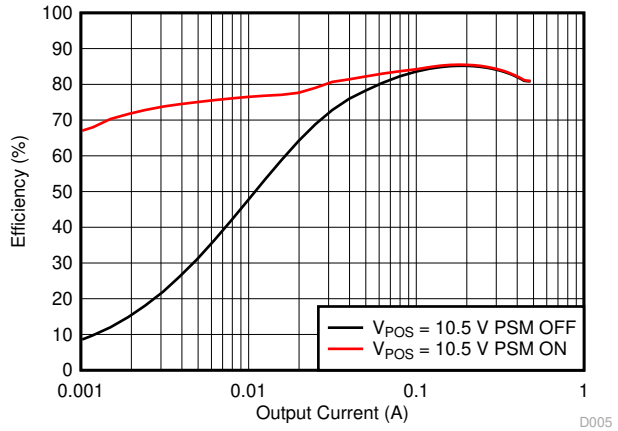
Three basic approaches for enhancing thermal performance follow.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow to the system

The recommended device junction temperature range, T_J, is –40°C to 125°C. The thermal resistance of the 24-pin QFN, 4–mm × 4–mm package (RGE) is $R_{\theta JA}$ = 34.1°C/W. The recommended operating ambient temperature range for the device is T_A = –40°C to 105°C. Use Equation 13 to calculate the maximum power dissipation, $P_D$max, as a function of T_A. In this equation, use T_J = 125°C to operate the device within the recommended temperature range, use $T_J = T_{(TS)}$ to determine the absolute maximum threshold when the device might go into thermal shutdown. If the maximum ambient temperature of the application is lower, more heat dissipation is possible.

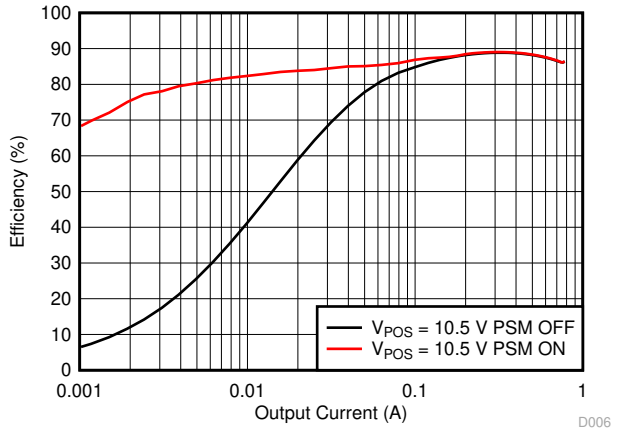
$$P_D\,\text{max} = \frac{T_J - T_A}{R_{\theta JA}} \tag{13}$$

8.2.6 Application Curves



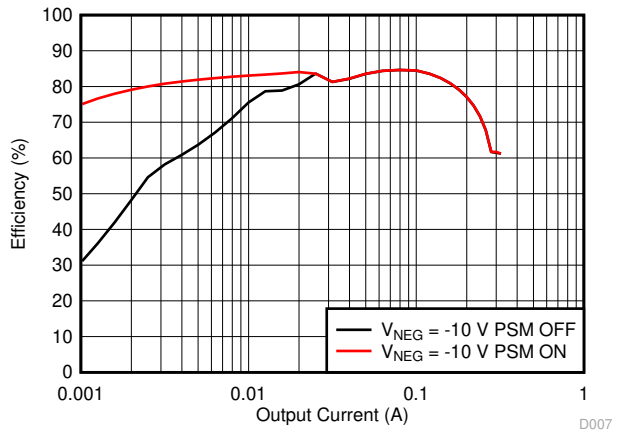
V_I = 3.3V V_{POS} = 10.5V Power-save mode on and off

Figure 8-2. Boost Converter (V_{POS}) Efficiency vs Output Current



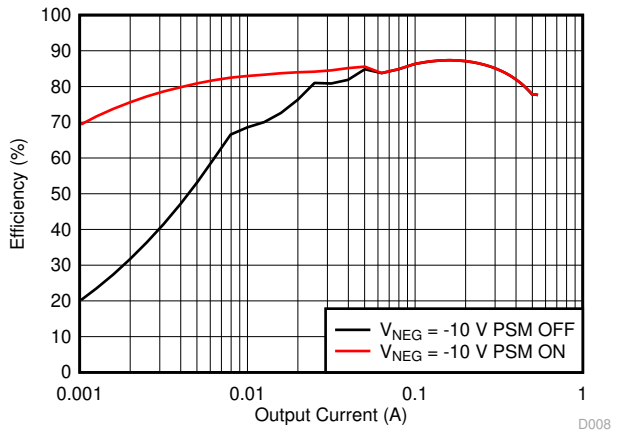
V_I = 5V V_{POS} = 10.5V Power-save mode on and off

Figure 8-3. Boost Converter (V_{POS}) Efficiency vs Output Current



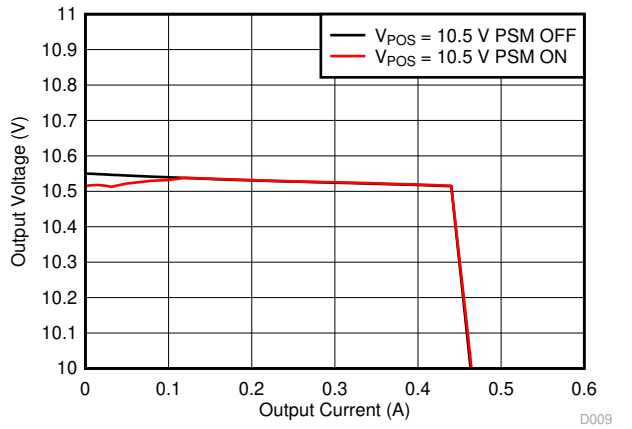
V_I = 3.3V V_{NEG} = –10V Power-save mode on and off

Figure 8-4. Inverting Converter (V_{NEG}) Efficiency vs Output Current



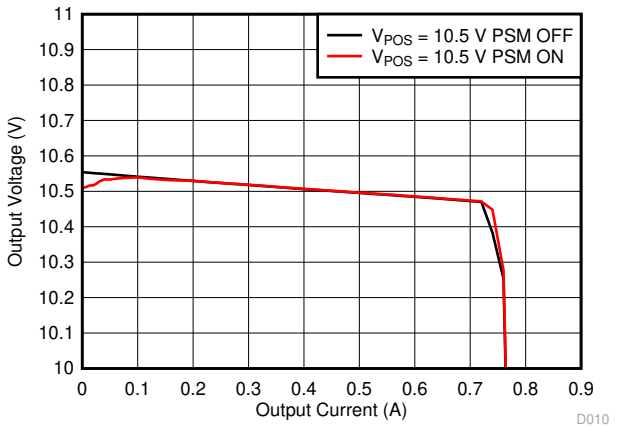
V_I = 5V V_{NEG} = –10V Power-save mode on and off

Figure 8-5. Inverting Converter (V_{NEG}) Efficiency vs Output Current



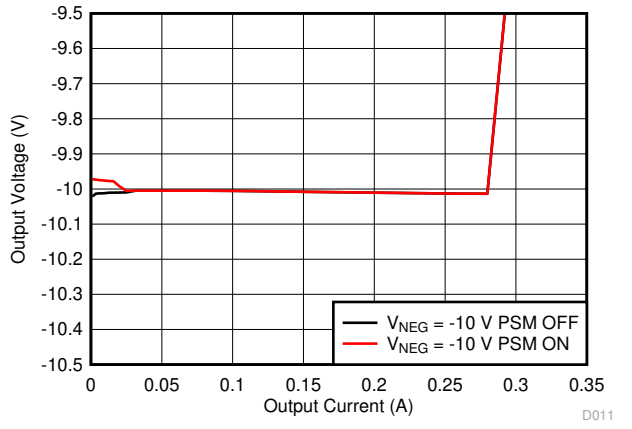
V_I = 3.3V V_{POS} = 10.5V Power-save mode on and off

Figure 8-6. Boost Converter (V_{POS}) Output Voltage vs Output Current



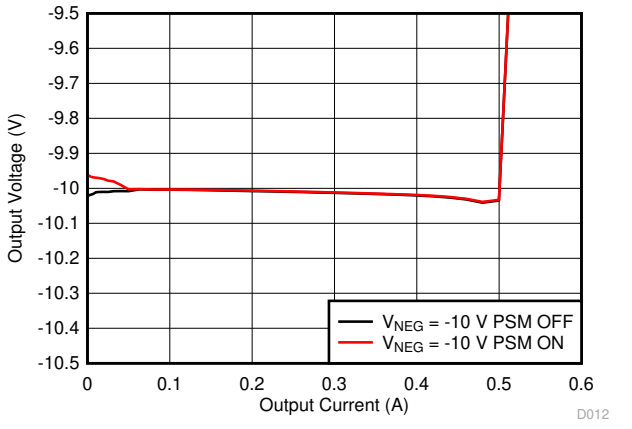
V_I = 5V V_{POS} = 10.5V Power-save mode on and off

Figure 8-7. Boost Converter (V_{POS}) Output Voltage vs Output Current



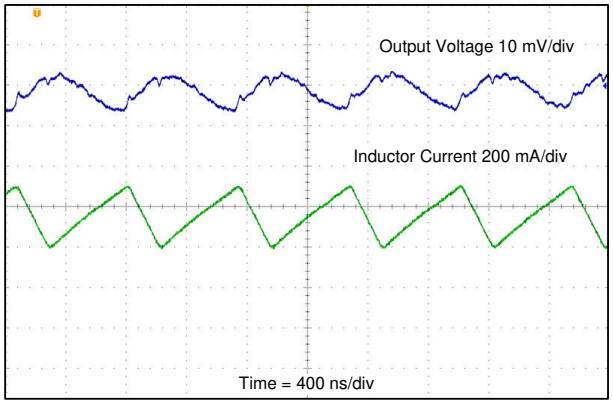
V_I = 3.3V V_{NEG} = –10V Power-save mode on and off

Figure 8-8. Inverting Converter (V_{NEG}) Output Voltage vs Output Current



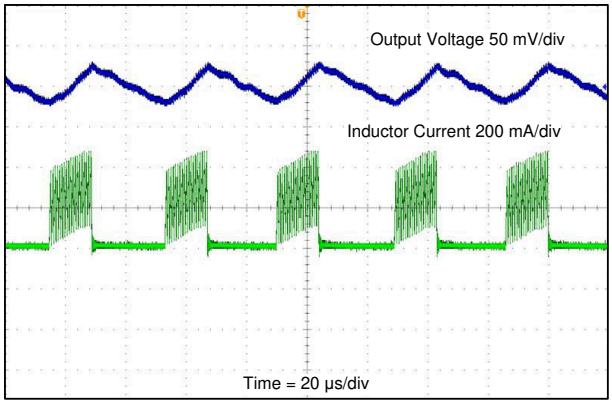
V_I = 5V V_{NEG} = –10V Power-save mode on and off

Figure 8-9. Inverting Converter (V_{NEG}) Output Voltage vs Output Current



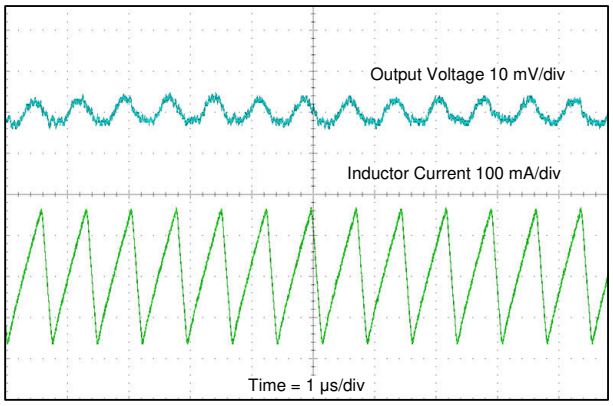
V_I = 3.3V V_{POS} = 10.5V I_{POS} = 200mA Power-save mode off

Figure 8-10. Boost Converter (V_{POS}) Output Ripple



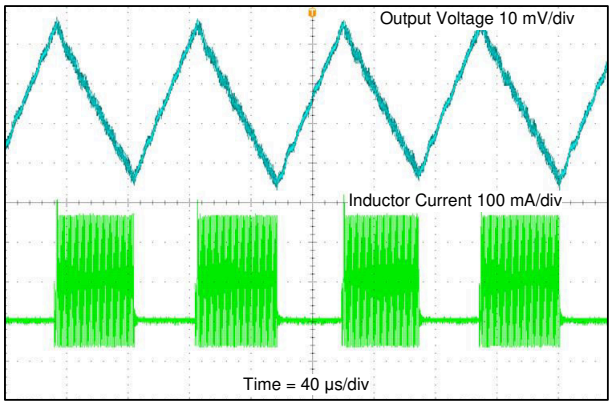
V_I = 3.3V V_{POS} = 10.5V I_{POS} = 20mA Power-save mode on

Figure 8-11. Boost Converter (V_{POS}) Output Ripple



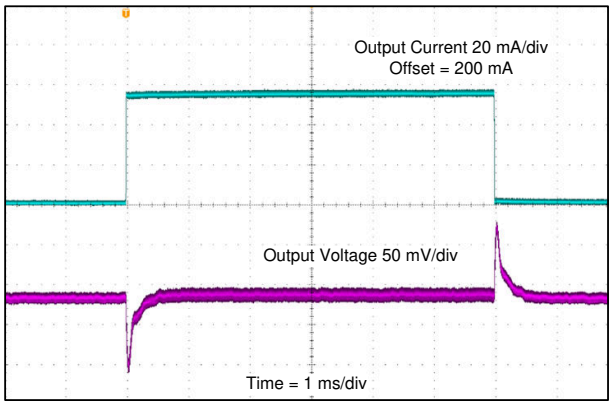
V_I = 3.3V V_{NEG} = –10V I_{NEG} = 200mA Power-save mode off

Figure 8-12. Inverting Converter (V_{NEG}) Output Ripple



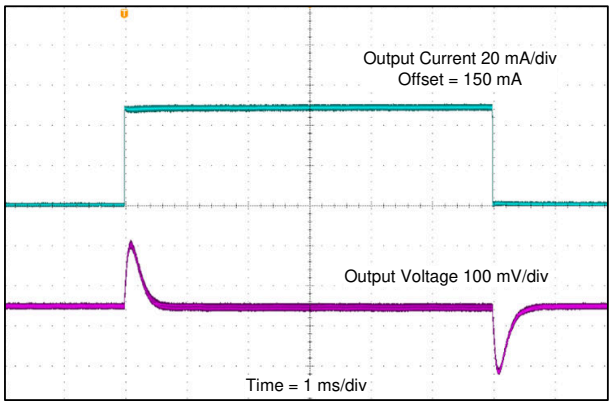
V_I = 3.3V V_{NEG} = –10V I_{NEG} = 20mA Power-save mode on

Figure 8-13. Inverting Converter (V_{NEG}) Output Ripple



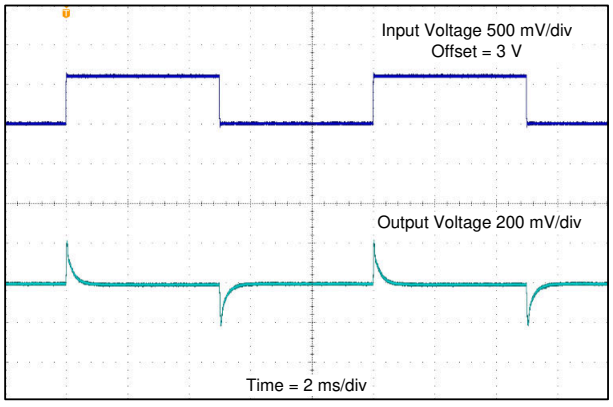
V_I = 3.3V V_{POS} = 10.5V I_{POS} = 200mA to 250mA

Figure 8-14. Boost Converter (V_{POS}) Load Transient Response



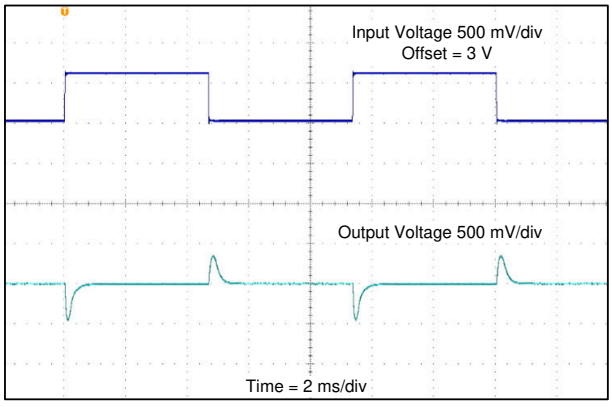
V_I = 3.3V V_{NEG} = –10V I_{NEG} = 150mA to 200mA

Figure 8-15. Inverting Converter (V_{NEG}) Load Transient Response



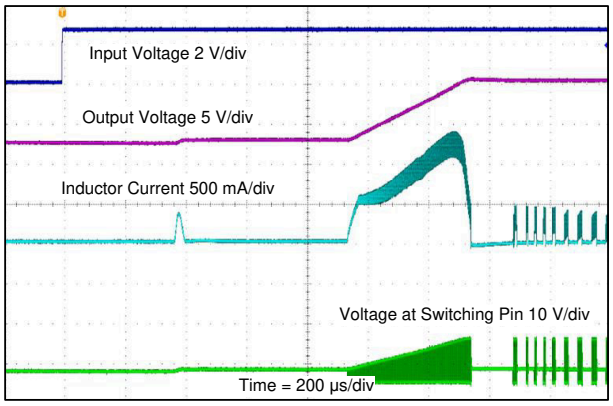
V_I = 3V to 3.6V V_{POS} = 10.5V I_{POS} = 150mA

Figure 8-16. Boost Converter (V_{POS}) Line Transient Response



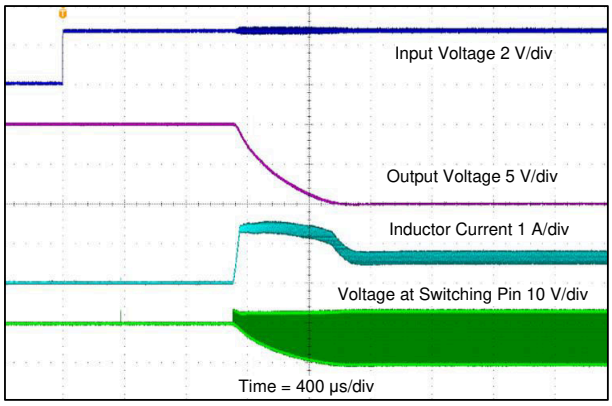
V_I = 3V to 3.6V V_{NEG} = –10V I_{NEG} = 100mA

Figure 8-17. Inverting (V_{NEG}) Converter Line Transient Response



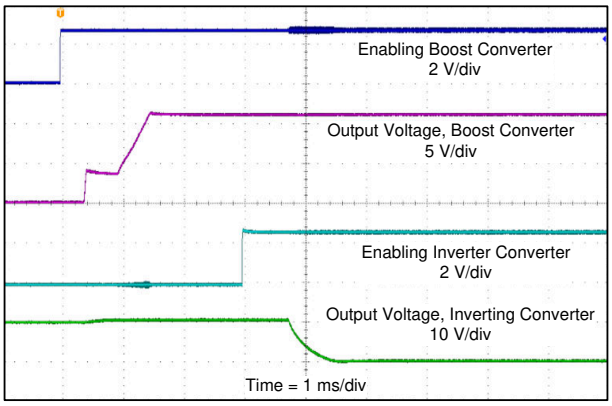
V_I = 3.3V V_{POS} = 10.5V I_{POS} = 46mA

Figure 8-18. Boost Converter (V_{POS}) Start-Up Into Load



V_I = 3.3V V_{NEG} = –10V I_{NEG} = 150mA

Figure 8-19. Inverting Converter (V_{NEG}) Start-Up Into Load



V_I = 3.3V V_{POS} = 10.5V V_{NEG} = –10V

I_{POS} = I_{NEG}= 160mA

Figure 8-20. Boost and Inverting Converter Start-Up Into Load

8.3 Power Supply Recommendations

The TPS65131-Q1 input voltage ranges from 2.7V to 5.5V. Consequently, the supply can come, for example, from a 3.3V or 5V rail. If the device starts into load during the *Soft Start* phase, the drawn input current can be higher than during post-start operation. Consider the application requirements when selecting the power supply.

To avoid unintended toggling of the *Undervoltage Lockout* , connect the TPS65131-Q1 via a low-impedance path to the power supply.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Therefore, use wide and short traces for the main current paths and for the power ground tracks. The input capacitors (C1, C2, C3), output capacitors (C4, C5), the inductors (L1, L2), and the rectifying diodes (D1, D2) should be placed as close as possible to the IC to keep parasitic inductances low. Use a wide PGND plane. Connect the analog ground pin (AGND) to the PGND plane. Further, connect the PGND plane with the exposed thermal pad. Place the feedback dividers as close as possible to the control pin (boost converter) or the VREF pin (inverting converter) of the IC.

Figure 8-21 provides an layout example which is recommended to be followed.

8.4.2 Layout Example

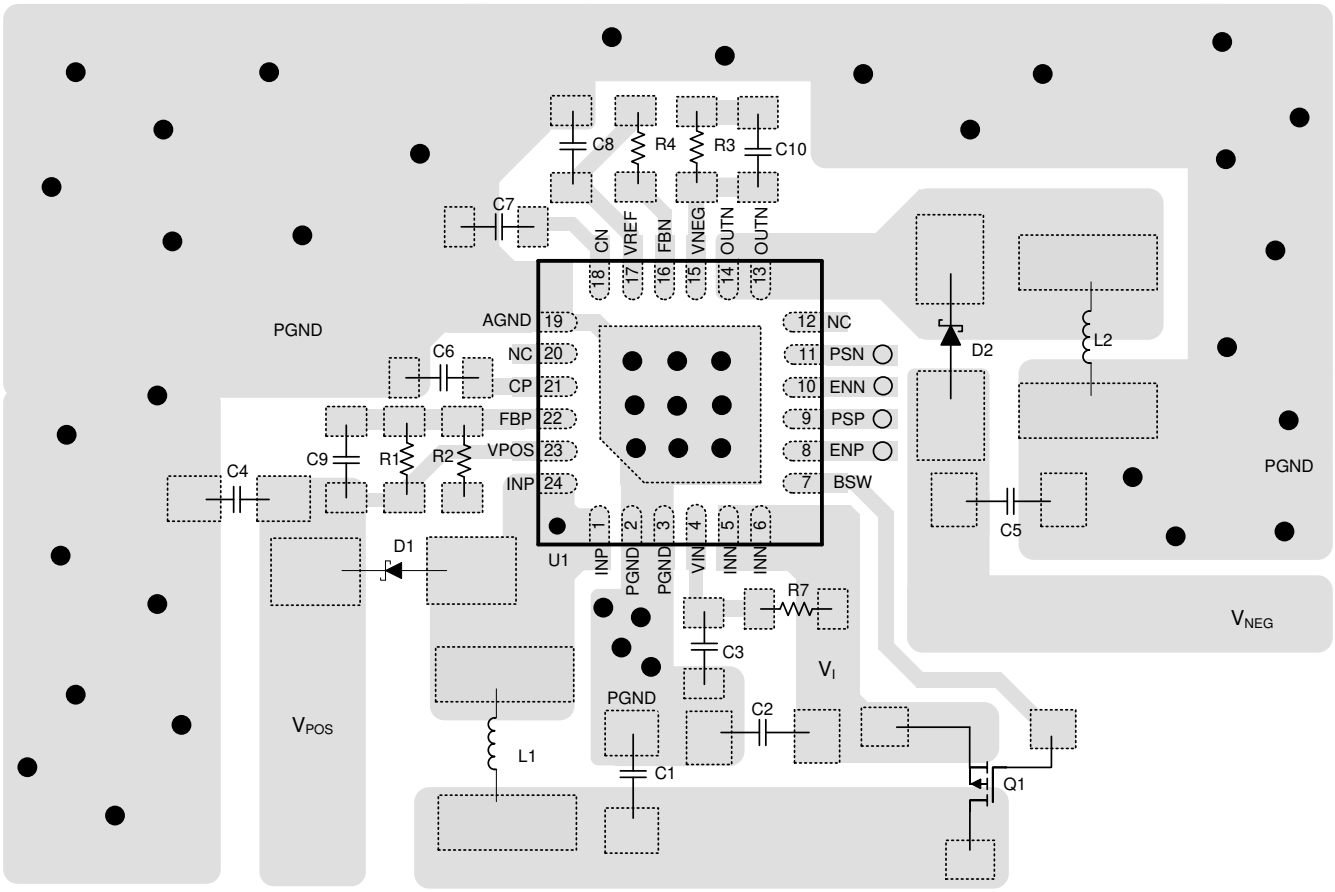


Figure 8-21. TPS65131-Q1 Layout Recommendation

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (March 2017) to Revision F (August 2024)	Page
• Updated *Device Information*Table	1

Changes from Revision D (October 2014) to Revision E (March 2017)	Page
• Changed Section 1 bullet text from "...Qualified.." to...Test Guidance.." and HBM classification level from "H2" to "H1C"	1
• Moved T_{stg} spec to the Abs Max Ratings table per new data sheet standard	4
• Changed "Handling Ratings" to "ESD Ratings" and HBM Value From "±2 kV" to "±1000 V"	4
• Changed Electrical Characteristics condition statement to "This specification applies over the full recommended input voltage range V_I = 2.7 V to 5.5 V and over the temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6 V and T_J = 25°C."	5
• Changed The specification applies over the full recommended input voltage range V_I = 2.7 V to 5.5 V and over the temperature range T_J = –40 °C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6 V and T_J = 25°	6
• Added Section 8.2.4 description	16

Changes from Revision C (March 2014) to Revision D (October 2014) **Page**

- Global editorial changes bringing the datasheet into the new format....1
- Changed max. efficiency from 89% to 91% and from 81% to 85% 1
- Deleted "Minimum 1.25 MHz"....1
- Changed 1-µA shutdown current to typ. 0.2 µA....1
- Added Thermal Pad to Absolute Maximum Ratings. Added min./max. values where missing....4
- Added $V_{(VIN)}$, $V_{(INN)}$, V_{NEG}, V_{POS}, $V_{(ENN)}$, $V_{(ENP)}$, $V_{(PSN)}$ to Recommended Operating Conditions table....4
- Changed symbol names to JEDEC compliance....5
- Added frequency and duty cycles to Switching Characteristics table. Removed from Electrical Characteristics table....6
- Added Rectifier Diode Selection Guide....15
- Added P-MOSFET Selection Guide....15

Changes from Revision B (February 2013) to Revision C (March 2014) **Page**

- Added "Electrical Characteristics tested over –40°C to 125°C Junction Temperature Range"....1
- Added Device Information table 1
- Deleted T_A table row....4
- Changed I_{NN} to V_{INN}, added pin names VIN and INN....4
- Added pin name VPOS....4
- Added pin name VNEG....4
- Changed I_{NP} to V_{INP}, added pin name INP....4
- Changed "between pins OUTN to V_{INN}" to "between pins OUTN to INN"....4
- Added operating junction temperature....4
- Added "In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may require derating. See Section 8.2.5 for details."....4
- Deleted "virtual" from "Operating virtual junction temperature range"....4
- Changed Electrical Characteristics condition statement to "This specification applies over the full recommended input voltage range V_I = 2.7 V to 5.5 V and over the temperature range $T_J = T_A$ = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6 V and $T_J = T_A$ = 25°C."....5
- Changed $I_{LIM,min}$ = 1800 mA to 1700 mA....5
- Deleted V_{POS} = 5 V (105°C) row....5
- Changed $r_{DS(on)P,max}$ (V_{POS} = 5 V) = 300 mΩ to 390 mΩ....5
- Changed $r_{DS(on)P,max}$ (V_{POS} = 10 V) = 200 mΩ to 230 mΩ....5
- Changed $I_{LIMP,min}$ = 1800 mA to 1700 mA....5
- Changed $I_{LIMP,max}$ = 2200 mA to 2250 mA....5
- Added T_A = –40°C to 85°C....5
- Changed minimum f = 1250 kHz to 1150 kHz....6
- Editorially updated Block Diagram....7
- Changed "The maximum recommended junction temperature (T_J) of the TPS65131-Q1 is 125°C." to "The recommended device junction temperature range, T_J, is -40°C to 125°C."....16
- Changed $R_{\theta JA}$ = 37.8°C/W to $R_{\theta JA}$ = 34.1°C/W....16
- Changed "Specified regulator operation is ensured to a maximum ambient temperature T_A of 105°C." to "The recommended operating ambient temperature range for the device is T_A = –40°C to 105°C."....16
- Changed "Therefore, the maximum power dissipation is about 1058 mW" to "Use Equation 13 to calculate the maximum power dissipation, $P_D$max, as a function of T_A. In this equation, use T_J = 125°C to operate the device within the recommended temperature range, use $T_J = T_{(TS)}$ to determine the absolute maximum threshold when the device might go into thermal shutdown."....16
- Changed Equation 13 16

Changes from Revision A (November 2012) to Revision B (February 2013)	Page
• Changed CDM ESD rating from C3B to C4B	1

Changes from Revision * (May 2012) to Revision A (November 2012)	Page
• Device is going from Preview to Production	1
• Added thermal information table values	5
• Added V_{POS} = 5 V (105°C) row and values to Electrical Characteristics table	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

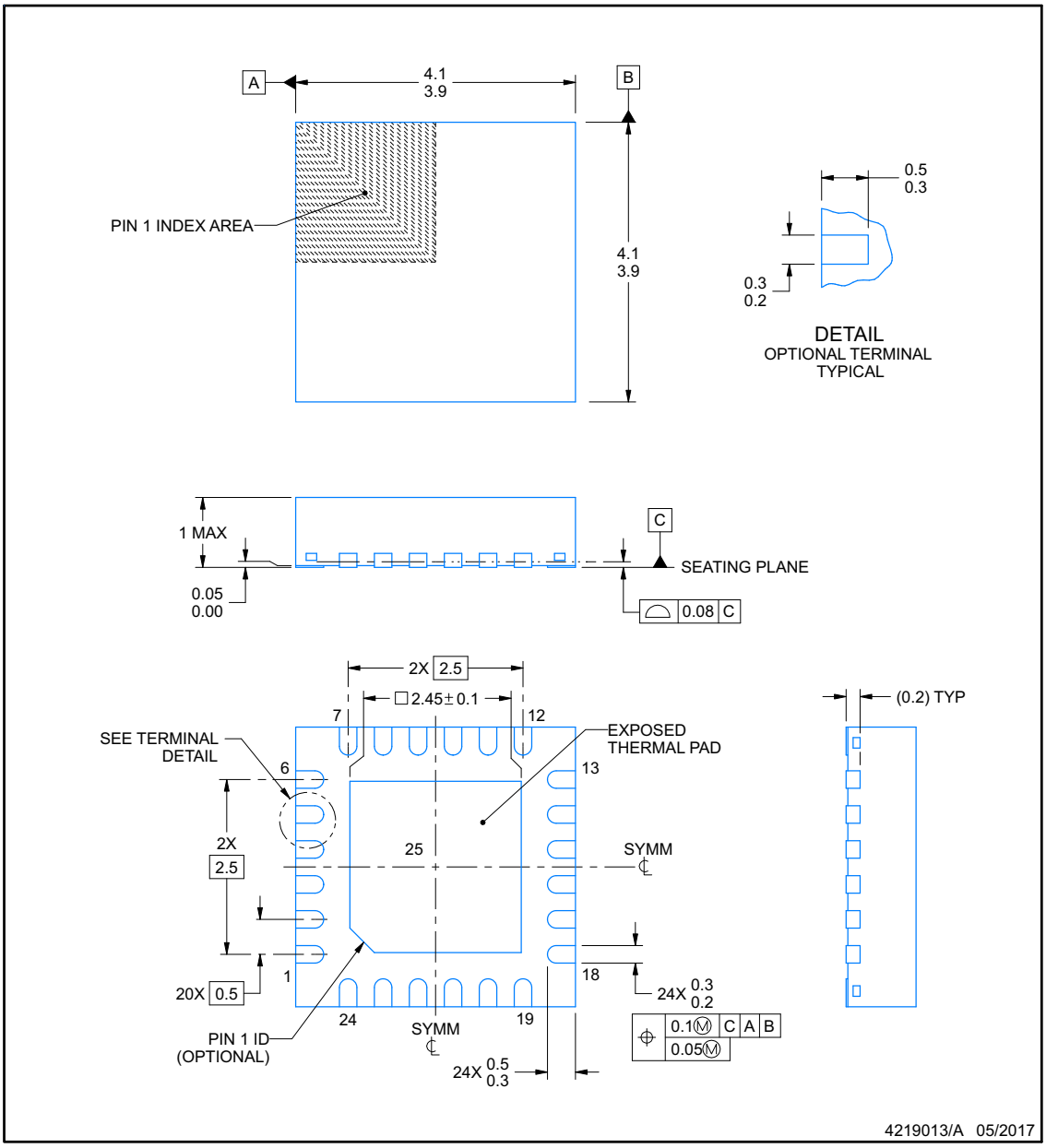
11.1 Mechanical Data

RGE0024B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



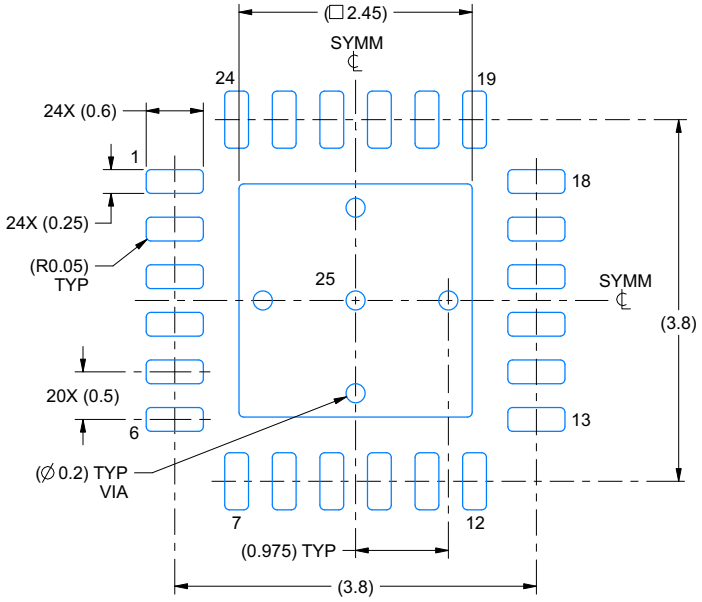
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

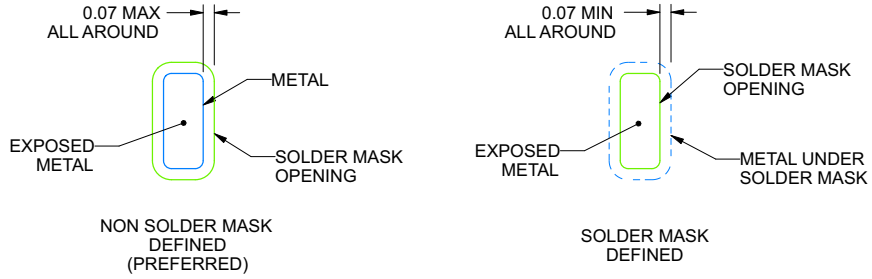
EXAMPLE BOARD LAYOUT

RGE0024B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

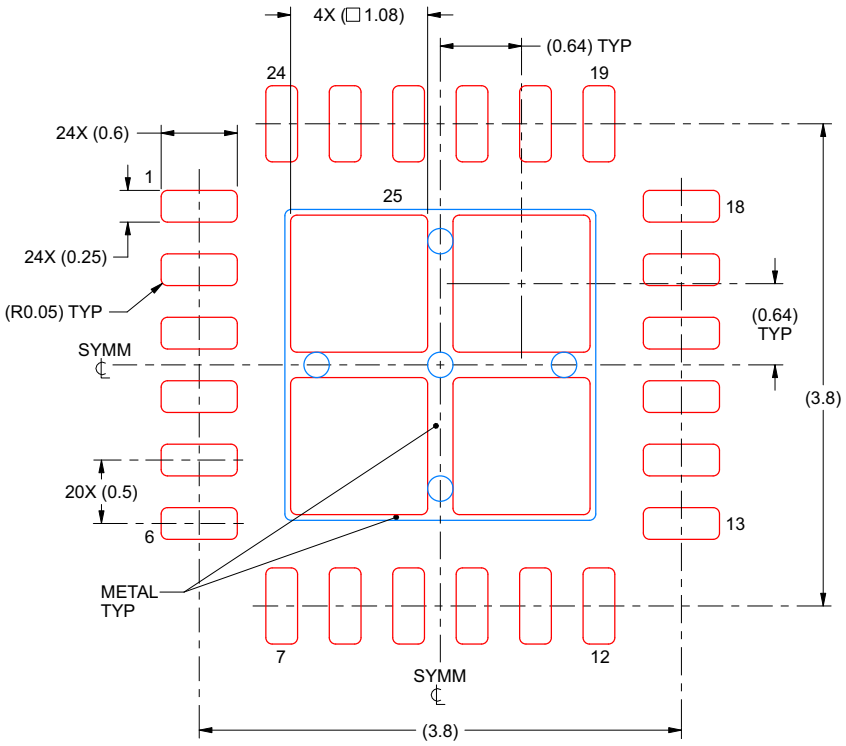
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

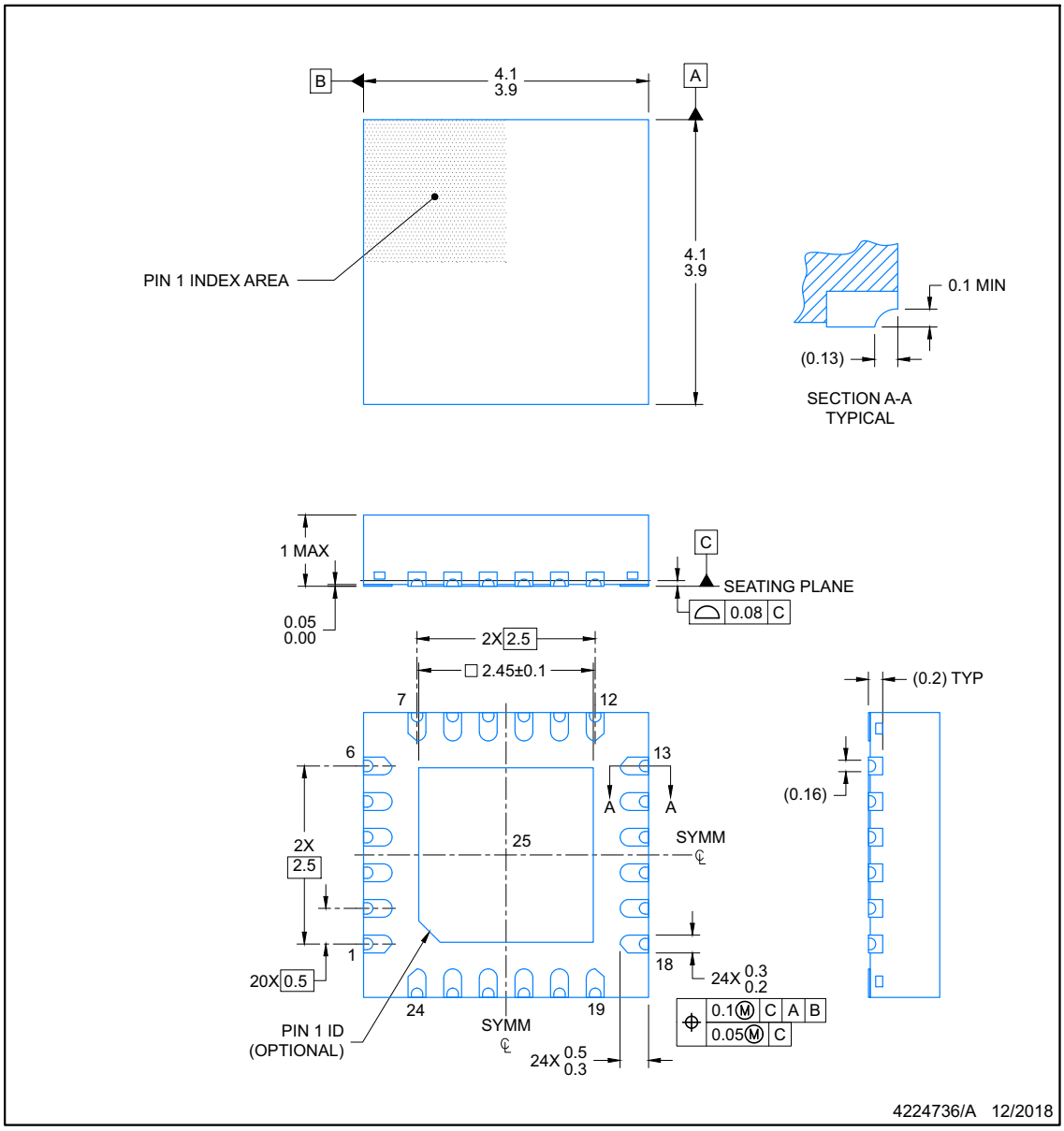
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

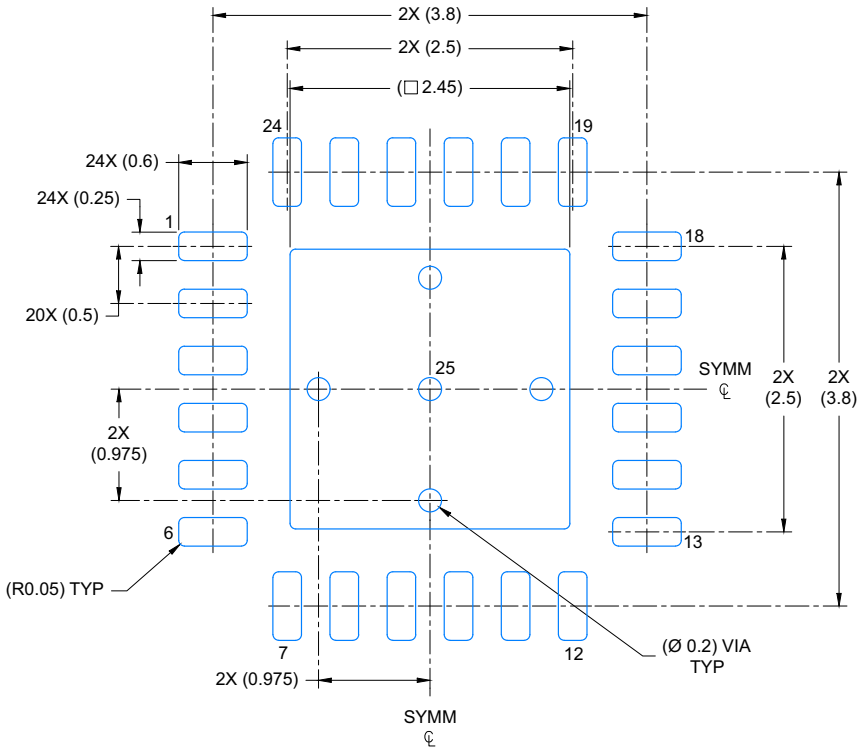
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

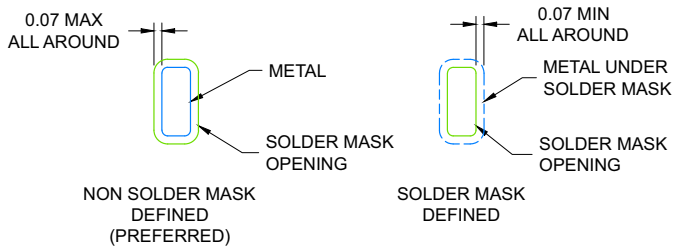
RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X



SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

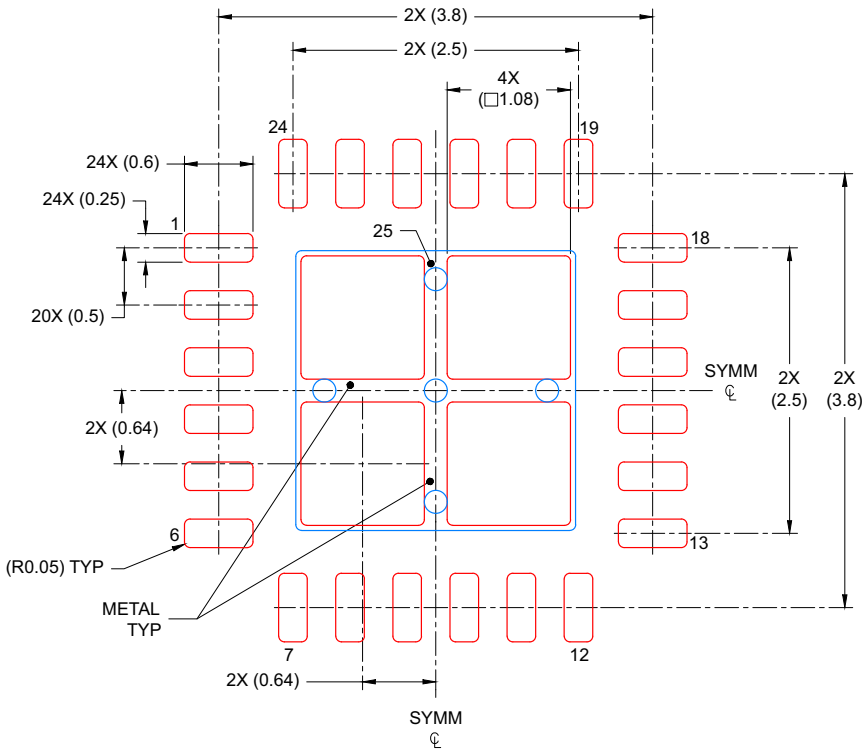
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024N

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

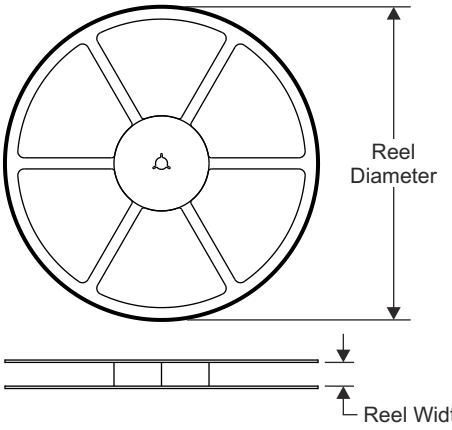
4224736/A 12/2018

NOTES: (continued)

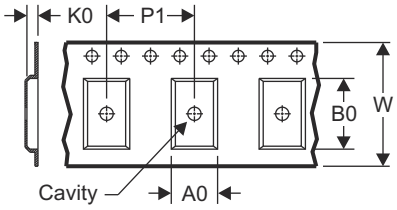
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

11.2 Tape and Reel Information

REEL DIMENSIONS

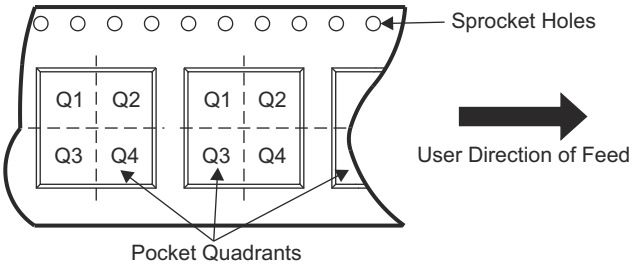


TAPE DIMENSIONS



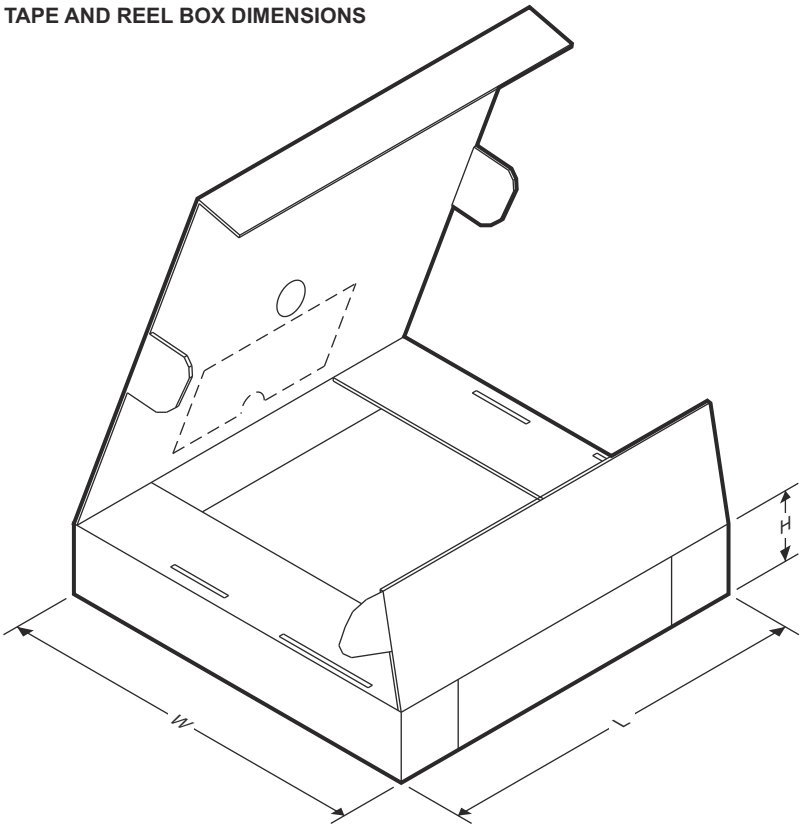
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65131TRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65131WTRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65131TRGERQ1	VQFN	RGE	24	3000	356.0	356.0	35.0
TPS65131WTRGERQ1	VQFN	RGE	24	3000	360.0	360.0	36.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65131TRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	2U65131 Q1	Samples
TPS65131WTRGERQ1	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65131W Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS65131-Q1 :

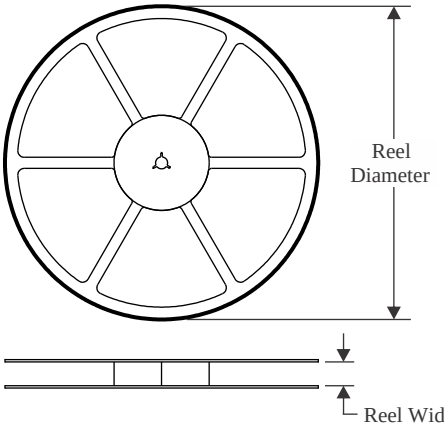
- Catalog : TPS65131

NOTE: Qualified Version Definitions:

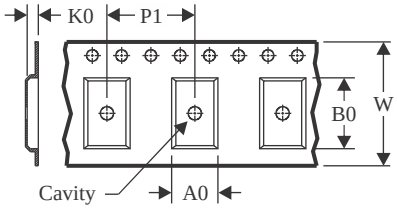
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

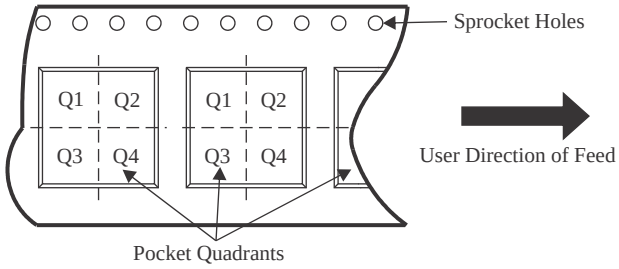


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

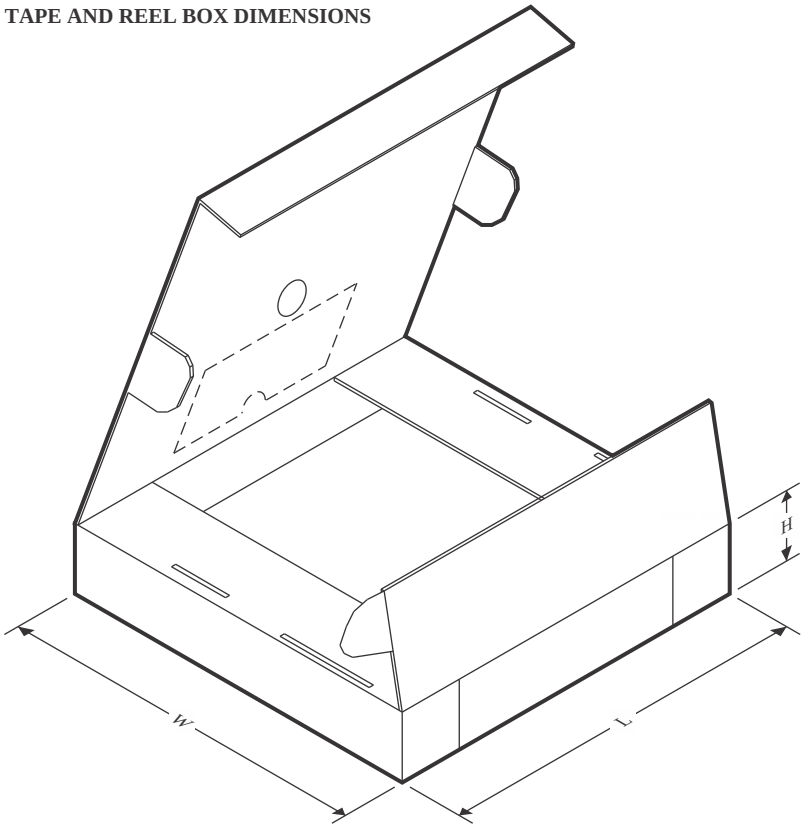
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65131TRGERQ1	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



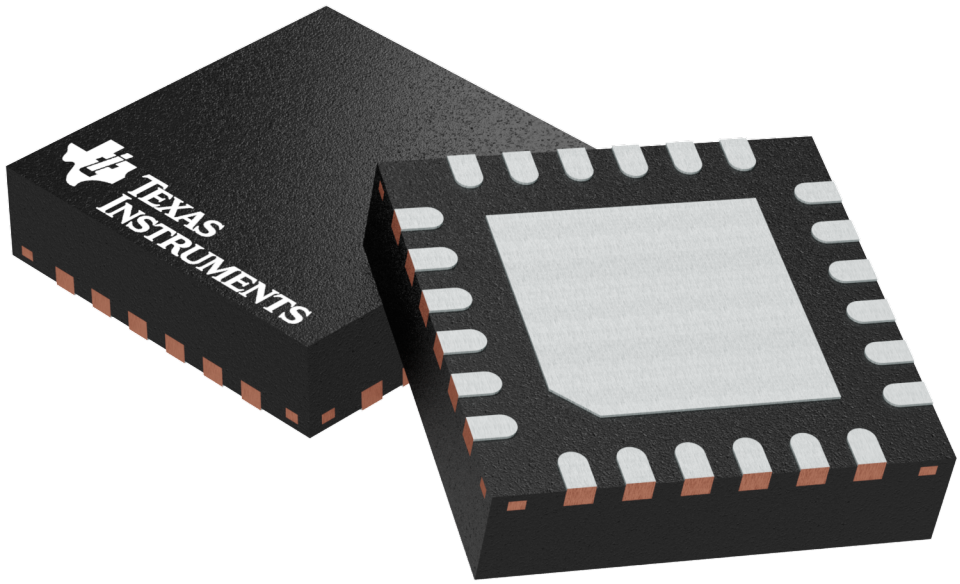
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65131TRGERQ1	VQFN	RGE	24	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

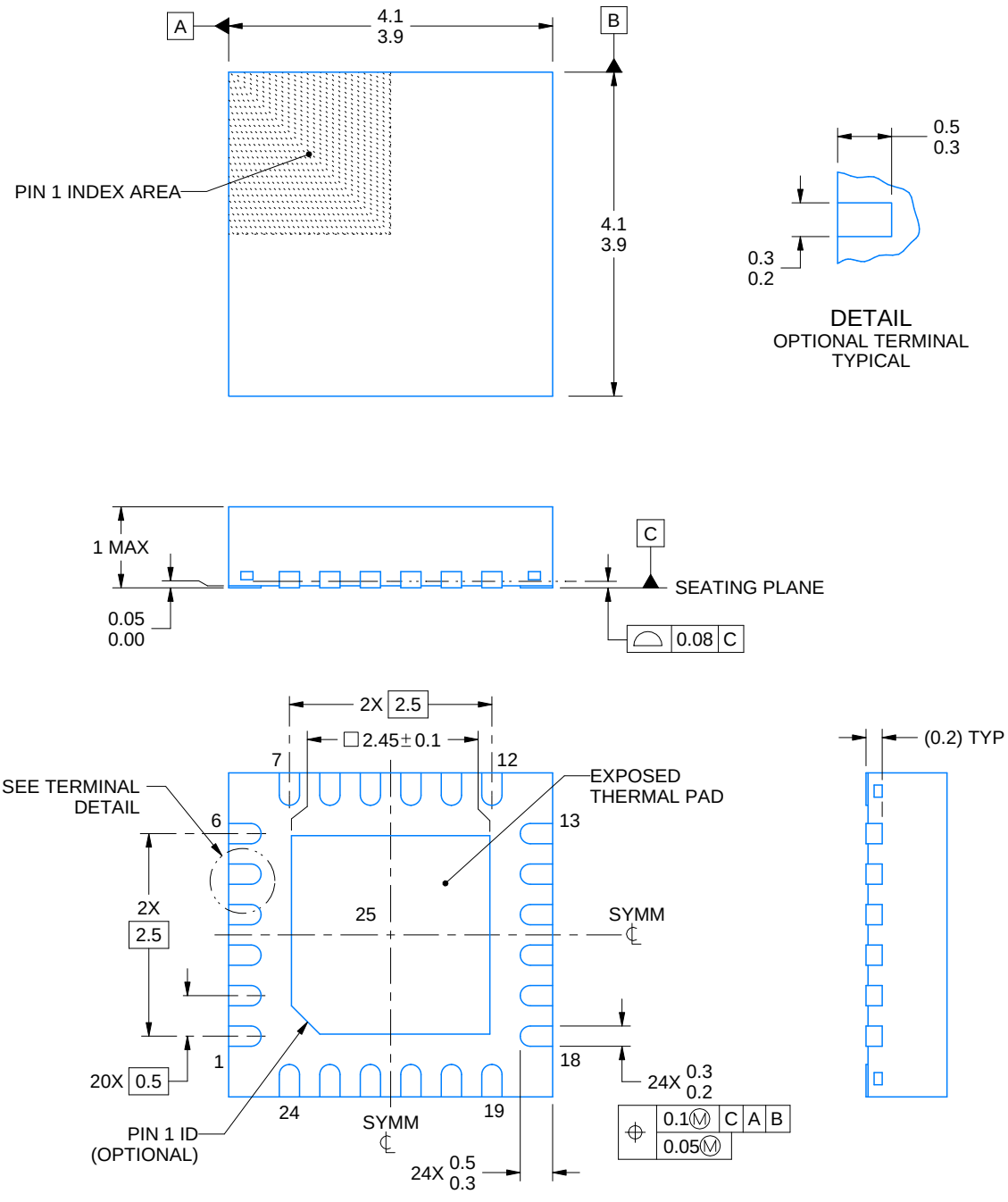
4204104/H

PACKAGE OUTLINE

RGE0024B

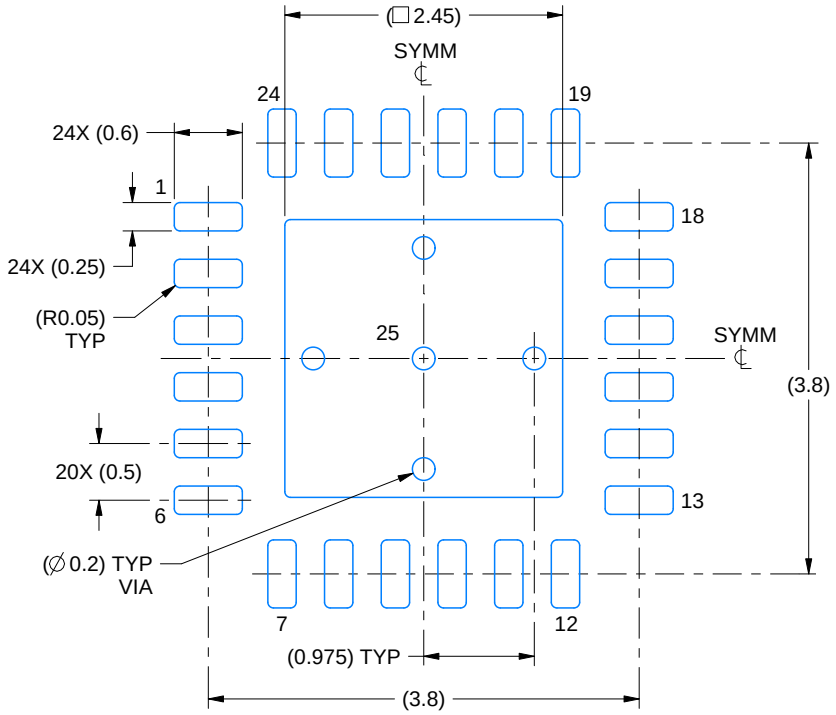
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

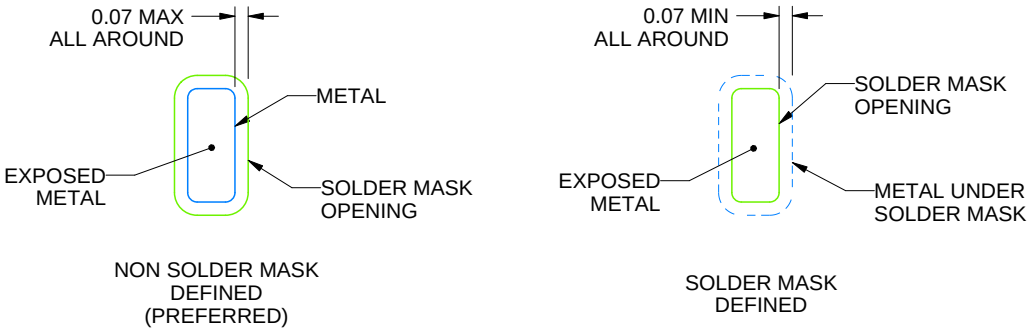


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

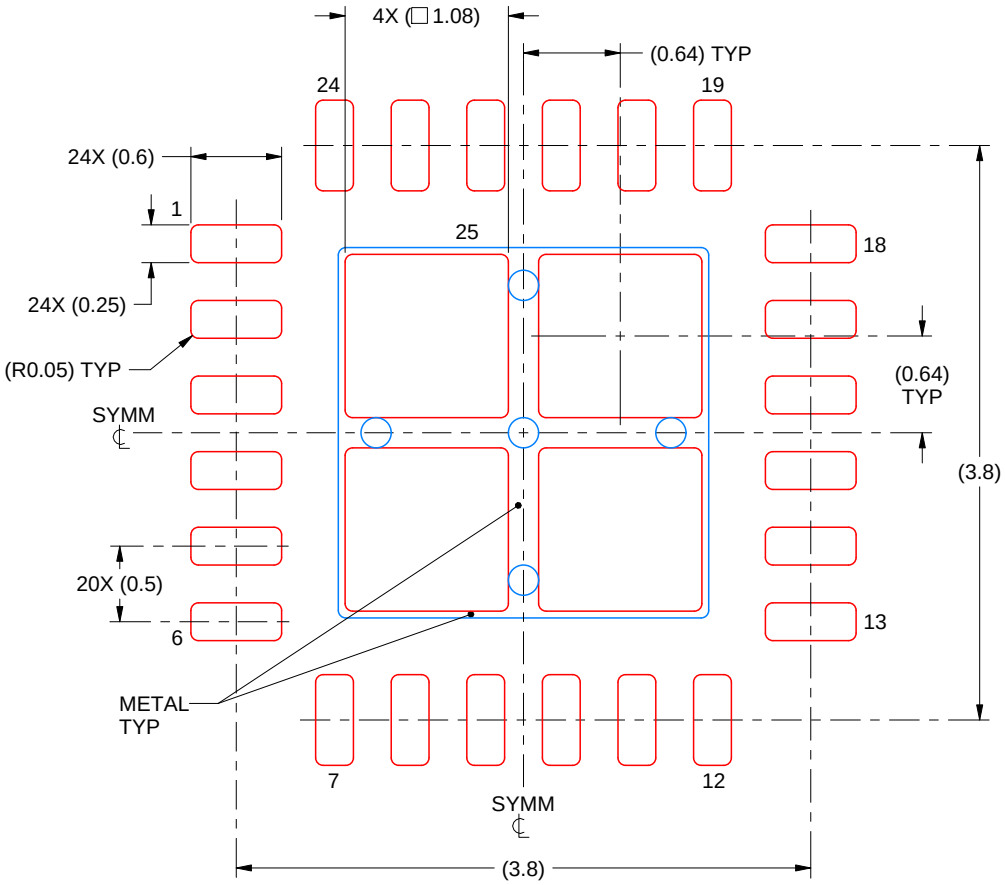


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



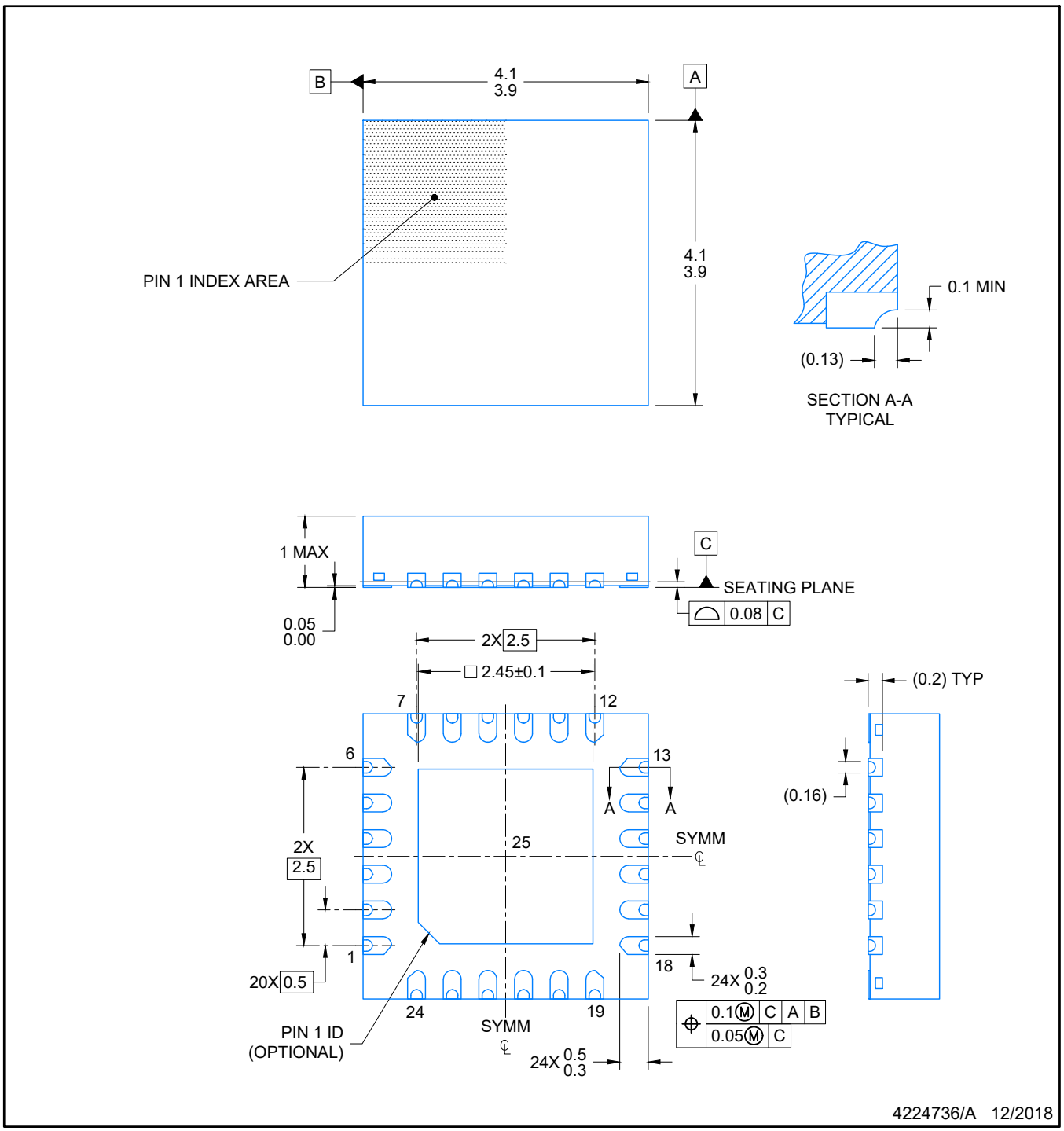
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

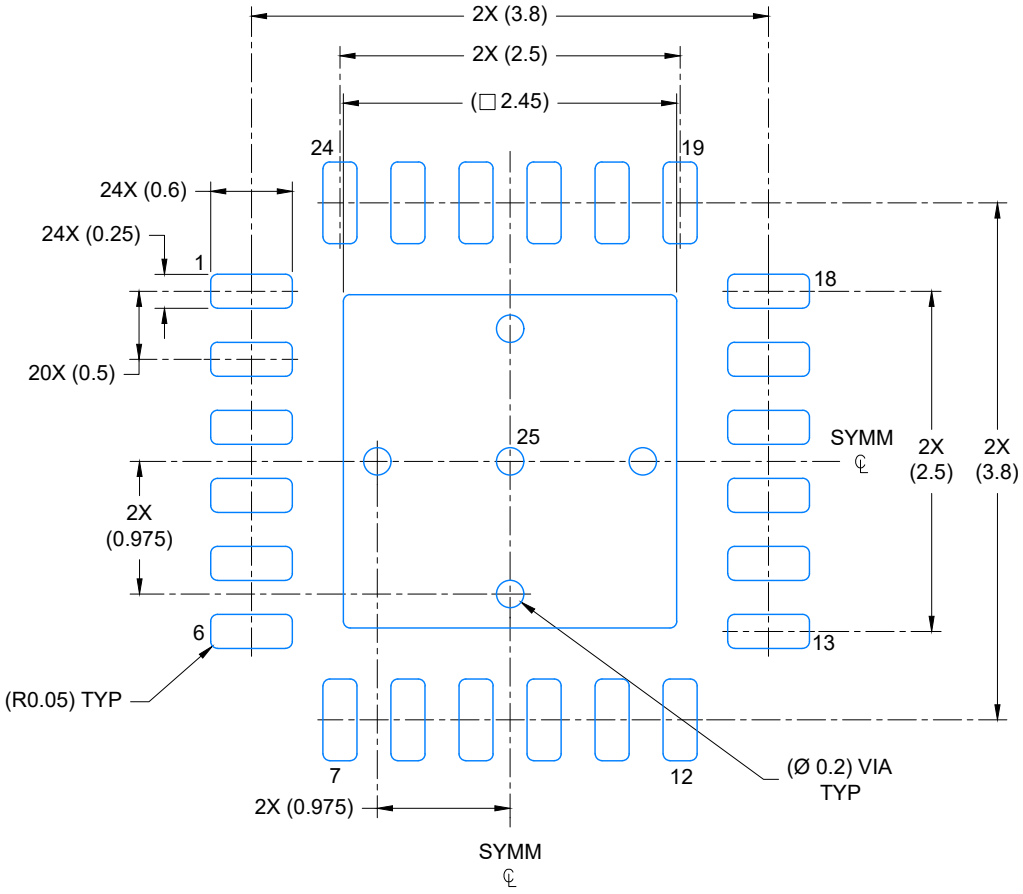
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

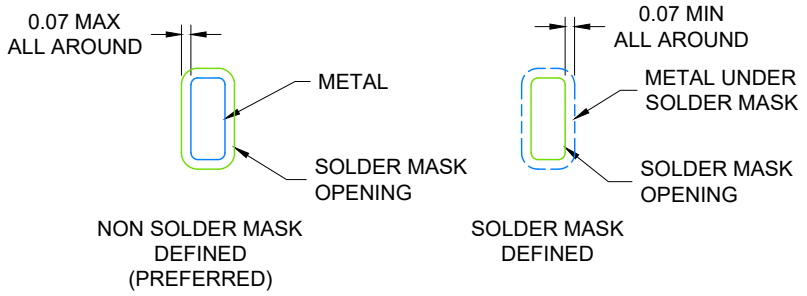


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

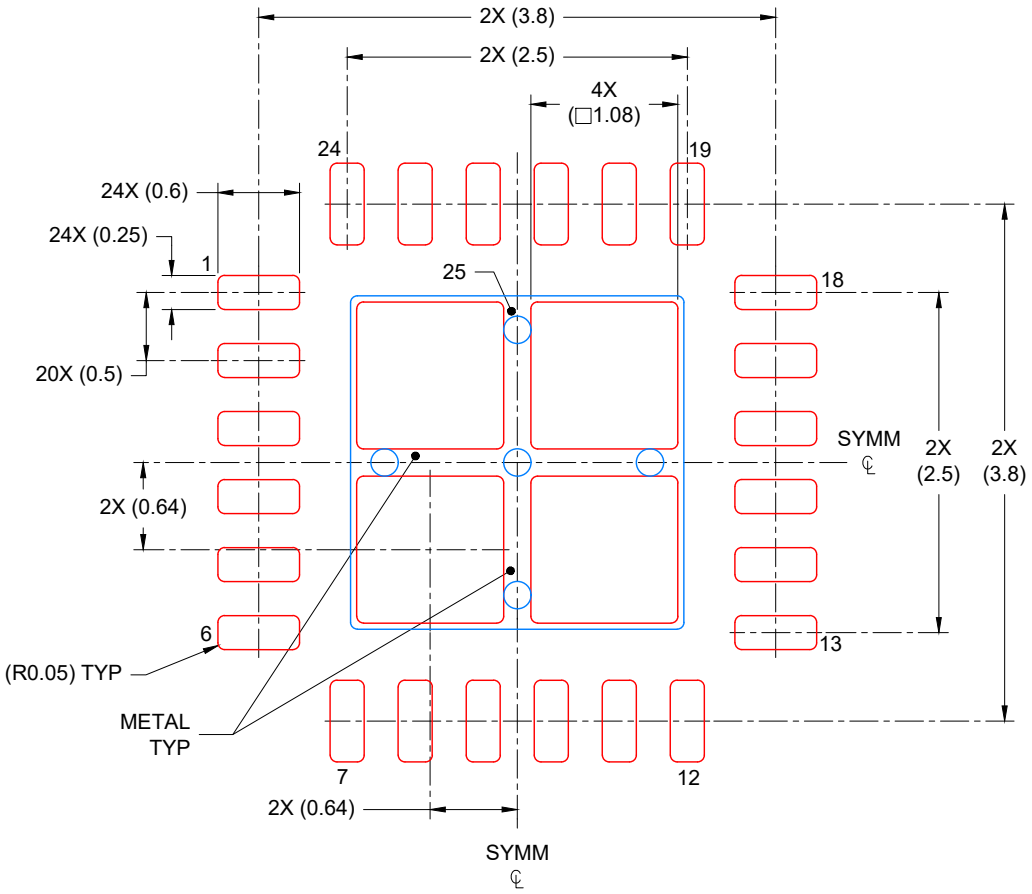


SOLDER MASK DETAILS

4224736/A 12/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 18X

4224736/A 12/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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