

# TPS92662-Q1 High-brightness LED Matrix Manager for Automotive Headlight Systems

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient operating temperature
  - Device HBM classification level H1C
  - Device CDM classification level C5
- Input voltage range: 4.5 V to 60 V
- 12 Integrated bypass switches
  - Four sub-strings of three series switches
  - 20-V maximum across switch
  - 62-V maximum switch to ground
- Multi-drop UART communication interface
  - Up to 31 addressable devices
- Compatible with CAN physical layer
  - Minimum number of wires in cable harness
- Eight-bit ADC with two MUXed inputs
- Crystal oscillator driver
- External EEPROM I<sup>2</sup>C interface
- Programmable 10-bit PWM dimming
  - Individual phase shift and pulse width
  - Device-to-device synchronization
- LED open and short detection and protection

## 2 Applications

- Automotive headlight systems
- High-brightness LED matrix systems
- ADB or glare-free high beam
- Sequential turn and animated daytime running lights

## 3 Description

The TPS92662-Q1 LED matrix manager device enables fully dynamic adaptive lighting solutions by providing individual pixel-level LED control.

The device includes four sub-strings of three series-connected integrated switches for bypassing individual LEDs. The individual sub-strings allow the device to accept either single or multiple current sources. It also allows paralleling up to four switches for bypassing high current LEDs.

A master microcontroller is used to control and manage the TPS92662-Q1 devices via a multi-drop universal asynchronous receiver transmitter (UART) serial interface. The serial interface supports the use of CAN transceivers for a more robust physical layer. The I<sup>2</sup>C communication interface can be used to read from and write to an external EEPROM that can store system calibration data.

An on-board 8-bit ADC with two multiplexed inputs can be used for system temperature compensation and used to measure a binning value which allows for LED binning and coding.

The internal charge pump rail supplies the gate drive voltage for the LED bypass switches. The low on-resistance ( $R_{DS(on)}$ ) of the bypass switch minimizes conduction loss and power dissipation.

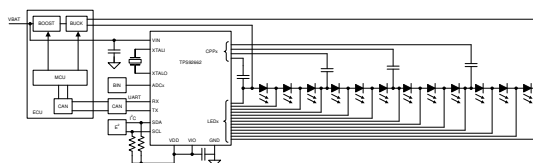
The phase shift and pulse width for each individual LED in the string are programmable. The device uses an internal register to adjust the PWM frequency. Multiple devices can be synchronized. The switch transitions during PWM dimming operation have a programmable slew rate to mitigate EMI concerns.

The device features open LED protection with programmable threshold. The serial interface reports open LED or short LED faults.

### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)   |
|-------------|------------------------|-------------------|
| TPS92662-Q1 | PHP (48)               | 7.00 mm × 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Application**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (January 2019) to Revision B (July 2020)</b>  | <b>Page</b> |
|--|-------------|
| • Added the CLK low-level ( $V_{IH-TH}$ ) and high-level ( $V_{IH-TH}$ ) threshold input voltage thresholds to the <i>Electrical Characteristics</i> ..... | <b>0</b>    |
| • Updated the numbering format for tables, figures and cross-references throughout the document.....   | <b>1</b>    |
| <b>Changes from Revision * (June 2017) to Revision A (January 2019)</b>  | <b>Page</b> |
| • Updated <a href="#">Section 2</a> .....  | <b>1</b>    |
| • Updated <a href="#">Section 3</a> .....  | <b>1</b>    |

## 5 Device and Documentation Support

### 5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS92662QPHPRQ1  | ACTIVE        | HTQFP        | PHP                | 48   | 1000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | 92662Q                  | <a href="#">Samples</a> |
| TPS92662QPHTQ1   | ACTIVE        | HTQFP        | PHP                | 48   | 250            | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | 92662Q                  | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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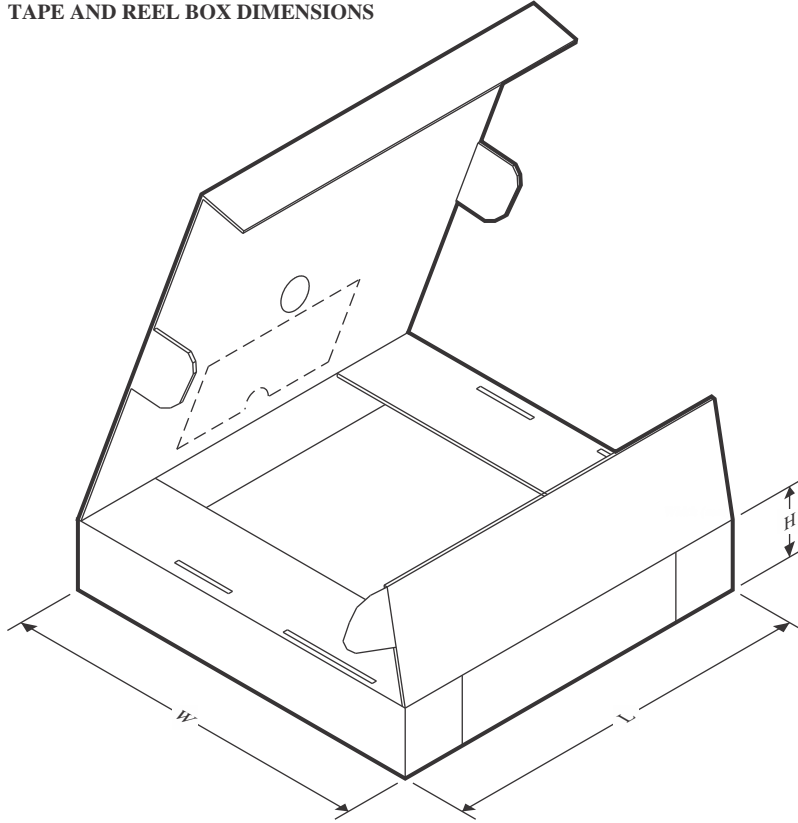
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS92662QPHPRQ1 | HTQFP        | PHP             | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |
| TPS92662QPHPRQ1 | HTQFP        | PHP             | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |
| TPS92662QPHPTQ1 | HTQFP        | PHP             | 48   | 250  | 330.0              | 16.4               | 9.6     | 9.6     | 1.5     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS92662QPHPRQ1 | HTQFP        | PHP             | 48   | 1000 | 350.0       | 350.0      | 43.0        |
| TPS92662QPHPRQ1 | HTQFP        | PHP             | 48   | 1000 | 336.6       | 336.6      | 31.8        |
| TPS92662QPHPTQ1 | HTQFP        | PHP             | 48   | 250  | 336.6       | 336.6      | 31.8        |



## GENERIC PACKAGE VIEW

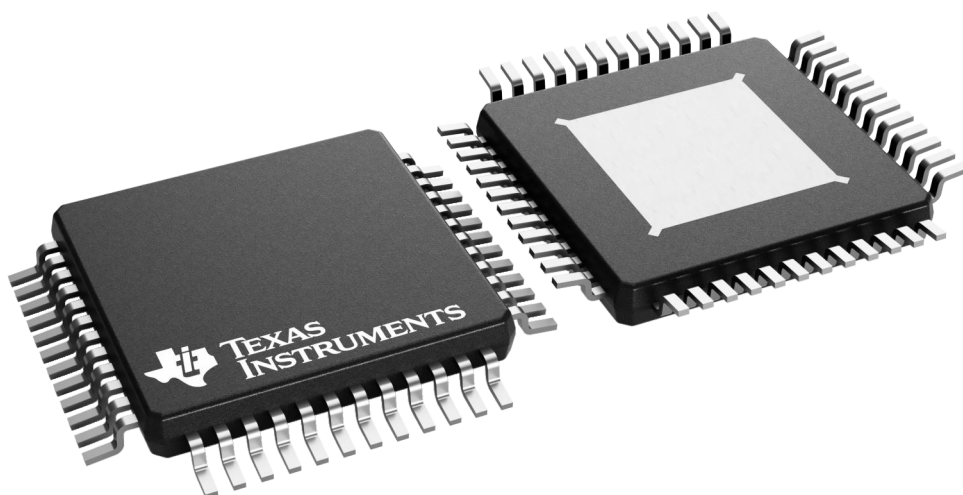
**PHP 48**

**TQFP - 1.2 mm max height**

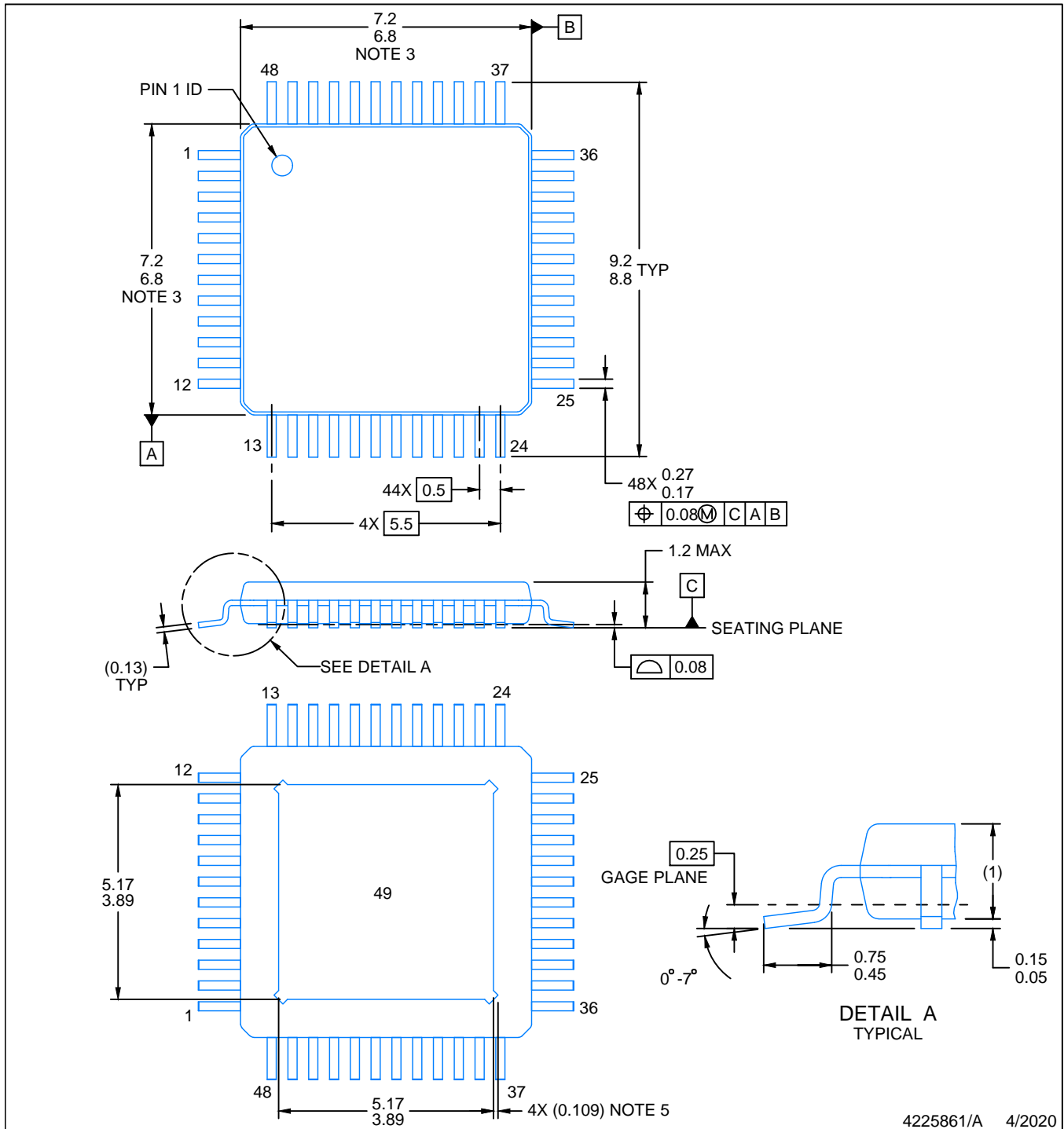
7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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#### NOTES:

PowerPAD is a trademark of Texas Instruments.

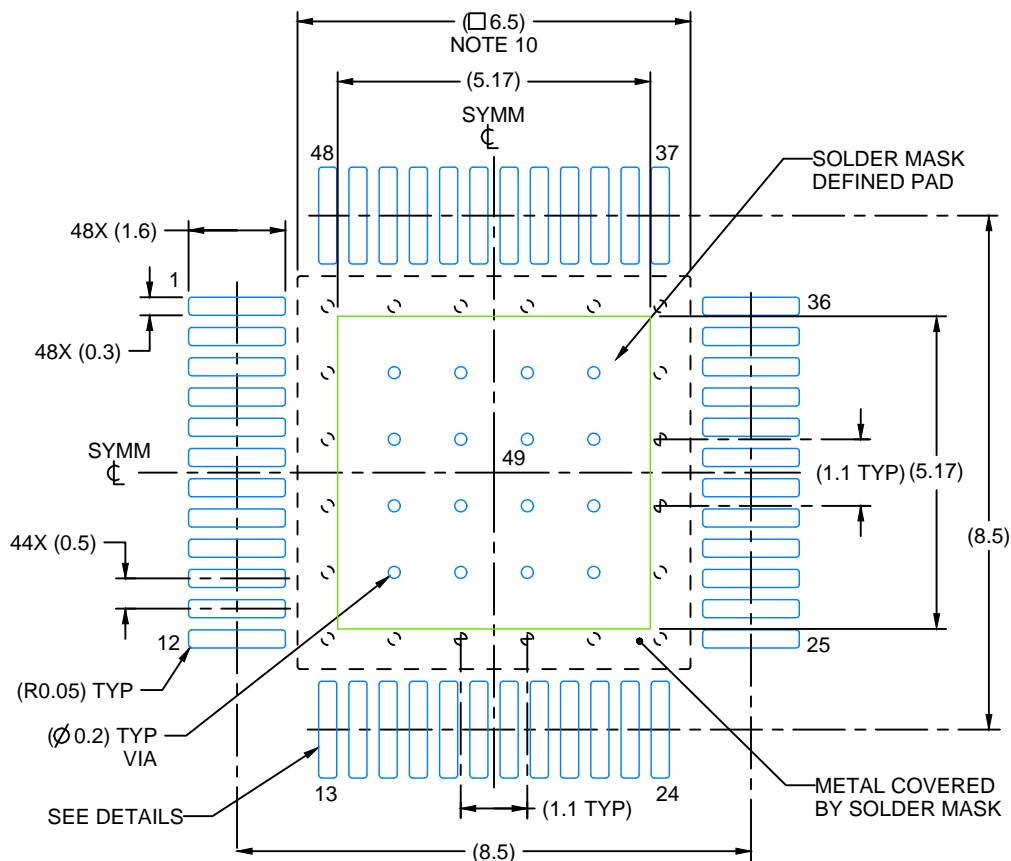
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

# EXAMPLE BOARD LAYOUT

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



4225861/A 4/2020

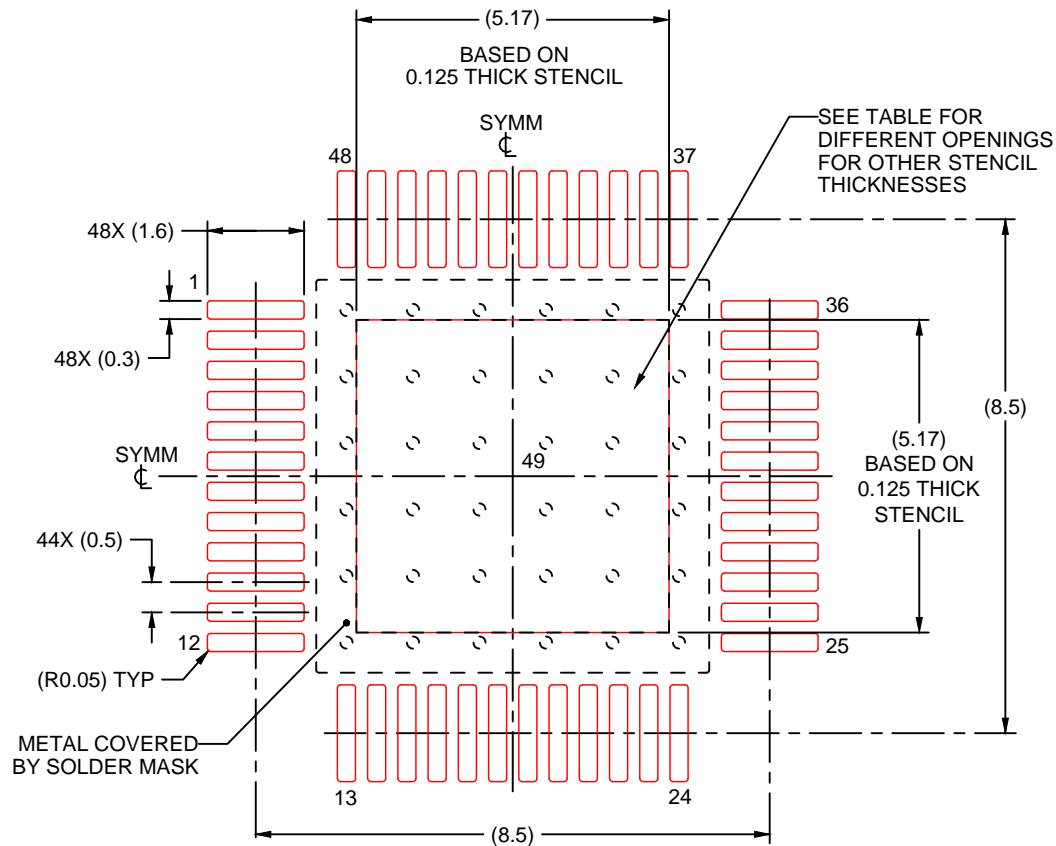
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

**PHP0048G**

## PowerPAD™ HTQFP - 1.2 mm max height

## PLASTIC QUAD FLATPACK



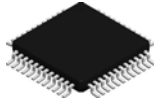
SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 5.78 X 5.78            |
| 0.125             | 5.17 X 5.17 (SHOWN)    |
| 0.150             | 4.72 X 4.72            |
| 0.175             | 4.37 X 4.37            |

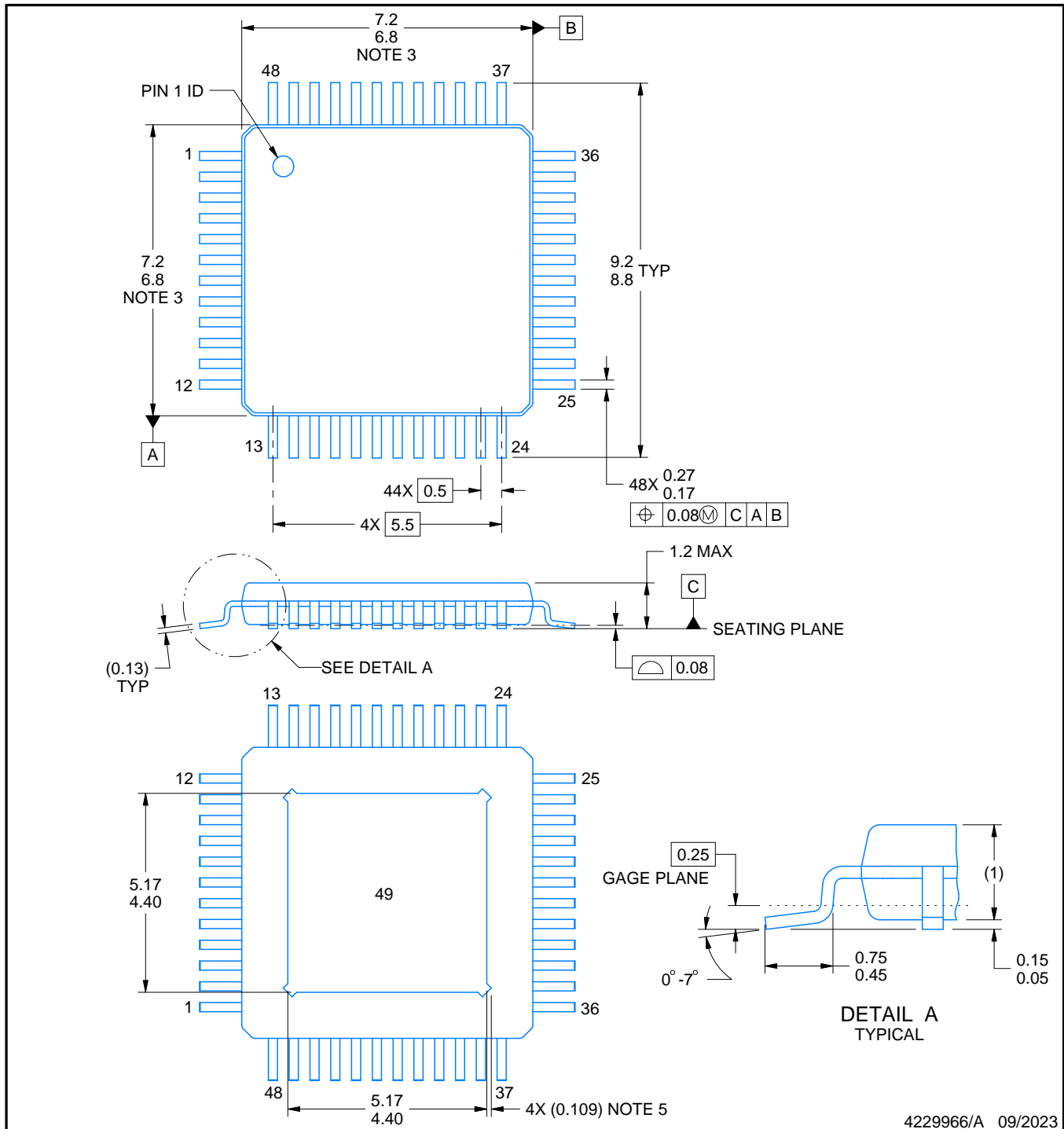
4225861/A 4/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

**PHP0048N****PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



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**NOTES:**

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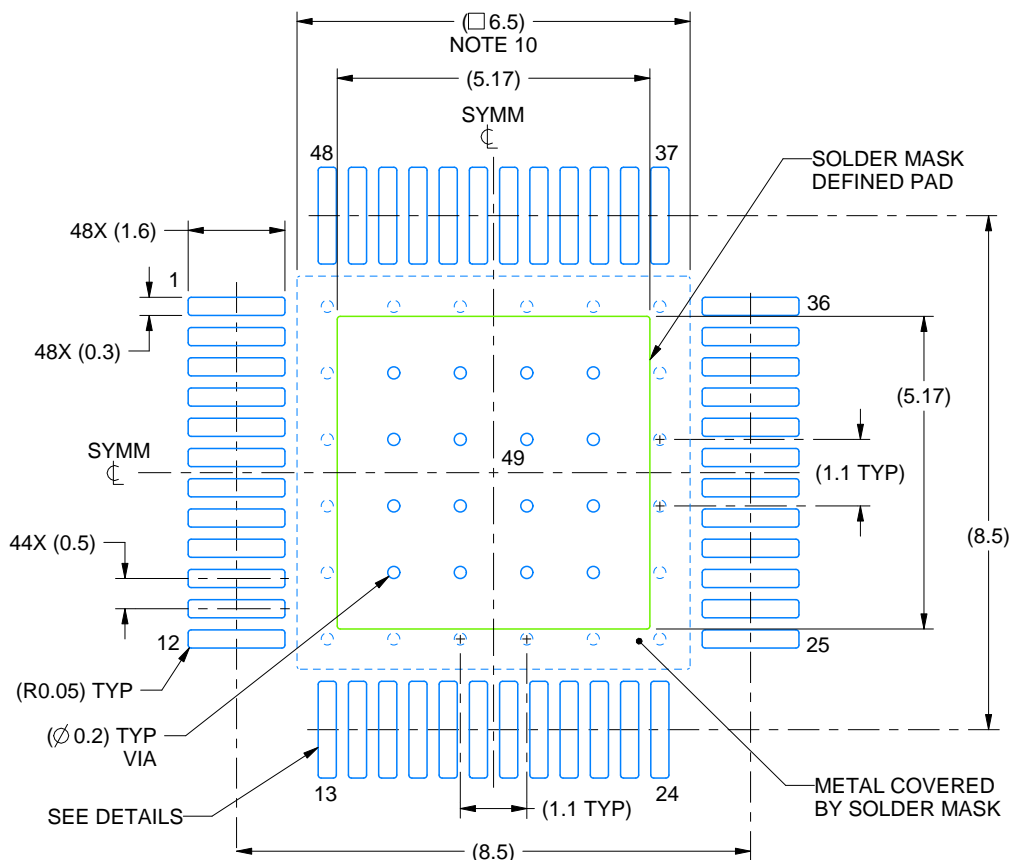
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# EXAMPLE BOARD LAYOUT

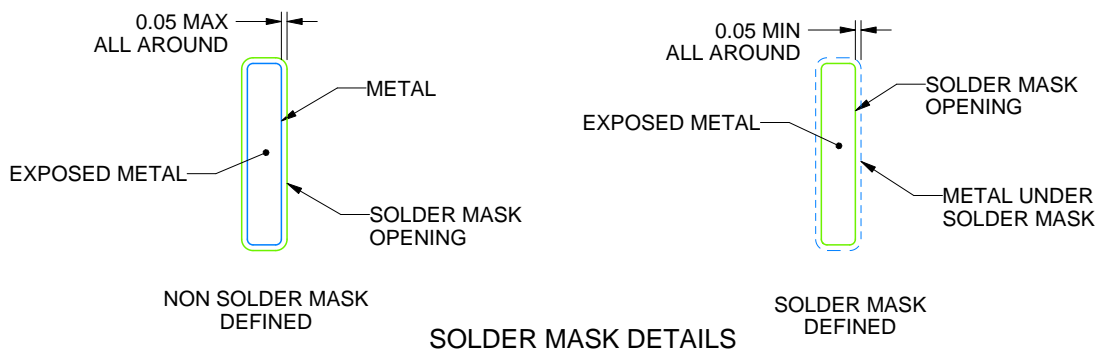
PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



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NOTES: (continued)

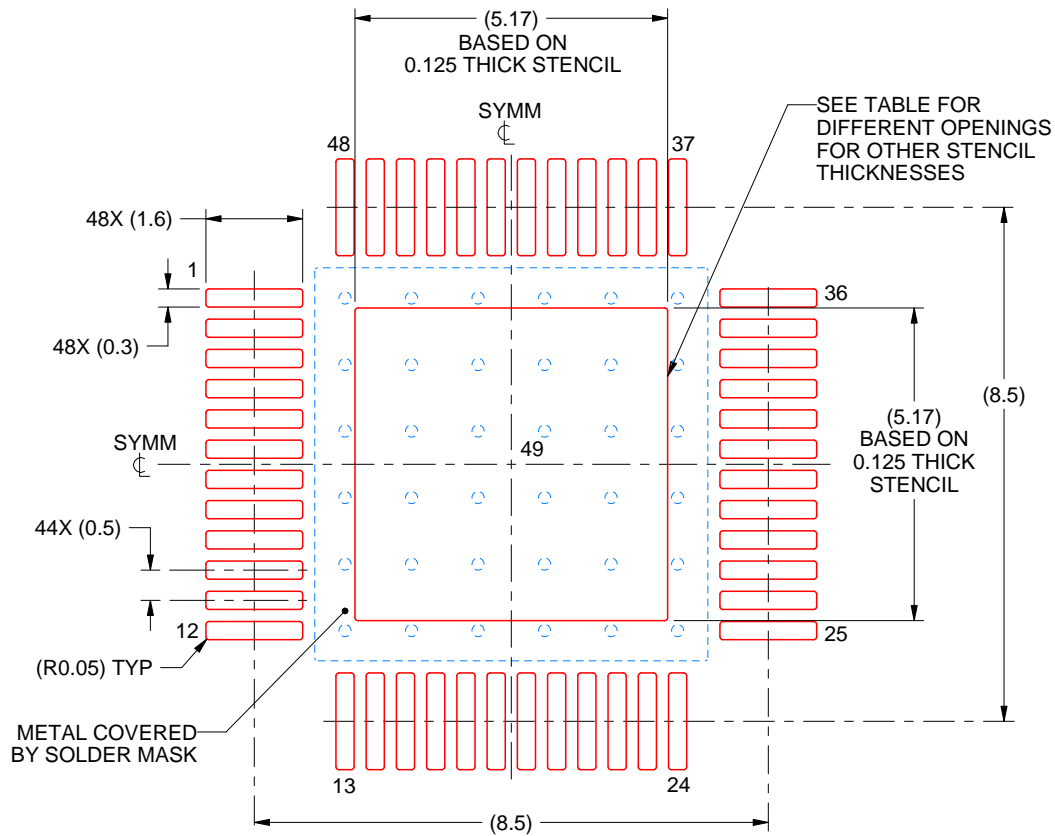
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9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE  
EXPOSED PAD  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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