DUAL 10-BIT 40 MSPS LOW-POWER ANALOG-TO-DIGITAL CONVERTER WITH PGA

FEATURES

- **Qualified for Automotive Applications**
- **3.3-V Single-Supply Operation**
- **Dual Simultaneous Sample-and-Hold Inputs**
- **Differential or Single-Ended Analog Inputs**
- **Programmable Gain Amplifier: 0 dB to 18 dB**
- **Separate Serial Control Interface**
- **Single or Dual Parallel Bus Output**
- **60-dB SNR at f_{IN} = 10.5 MHz**
- **73-dB SFDR at f_{IN} = 10.5 MHz**
- **Low Power: 275 mW**
- **300-MHz Analog Input Bandwidth**
- **3.3-V TTL/CMOS-Compatible Digital I/O**
- **Internal or External Reference**
- **Adjustable Reference Input Range**
- **Power-Down (Standby) Mode**
- **TQFP-48 Package**

APPLICATIONS

- **Digital Communications (Baseband Sampling)**
- **Portable Instrumentation**
- **Video Processing**

DESCRIPTION

The ADS5204 is a dual 10-bit, 40 MSPS analog-to-digital converter (ADC). It simultaneously converts each analog input signal into a 10-bit, binary coded digital word up to a maximum sampling rate of 40 MSPS per channel. All digital inputs and outputs are 3.3-V TTL/CMOS compatible.

An innovative dual pipeline architecture implemented in a CMOS process and the 3.3-V supply results in very low power dissipation. In order to provide maximum flexibility, both top and bottom voltage references can be set from user-supplied voltages. Alternatively, if no external references are available, the on-chip internal references can be used. Both ADCs share a common reference to improve offset and gain matching. If external reference voltage levels are available, the internal references can be powered down independently from the rest of the chip, resulting in even greater power savings.

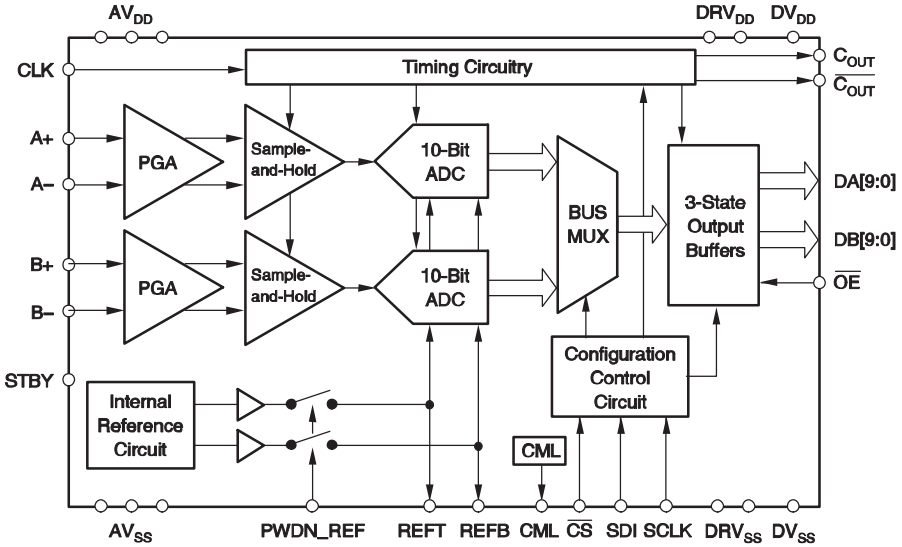
The ADS5204 also features dual, onboard programmable gain amplifiers (PGAs) that allow a setting of 0 dB to 18 dB to adjust the gain of each set of inputs in order to match the amplitude of the incoming signal.

The ADS5204 is characterized for operation from −40°C to +85°C and is available in a TQFP-48 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM



ORDERING INFORMATION†

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR‡	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS5204	TQFP−48	PFB	−40°C to +85°C	AZ5204Q	ADS5204IPFBRQ1	Tape and Reel, 1000

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

		ADS5204−Q1
A_{VDD} to AGND, D_{VDD} to DGND	Supply voltage	−0.5 V to 3.6 V
A_{VDD} to D_{VDD}, AGND to DGND	Supply voltage	−0.5 V to 0.5 V
	Digital input voltage range to DGND	−0.5 V to D_{VDD} + 0.5 V
Now	Analog input voltage range to AGND	−0.5 V to A_{VDD} + 0.5 V
Now	Digital output voltage applied from Ext. Source to DGND	−0.5 V to D_{VDD} + 0.5 V
V_{REFT}, V_{REFB}	Reference voltage input range to AGND	−0.5 V to A_{VDD} + 0.5 V
T_A	Operating free−air temperature range (ADS5204I	−40°C to 85°C
T_{STG}	Storage temperature range	−65°C to 150°C
Now	Soldering temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, T_A, unless otherwise noted(1)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
POWER SUPPLY						
AV_{DD}	Supply voltage		0	3.3	3.6	V
DV_{DD}						
DRV_{DD}						
ANALOG AND REFERENCE INPUTS						
V_{REFT}	Reference input voltage (top)	f_{CLK} = 1 MHz to 80 MHz	1.9	2	2.15	V
V_{REFB}	Reference input voltage (bottom)	f_{CLK} = 1 MHz to 80 MHz	0.95	1	1.1	V
$V_{REFT}–V_{REFB}$	Reference voltage differential	f_{CLK} = 1 MHz to 80 MHz	0.95	1	1.1	V
R_{REF}	Reference input resistance	f_{CLK} = 80 MHz		1650		Ω
I_{REF}	Reference input current	f_{CLK} = 80 MHz		0.62		mA
V_{IN}	Analog input voltage, differential		−1		1	V
V_{IN}	Analog input voltage, single−ended(1)		CML −1		CML +1	V
C_I	Analog input capacitance			8		pF
	Clock input(2)		0		AV_{DD}	V
ANALOG OUTPUTS						
	CML voltage			$AV_{DD}/2$		V
	CML output resistance			2.3		kΩ
DIGITAL INPUTS						
V_{IH}	High-level input voltage		2.4		DV_{DD}	V
V_{IL}	Low-level input voltage		DGND		0.8	V
	Input capacitance			5		pF
t_c (80 MHz)	Clock period		12.5			ns
$t_{w(CLKH)}$, $t_{w(CLKL)}$ (80 MHz)	Pulse duration	Clock high or low	5.25			ns
t_c (40 MHz)	Clock period		25			ns
$t_{w(CLKH)}$, $t_{w(CLKL)}$ (40 MHz)	Pulse duration	Clock high or low	11.25			ns

(1) Applies only when the signal reference input connects to CML.
(2) Clock pin is referenced to AV_{DD}/AV_{SS}.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions with f_{CLK} = 80MHz and use of internal voltage references, and PGA Gain = 0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
AV_{DD}	I_{DD} Operating Supply Current	AV_{DD} = DV_{DD} = DRV_{DD} = 3.3 V, C_L = 10 pF, V_{IN} = 3.5 MHz, −1 dBFS			64	72	mA
DV_{DD}					1.7	2.2	
DRV_{DD}					18	27	
P_D	Power Dissipation	PWDN_REF = 'L'			275	345	mW
		PWDN_REF = 'H'			240	300	
$P_{D(STBY)}$	Standby Power	STDBY = 'H', CLK Held HIGH or LOW			125	175	µW
t_{PD}	Power-up time for all references from standby				550		ms
t_{WU}	Wake-up time	External Reference			40		µs
DIGITAL INPUTS							
I_{IH}	High-level input current on digital inputs include CLK	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V		−1		1	µA
I_{IL}	Low-level input current on digital inputs include CLK			−1		1	µA
DIGITAL OUTPUTS							
V_{OH}	High−level output voltage	AV_{DD} = DV_{DD} = DRV_{DD} = 3 V at I_{OH} = 50 µA, Digital outputs forced HIGH		2.8	2.96		V
V_{OL}	Low-level output voltage	AV_{DD} = DV_{DD} = DRV_{DD} = 3 V at I_{OL} = 50 µA, Digital outputs forced LOW			0.04	0.2	V
C_O	Output capacitance				5		pF
I_{OZH}	High- impedance state output current to high level	AV_{DD} = DV_{DD} = DRV_{DD} = 3.6 V		−1		1	µA
I_{OZL}	High-impedance state output current to low level			−1		1	µA
	Data output rise and fall time	C_{LOAD} = 10 pF, Single-bus mode			3		ns
		C_{LOAD} = 10 pF, Dual-bus mode			5		ns
REFERENCE OUTPUTS							
V_{REFTO}	Reference top voltage	Absolute Min/Max values valid and tested for AV_{DD} = 3.3 V		1.85	2	2.1	V
V_{REFBO}	Reference bottom voltage			0.925	1	1.05	V
REFT−REFB	Differential reference voltage			0.925	1.0	1.05	V
DC ACCURACY							
INL	Integral nonlinearity, end point .	Internal references(1)	T_A = −40°C to 85°C	−1.5	±0.4	1.5	LSB
DNL	Differential nonlinearity	Internal references(2)	T_A = −40°C to 85°C	−0.9	±0.4	1.0	LSB
	Missing codes	No Missing Codes Assured					
	Zero error(3)	AV_{DD} = DV_{DD} = DRV_{DD} = 3.3 V External References (3)			0.12	±1.5	%FS
	Full-scale error				0.28	±1.5	%FS
	Gain error				0.24	±1.5	%FS

(1) Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best-fit line between these two endpoints.

(2) Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the best-fit line between these two endpoints.

(3) Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/2 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024). Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1.5 LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

DYNAMIC PERFORMANCE(1)

$T_A = T_{MIN}$ to T_{MAX}, $AV_{DD} = DV_{DD} = DRV_{DD} = 3.3$ V, $f_{IN} = -1$ dBFS, Internal Reference, $f_{CLK} = 80$ MHz, $f_S =$ 40 MSPS, Differential Input Range = 2 Vp−p, and PGA Gain = 0 dB, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{IN} = 3.5 MHz		9.7		Bits
		f_{IN} = 10.5 MHz	9.3	9.7		Bits
		f_{IN} = 20 MHz		9.6		Bits
THD	Total harmonic distortion	f_{IN} = 3.5 MHz		−71		dB
		f_{IN} = 10.5 MHz		−71	−63	dB
		f_{IN} = 20 MHz		−68		dB
SNR	Signal-to-noise ratio	f_{IN} = 3.5 MHz		60.5		dB
		f_{IN} = 10.5 MHz		60.5		dB
		f_{IN} = 20 MHz		60		dB
SINAD	Signal-to-noise ratio + distortion	f_{IN} = 3.5 MHz		60		dB
		f_{IN} = 10.5 MHz	57	60		dB
		f_{IN} = 20 MHz		60		dB
SFDR	Spurious-free dynamic range	f_{IN} = 3.5 MHz		75		dB
		f_{IN} = 10.5 MHz	66	73		dB
		f_{IN} = 20 MHz		70.5		dB
	Analog input bandwidth	See Note (2)		300		MHz
IMD	2-Tone intermodulation distortion	f_1 = 9.5 MHz, f_2 = 9.9 MHz		−68		dBc
	A/B channel crosstalk			−75		dBc
	A/B channel offset mismatch			0.016	1.75	% of FS
	A/B channel full-scale error mismatch			0.025	1	% of FS

(1) These specifications refer to a 25-Ω series resistor and 15-pF differential capacitor between A/B+ and A/B− inputs; any source impedance brings the bandwidth down.

(2) Analog input bandwidth is defined as the frequency at which the sampled input signal is 3 dB down on unity gain and is limited by the input switch impedance.

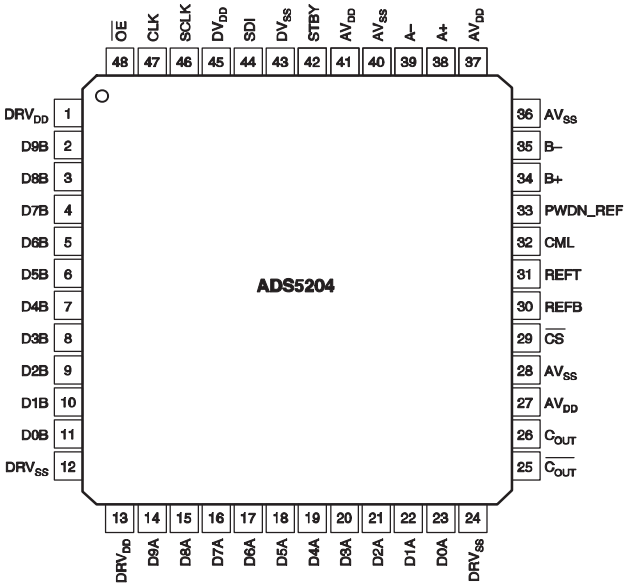
PGA SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Gain Range		0 to 18		dB
Gain Step Size(1)		0.5826		dB
Gain Error(2)	−0.15	±0.025	0.15	dB
Control Bits Per Channel			5	Bits

(1) See Table 2, PGA Gain Code. Ideal step size: 18.0618 dB / 31 = 0.5826 dB

(2) Deviation from ideal. See Table 2, all gain settings.

PIN CONFIGURATION



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
DRV_{DD}	1,13	I	Supply Voltage for Output Drivers
DRV_{SS}	12, 24	I	Digital Ground for Output Drivers
DA 9..0	14-23	O	Data Outputs for Bus A. D9 is MSB. This is the primary bus. Data from both input channels can be output on this bus or data from channel A only. The data outputs are in 3-state during power-down (see the *Register Configuration* table).
DB 9..0	2-11	O	Data Outputs for Bus B. D9 is MSB. This is the second bus. Data is output from the B channel when dual bus output mode is selected. The data outputs are in 3-state during power-down and single-bus modes (see the *Timing Options* table).
$\overline{OE}$	48	I	Output Enable. A low on this terminal will enable the data output bus, C_{OUT} and $\overline{C_{OUT}}$.
C_{OUT}	26	O	Latch Clock for the Data Outputs. C_{OUT} is in 3-state during power down.
$\overline{C_{OUT}}$	25	O	Inverted Latch Clock control for the Data Outputs. $\overline{C_{OUT}}$ is in 3-state during power down.
SDI	44	I	Serial Data I/O
DV_{SS}	43	I	Digital Ground
CLK	47	I	Clock Input. The input is sampled on each rising edge of CLK when using a 40-MHz input and alternate rising edges when using an 80-MHz input. The clock pin is referenced to AV_{DD} and AV_{SS} to reduce noise coupling from digital logic.
DV_{DD}	45	I	Digital Supply Voltage
AV_{DD}	27,37,41	I	Analog Supply Voltage
$\overline{CS}$	29	I	Serial Data Registers Chip Select
AV_{SS}	28,36,40	I	Analog Ground
B−	35	I	Negative Input for the Analog B Channel
B+	34	I	Positive Input for the Analog B Channel
REFT	31	I/O	Reference Voltage Top. The voltage at this terminal defines the top reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1-µF capacitor between REFT and AV_{SS} is highly recommended. Additionally a 0.1-µF capacitor should be connected between REFT and REFB.
REFB	30	I/O	Reference Voltage Bottom. The voltage at this terminal defines the bottom reference voltage for the ADC. Sufficient filtering should be applied to this input: the use of 0.1-µF capacitor between REFB and AV_{SS} is recommended. Additionally, a 0.1-µF capacitor should be connected between REFT and REFB.
CML	32	O	Common-Mode Level. This voltage is equal to (AV_{DD} − AV_{SS})/2. An external capacitor of 0.1µF should be connected between this terminal and AV_{SS} when CML is used as a bias voltage. No capacitor is required if CML is not used.
PDWN_REF	33	I	Power-Down for Internal Reference Voltages. A HIGH on this terminal disables the internal reference circuit.
STBY	42	I	Standby Input. A high on this terminal powers down the device.
A−	39	I	Negative Input for the Analog A Channel
A+	38	I	Positive Input for Analog A Channel
SCLK	46	I	Serial Data Clock. Maximum clock rate is 20 MHz.

TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	Input clock rate		1		80	MHz
	Conversion rate		1		40	MSPS
	Clock duty cycle (40MHz)		45	50	55	%
	Clock duty cycle (80MHz)		42	50	58	%
$t_{d(o)}$	Output delay time	C_L = 10 pF		9	14	ns
$t_{s(m)}$	Mux setup time		9	10.4		ns
$t_{h(m)}$	Mux hold time	C_L = 10 pF	1.7	2.1		ns
$t_{s(o)}$	Output setup time	C_L = 10 pF	9	10.4		ns
$t_{d(pipe)}$	Pipeline delay (latency, channels A and B)	MODE = 0, SELB = 0		8		CLK Cycles
$t_{d(pipe)}$	Pipeline delay (latency, channels A and B)	MODE = 1, SELB = 0		4		CLK Cycles
$t_{d(pipe)}$	Pipeline delay (latency, channel A)	MODE = 0, SELB = 1		8		CLK Cycles
$t_{d(pipe)}$	Pipeline delay (latency, channel B)	MODE = 0, SELB = 1		9		CLK Cycles
$t_{d(pipe)}$	Pipeline delay (latency, channel A)	MODE = 1, SELB = 1		8		CLK Cycles
$t_{d(pipe)}$	Pipeline delay (latency, channel B)	MODE = 1, SELB = 1		9		CLK Cycles
$t_{h(o)}$	Output hold time	C_L = 10 pF	1.5	2.2		ns
$t_{d(a)}$	Aperture delay time			3		ns
$t_{J(a)}$	Aperture jitter			1.5		ps, rms
t_{dis}	Disable time, $\overline{OE}$ rising to Hi-Z			5	8	ns
t_{en}	Enable T\time, $\overline{OE}$ falling to valid data			5	8	ns

(1) All internal operations are performed at a 40-MHz clock rate.

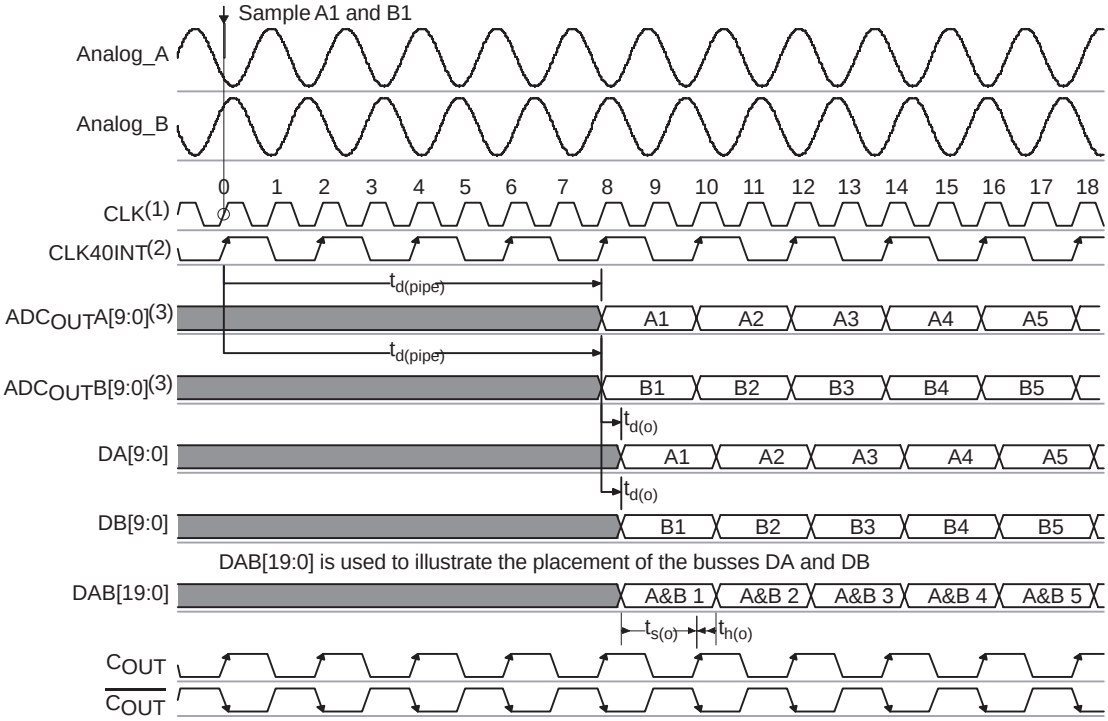
SERIAL INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	Maximum Clock Rate	20			MHz
t_{WH}	SCLK Pulse Width high	25			ns
t_{WH}	SCLK Pulse Width low	25			ns
$t_{SU(CS\_CK)}$	Setup Time, $\overline{CS}$ low Before First Negative SCLK Edge	5			ns
$t_{WH(CS)}$	$\overline{CS}$ HIGH Width	10			ns
$t_{SU(C16\_CK)}$	Setup Time, 16th Negative SCLK Edge before $\overline{CS}$ Rising Edge	5			ns
$t_{SU(D)}$	Setup Time, Data Ready Before SCLK Falling Edge	5			ns
$t_{SU(H)}$	Hold Time, Data Held Valid After SCLK Falling Edge	5			ns

TIMING OPTIONS

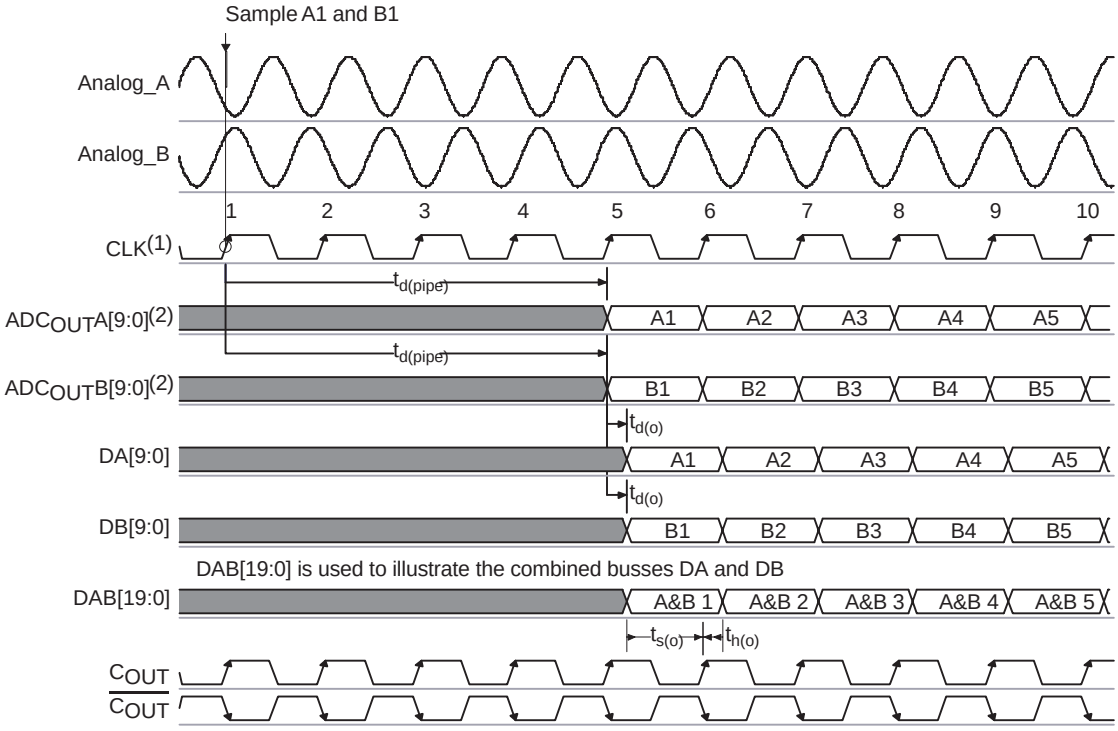
OPERATING MODE	MODE	SELB	TIMING DIAGRAM FIGURE
80-MHz Input Clock, Dual-Bus Output, C_{OUT} = 40 MHz	0	0	1
40-MHz Input Clock, Dual-Bus Output, C_{OUT} = 40 MHz	1	0	2
80-MHz Input Clock, Single-Bus Output, C_{OUT} = 40 MHz	0	1	3
80-MHz Input Clock, Single-Bus Output, C_{OUT} = 80 MHz	1	1	4

TIMING DIAGRAMS



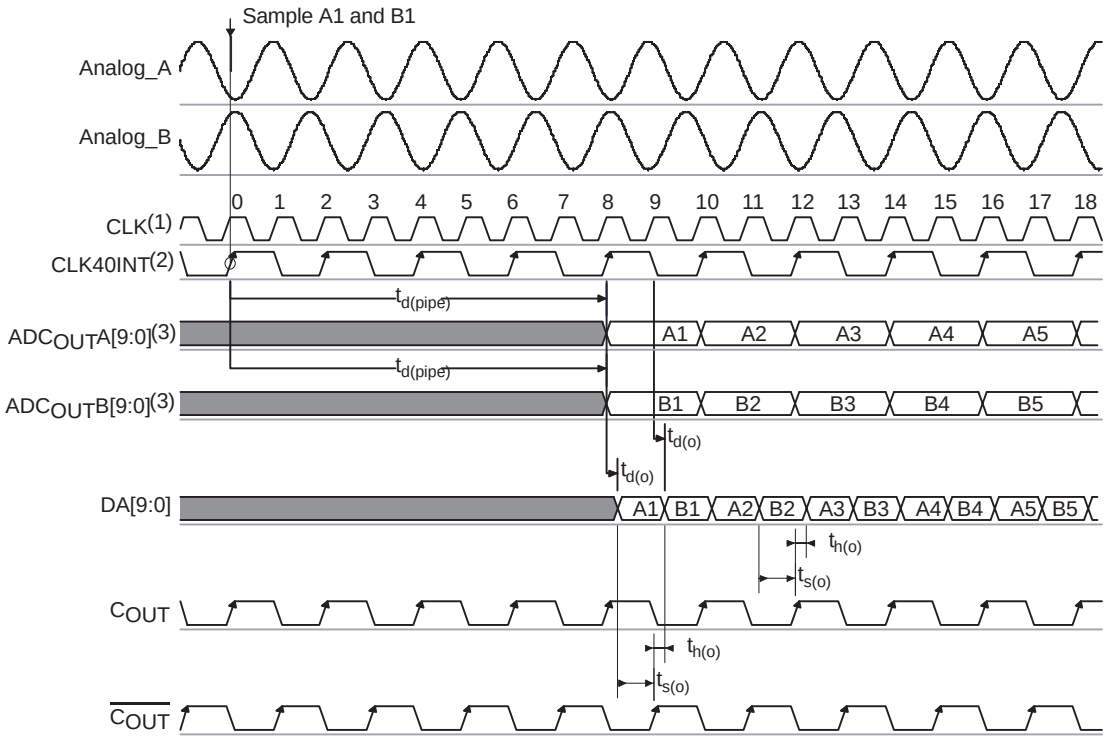
(1) In this option CLK = 80 MHz.
(2))CLK40INT refers to 40-MHz Internal Clock, per channel.
(3))Internal signal only.

Figure 1. Dual Bus Output—Option 1



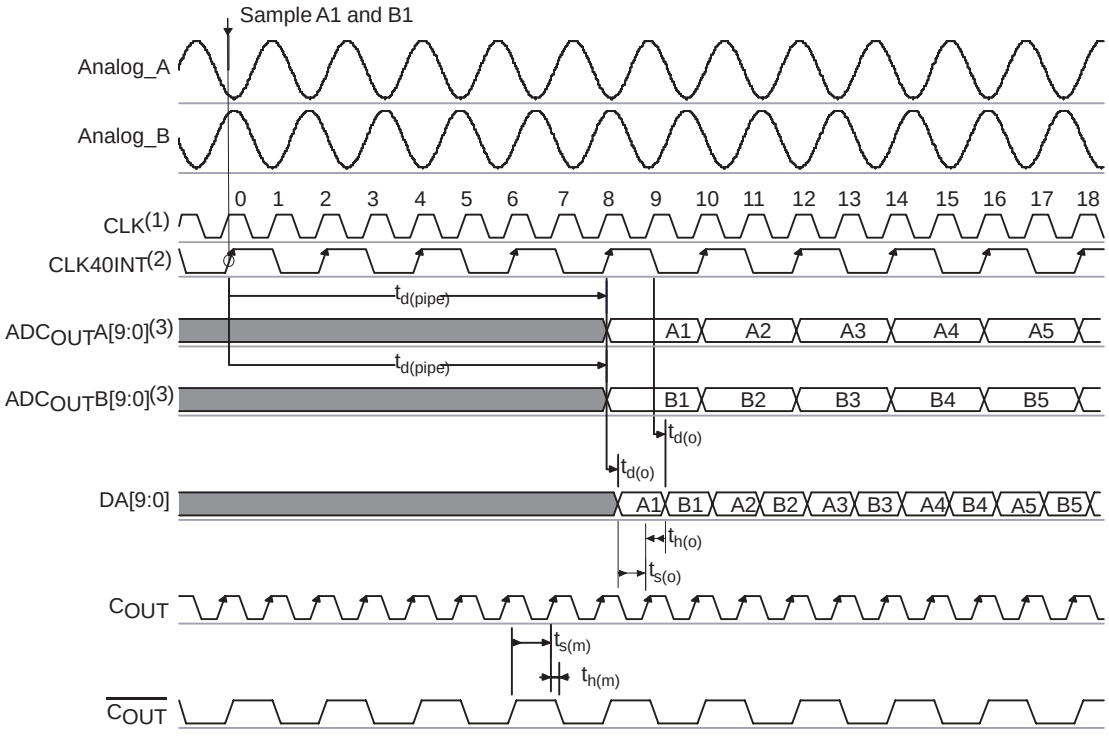
(1) In this option CLK = 40 MHz, per channel.
(2))Internal signal only.

Figure 2. Dual Bus Output—Option 2



(1) In this option CLK = 80 MHz, per channel.
(2)) CLK40INT refers to 40-MHz internal Clock, per channel.
(3)) Internal signal only.

Figure 3. Single Bus Output—Option 1



(1) In this option CLK = 80 MHz.
(2)) CLK40INT refers to 40-MHz internal Clock, per channel.
(3)) Internal signal only.

Figure 4. Single Bus Output—Option 2

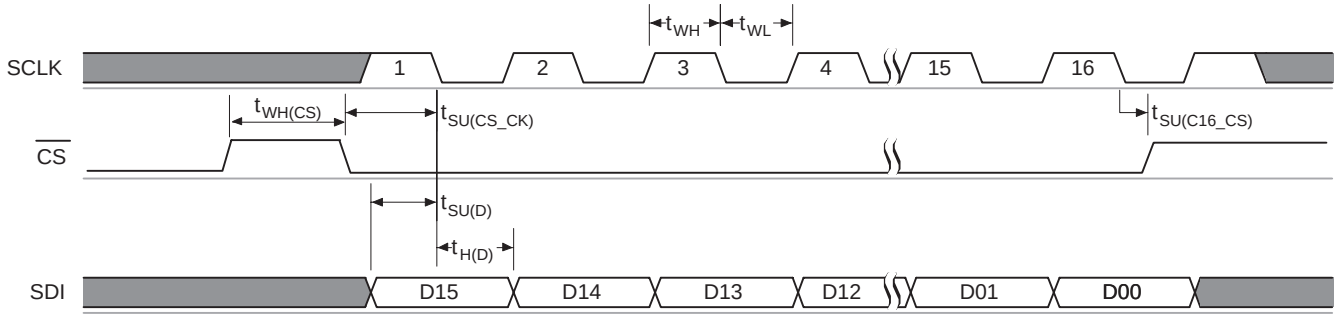


Figure 5. Serial Data Write

Table 1. Register Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Reserved	TWOS	MODE	SELB	PGA4 B	PGA3 B	PGA2 B	PGA1 B	PGA0 B	PGA4 A	PGA3 A	PGA2 A	PGA1 A	PGA0 A

Always write 0

Default (power up) condition for this register is all bits = 0. The user register is updated on either the first rising edge of SCLK after the 16th falling edge or $\overline{CS}$ rising, whichever comes first. Raising $\overline{CS}$ before 16 falling SCLK edges have been seen is an incomplete write error and no register update occurs. The PGA gain settings are resynchronized to the internal data conversion clock to avoid data glitches caused by changing gain settings while sampling the inputs.

PGA gain control data is applied to the PGAs on the second falling edge of the ADC sample clock (CLK40INT) after a successful register write. This resynchronization ensures that no analog glitch occurs even when SCLK is asynchronous to CLK.

Note that only the PGA data is resynchronized. The TWOS, MODE, and SELB register bits take effect immediately after a successful register write.

OUTPUT DATA FORMAT

The output data format can either be in Binary Two's Complement ouput mode or in unsigned binary mode, which affects both A and B channels.

TWOS − Binary Two's Complement Mode:

0 − Unsigned Binary

1 − Binary Two's Complement Output.

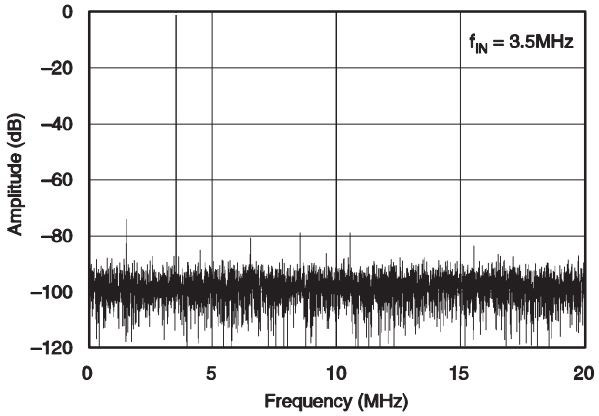
Table 2. PGA DB[0:4], 5−bit PGA gain code for channel A or B

GAIN (dB)	PGx4	PGx3	PGx2	PGx1	PGx0
0	0	0	0	0	0
0.5606	0	0	0	0	1
1.1599	0	0	0	1	0
1.6643	0	0	0	1	1
2.3806	0	0	1	0	0
2.8703	0	0	1	0	1
3.5218	0	0	1	1	0
4.0824	0	0	1	1	1
4.6817	0	1	0	0	0
5.1630	0	1	0	0	1
5.8451	0	1	0	1	0
6.3903	0	1	0	1	1
6.9807	0	1	1	0	0
7.6040	0	1	1	0	1
8.0497	0	1	1	1	0
8.7712	0	1	1	1	1
9.2831	1	0	0	0	0
9.8272	1	0	0	0	1
10.4078	1	0	0	1	0
11.0301	1	0	0	1	1
11.7005	1	0	1	0	0
12.0412	1	0	1	0	1
12.7970	1	0	1	1	0
13.2208	1	0	1	1	1
14.0944	1	1	0	0	0
14.5400	1	1	0	0	1
15.0666	1	1	0	1	0
15.5630	1	1	0	1	1
16.1623	1	1	1	0	0
16.7229	1	1	1	0	1
17.4181	1	1	1	1	0
18.0618	1	1	1	1	1

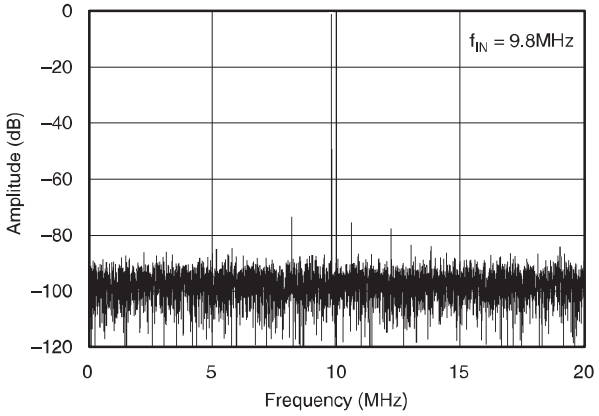
TYPICAL CHARACTERISTICS

At T_A = 25°C, AV_{DD} = DV_{DD} = DRV_{DD} = 3.3 V, f_{IN} = −0.5 dBFS, Internal Reference, f_{CLK} = 80 MHz, f_S = 40 MSPS, Differential Input Range = 2 Vp-p, 25-Ω series resistor, and 15-pF differential capacitor at A/B+ and A/B− inputs, unless otherwise noted.

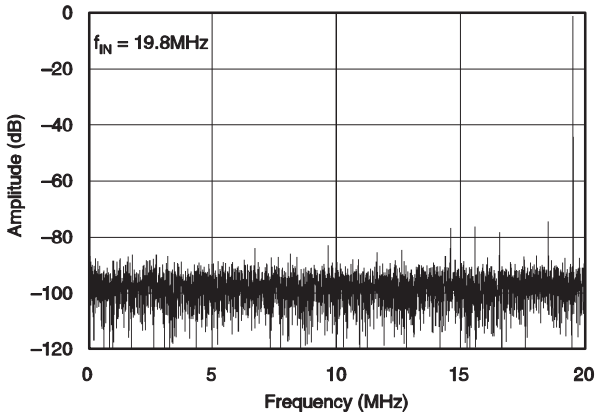
SPECTRAL PERFORMANCE



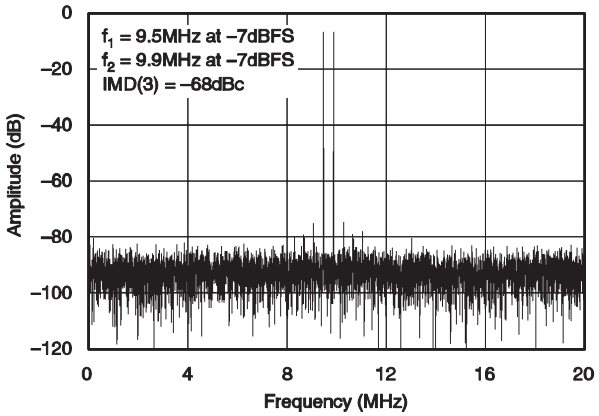
SPECTRAL PERFORMANCE



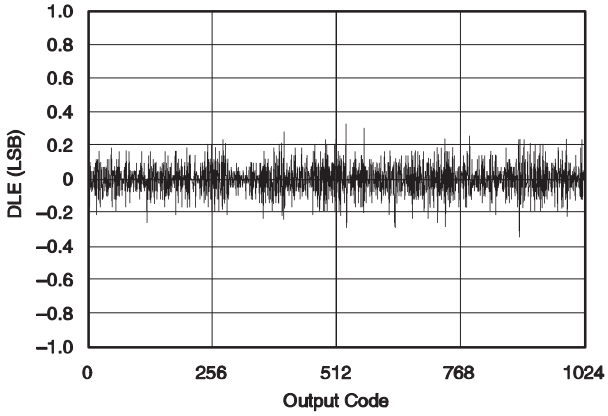
SPECTRAL PERFORMANCE



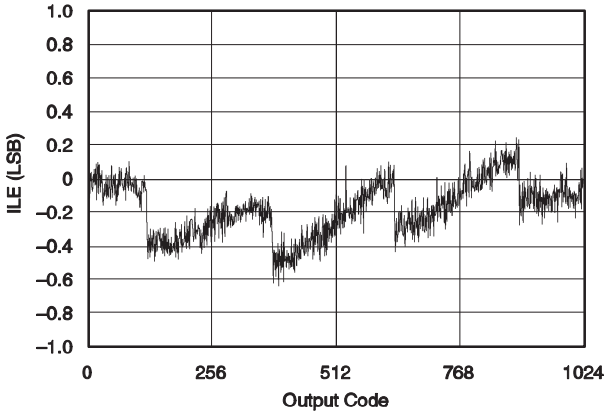
2-TONE INTERMODULATION DISTORTION



DIFFERENTIAL LINEARITY ERROR



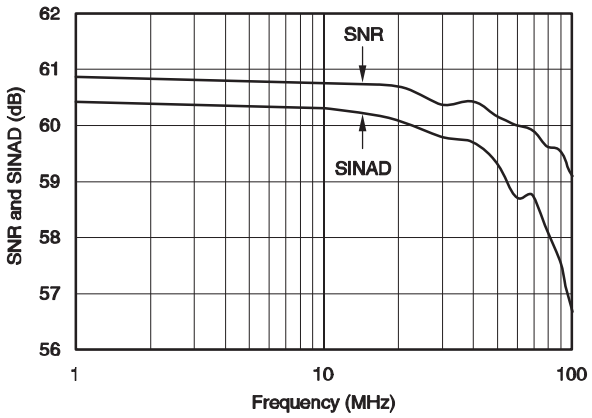
INTEGRAL LINEARITY ERROR



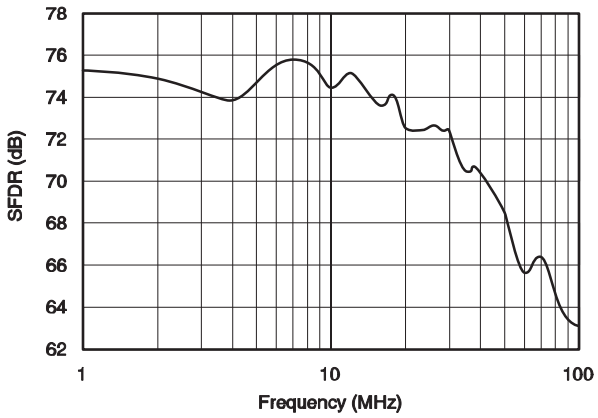
TYPICAL CHARACTERISTICS (Continued)

At T_A = 25°C, AV_{DD} = DV_{DD} = DRV_{DD} = 3.3 V, f_{IN} = −0.5 dBFS, Internal Reference, f_{CLK} = 80 MHz, f_S = 40 MSPS, Differential Input Range = 2 Vp-p, 25-Ω series resistor, and 15-pF differential capacitor at A/B+ and A/B− inputs, unless otherwise noted.

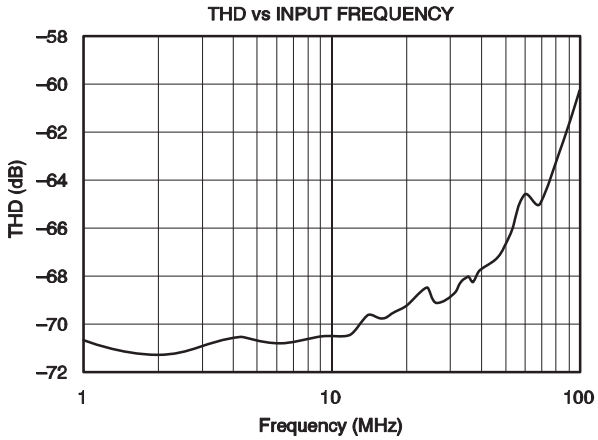
SNR AND SINAD vs INPUT FREQUENCY



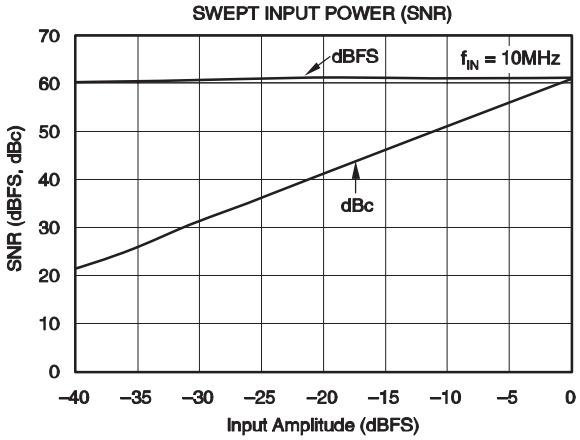
SFDR vs INPUT FREQUENCY



THD vs INPUT FREQUENCY



SWEPT INPUT POWER (SNR)



PRINCIPLE OF OPERATION

The ADS5204 implements a dual high-speed 10-bit, 40MSPS converter in a cost-effective CMOS process. The differential inputs on each channel are sampled simultaneously. Signal inputs are differential and the clock signal is single-ended. The clock signal is either 80 MHz or 40 MHz, depending on the device configuration set by the user. Powered from 3.3 V, the dual-pipeline design architecture ensures low-power operation and 10-bit resolution. The digital inputs are 3.3-V TTL/CMOS compatible. Internal voltage references are included for both bottom and top voltages. Alternatively, the user may apply externally generated reference voltages. In doing so, the input range can be modified to suit the application.

The ADC is a 5-stage pipelined ADC with four stages of fully-differential switched capacitor sub-ADC/MDAC pairs and a single sub-ADC in stage five. All stages deliver two bits of the final conversion result. A digital error correction is used to compensate for modest comparator offsets in the sub-ADCs.

SAMPLE-AND-HOLD AMPLIFIER

Figure 6 shows the internal SHA/SHPGA architecture. The circuit is balanced and fully differential for good supply noise rejection. The sampling circuit has been kept as simple as possible to obtain good performance for high-frequency input signals.

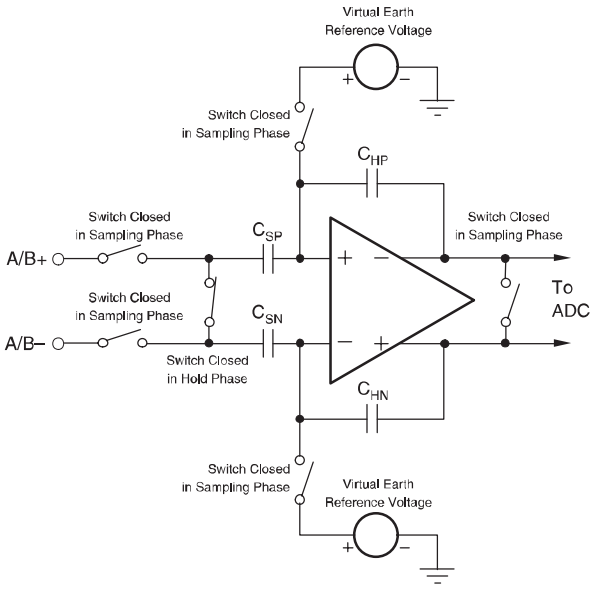


Figure 6. SHA/SHPGA Architecture

The analog input signal is sampled on capacitors C_{SP} and C_{SN} while the internal device clock is low. The sampled voltage is transferred to capacitors C_{HP} and C_{HN} and held on these while the internal device clock is high. The SHA can sample both single-ended and differential input signals.

The load presented to the AIN pin consists of the switched input sampling capacitor C_S (approximately 2 pF) and its various stray capacitances. A simplified equivalent circuit for the switched capacitor input is shown in Figure 7. The switched capacitor circuit is modeled as a resistor R_{IN}. f_{CLK} is the clock frequency, which is 40 MHz at full speed, and C_S is the sampling capacitor. The use of 25-Ω series resistors and a differential 15-pF capacitor at the A/B+ and A/B− inputs is recommended to reduce noise.

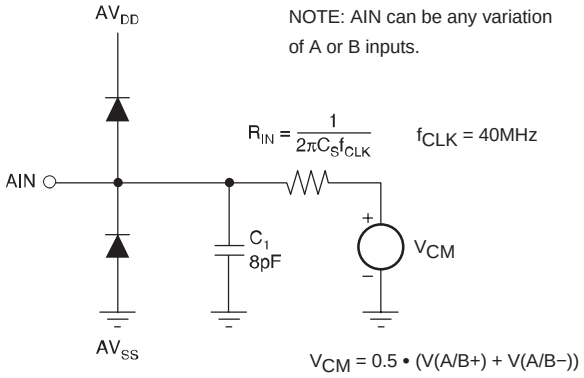


Figure 7. Equivalent Circuit for the Switched Capacitor Input

ANALOG INPUT, DIFFERENTIAL CONNECTION

The analog input of the ADS5204 is a differential architecture that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection will deliver the best performance from the converter. The analog inputs must not go below AV_{SS} or above AV_{DD}. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltages stay within the range AV_{SS} to AV_{DD}. It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. CML is made available to the user to help simplify circuit design. This output voltage source is not designed to be a reference or to be loaded but makes an excellent dc bias source and stays well within the analog input common-mode voltage range over temperature.

Table 3 lists the digital outputs for the corresponding analog input voltages.

Table 3. Output Format for Differential Configuration

DIFFERENTIAL INPUT	
V_{IN} = (A/B+) – (A/B−), REFT − REFB = 1 V, PGA = 0 dB	
ANALOG INPUT VOLTAGE	DIGITAL OUTPUT CODE
V_{IN} = +1 V	$3FF_H$
V_{IN} = 0	200_H
V_{IN} = −1 V	000_H

DC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved in various ways. Figure 8 gives an example where a single-ended signal is converted into a differential signal by using a fully differential amplifier such as the THS4141. The input voltage applied to V_{OCM} of the THS4141 shifts the output signal into the desired common-mode level. V_{OCM} can be connected to CML of the ADS5204, the common-mode level is shifted to $AV_{DD}/2$.

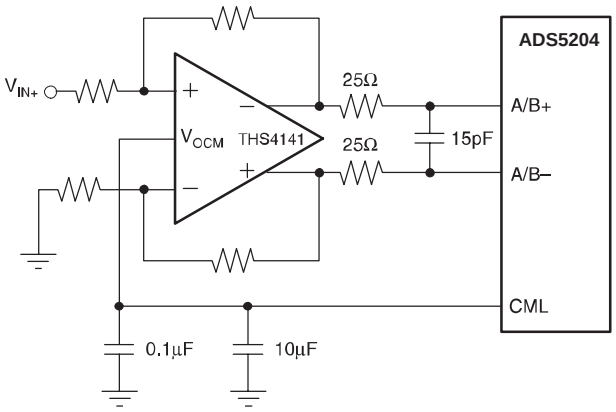


Figure 8. Single-Ended to Differential Conversion Using the THS4141

AC-COUPLED DIFFERENTIAL ANALOG INPUT CIRCUIT

Driving the analog input differentially can be achieved by using a transformer coupling, as illustrated in NO TAG. The center tap of the transformer is connected to the voltage source CML, which sets the common-mode voltage to $AV_{DD}/2$. No buffer is required at the output of CML since the circuit is balanced and no current is drawn from CML.

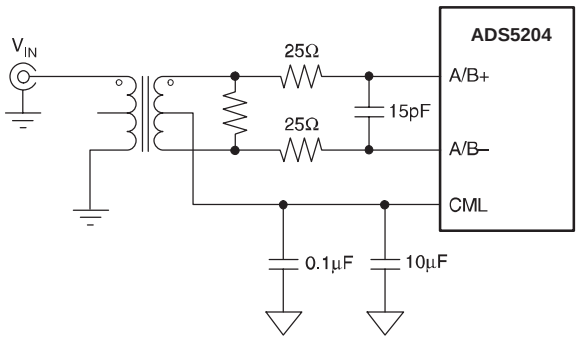


Figure 9. AC-Coupled Differential Input with Transformer

ANALOG INPUT, SINGLE-ENDED CONFIGURATION

For a single-ended configuration, the input signal is applied to only one of the two inputs. The signal applied to the analog input must not go below AV_{SS} or above AV_{DD}. The inputs can be biased with any common-mode voltage provided that the minimum and maximum input voltage stays within the range AV_{SS} to AV_{DD}. It is recommended to bias the inputs with a common-mode voltage around $AV_{DD}/2$. This can be accomplished easily with the output voltage source CML, which is equal to $AV_{DD}/2$. An example for this is shown in Figure 10.

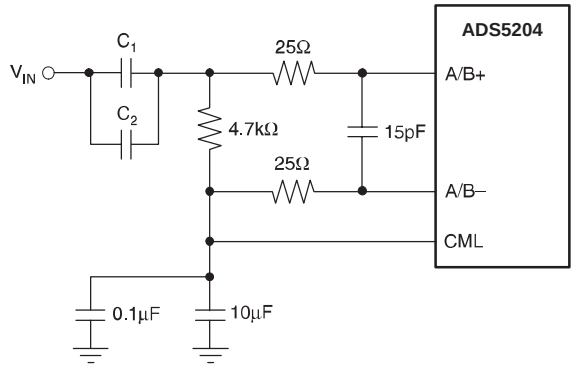


Figure 10. AC-Coupled, Single-Ended Configuration

The signal amplitude to achieve full-scale is 2 Vp-p. The signal, which is applied at A/B+ is centered at the bias voltage. The input A/B− is also centered at the bias voltage. The CML output is connected via a 4.7-kΩ resistor to bias the input signal. There is a direct dc-coupling from CML to A/B− while this input is ac-decoupled through the 10-µF and 0.1-µF capacitors. The decoupling minimizes the coupling of A/B+ into the A/B− path.

Table 4 lists the digital outputs for the corresponding analog input voltages.

Table 4. Output Format for Single-Ended Configuration

SINGLE-ENDED INPUT, REFT − REFB = 1V, PGA = 0dB	
ANALOG INPUT VOLTAGE	**DIGITAL OUTPUT CODE**
$V(A/B+) = V_{CML} + 1V$	$3FF_H$
$V(A/B+) = V_{CML}$	200_H
$V(A/B+) = V_{CML} - 1V$	000_H

REFERENCE TERMINALS

The ADS5204's input range is determined by the voltages on its REFB and REFT pins. The ADS5204 has an internal voltage reference generator that sets the ADC reference voltages REFB = 1 V and REFT = 2 V. The internal ADC references must be decoupled to the PCB AV_{SS} plane. The recommended decoupling scheme is shown in Figure 11. The common-mode reference voltages should be 1.5 V for best ADC performance.

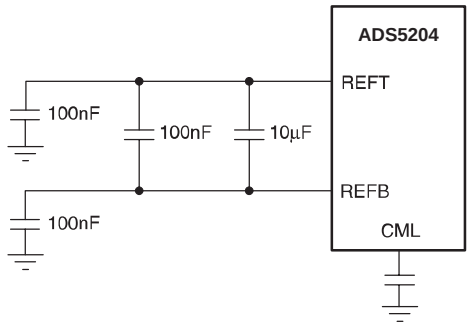


Figure 11. Recommended External Decoupling for the Internal ADC Reference

External ADC references can also be chosen. The ADS5204 internal references must be disabled by tying PWDN_REF high before applying the external reference sources to the REFT and REFB pins. The common-mode reference voltages should be 1.5 V for best ADC performance.

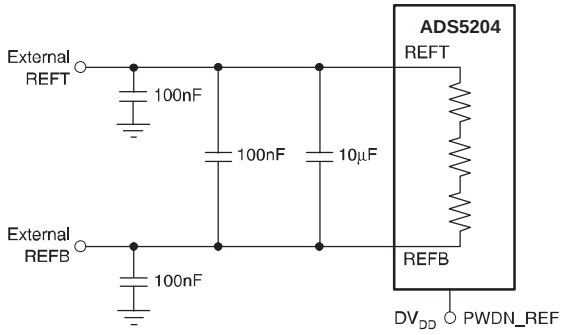


Figure 12. External ADC Reference Configuration

DIGITAL INPUTS

Digital inputs are CLK, SCLK, SDI, $\overline{CS}$, STDBY, PWDN_REF, and $\overline{OE}$. These inputs don't have a pulldown resistor to ground, therefore, they should not be left floating.

The CLK signal at high frequencies should be considered as an 'analog' input. CLK should be referenced to AV_{DD} and AV_{SS} to reduce noise coupling from the digital logic. Overshoot/undershoot should be minimized by proper termination of the signal close to the ADS5204. An important cause of performance degradation for a high-speed ADC is clock jitter. Clock jitter causes uncertainty in the sampling instant of the ADC, in addition to the inherent uncertainty on the sampling instant caused by the part itself, as specified by its aperture jitter. There is a theoretical relationship between the frequency (f) and resolution (2^N) of a signal that needs to be sampled on one hand, and on the other hand the maximum amount of aperture error dt_{max} that is tolerable. It is given by the following relation:

$$dt_{max} = 1/[\pi\ f\ 2^{(N+1)}]$$

As an example, for a 10-bit converter with a 20MHz input, the jitter needs to be kept less than 7.8ps in order not to have changes in the LSB of the ADC output due to the total aperture error.

DIGITAL OUTPUTS

The output of ADS5204 is an unsigned binary or Binary Two's Complement code. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10 pF is recommended) to ensure best performance. Higher output loading causes higher dynamic output currents and can, therefore, increase noise coupling into the part's analog front end. To drive higher loads, the use of an output buffer is recommended.

When clocking output data from ADS5204, it is important to observe its timing relation to C_{OUT}. See the Timing section for detailed information on the pipeline latency in the different modes.

For safest system timing, C_{OUT} and $\overline{C_{OUT}}$ should be used to latch the output data (see Figure 1 through Figure 4). In Figure 4, $\overline{C_{OUT}}$ can be used by the receiving device to identify whether the data presently on the bus is from channel A or B.

LAYOUT, DECOUPLING, AND GROUNDING RULES

Proper grounding and layout of the PCB on which the ADS5204 is populated is essential to achieve the stated performance. It is advised to use separate analog and digital ground planes that are spliced underneath the IC. The ADS5204 has digital and analog pins on opposite sides of the package to make this easier. Since there is no connection internally between analog and digital grounds, they have to be joined on the PCB. It is advised to do this at one point in close proximity to the ADS5204.

As for power supplies, separate analog and digital supply pins are provided on the part (AV_{DD}/DV_{DD}). The supply to the digital output drivers is kept separate as well (DRV_{DD}). Lowering the voltage on this supply to 3 V instead of the nominal 3.3 V improves performance because of the lower switching noise caused by the output buffers.

Due to the high sampling rate and switched-capacitor architecture, the ADS5204 generates transients on the supply and reference lines. Proper decoupling of these lines is, therefore, essential.

SERIAL INTERFACE

A falling edge on $\overline{CS}$ enables the serial interface, allowing the 16-bit control register date to be shifted (MSB first) on subsequent falling edges of SCLK. The data is loaded into the control register on the first rising edge of SCLK after its 16th falling edge or $\overline{CS}$ rising, whichever occurs first. $\overline{CS}$ rising before 16 falling SCLK edges have been counted is an error and the control register will not be updated.

The maximum update rate is:

$$f_{UPDATEMAX} = \frac{f_{SCLK}}{16} = \frac{20MHz}{16} = 1.25MHz$$

NOTES

1. Integral Nonlinearity (INL)—Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full-scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as a level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two endpoints.

2. Differential Nonlinearity (DNL)—An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test [i.e. (last transition level − first transition level)/(2^n − 2)]. Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1LSB ensures no missing codes.

3. Zero and Full-Scale Error—Zero error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 0 to code 1. The ideal voltage level is determined by adding the voltage corresponding to 1/5 LSB to the bottom reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

Full-scale error is defined as the difference in analog input voltage—between the ideal voltage and the actual voltage—that switches the ADC output from code 1022 to code 1023. The ideal voltage level is determined by subtracting the voltage corresponding to 1. 5LSB from the top reference level. The voltage corresponding to 1 LSB is found from the difference of top and bottom references divided by the number of ADC output levels (1024).

4. Analog Input Bandwidth—The analog input bandwidth is defined as the max. frequency of a 1-dBFS input sine that can be applied to the device for which an extra 3-dB attenuation is observed in the reconstructed output signal.

5. Output Timing—Output timing $t_{d(o)}$ is measured from the 1.5-V level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10 pF. Output hold time $t_{h(o)}$ is measured from the 1.5-V level of the C_{OUT} input rising edge to the 10%/90% level of the digital output. The digital output is load is not less than 2 pF. Aperture delay $t_{d(A)}$ is measured from the 1.5-V level of the CLK input to the actual sampling instant.

The $\overline{OE}$ signal is asynchronous. $\overline{OE}$ timing t_{dis} is measured from the $V_{IH(MIN)}$ level of $\overline{OE}$ to the high-impedance state of the output data. The digital output load is not higher than 10 pF. $\overline{OE}$ timing t_{en} is measured from the $V_{IL(MAX)}$ level of $\overline{OE}$ to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10 pF.

6. Pipeline Delay (latency)—The number of clock cycles between conversion initiation on an input sample and the corresponding output data being made available from the ADC pipeline. Once the data pipeline is full, new valid output data is provided on every clock cycle. The first valid data is available on the output pins after the latency time plus the output delay time $t_{d(o)}$ through the digital output buffers. Note that a minimum $t_{d(o)}$ is not assured because data can transition before or after a CLK edge. It is possible to use CLK for latching data, but at the risk of the prop delay varying over temperature, causing data to transition one CLK cycle

earlier or later. The recommended method is to use the latch signals C_{OUT} and $\overline{C_{OUT}}$ which are designed to provide reliable setup and hold times with respect to the data out.

7. Wake-Up Time—Wake-up time is from the power-down state to accurate ADC samples being taken and is specified for external reference sources applied to the device and an 80-MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, bias generator, SHAs, and ADCs.

8. Power-Up Time—Power-up time is from the power-down state to accurate ADC samples being taken with an 80-MHz clock applied at the time of release of STDBY. Cells that need to power up are the bandgap, internal reference circuit, bias generator, SHAs, and ADCs.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS5204IPFBRG4Q1	Obsolete	Production	TQFP (PFB) | 48	-	-	Call TI	Call TI	-40 to 85	AZ5204Q
ADS5204IPFBRQ1	Obsolete	Production	TQFP (PFB) | 48	-	-	Call TI	Call TI	-40 to 85	AZ5204Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

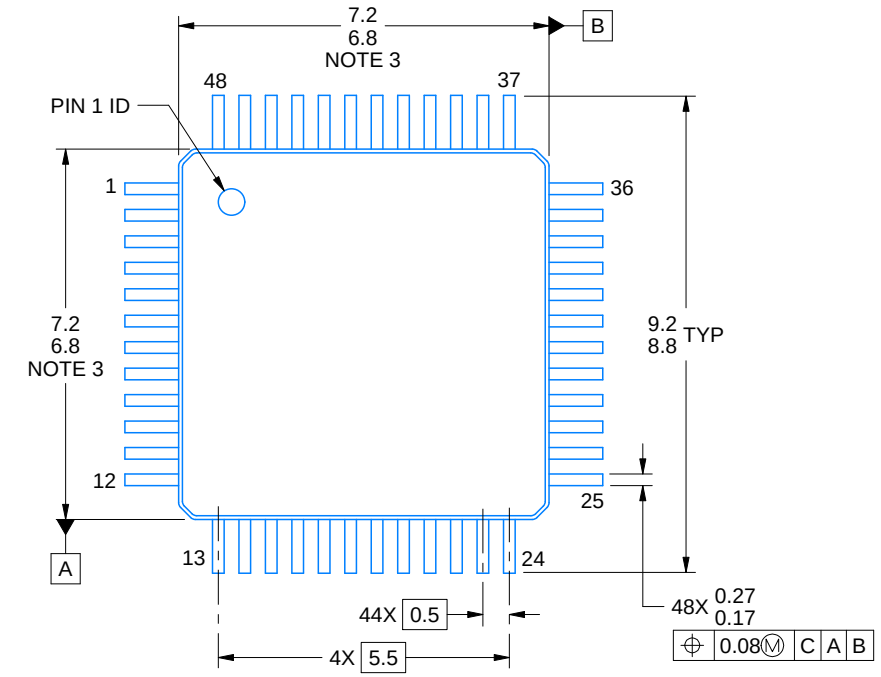
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

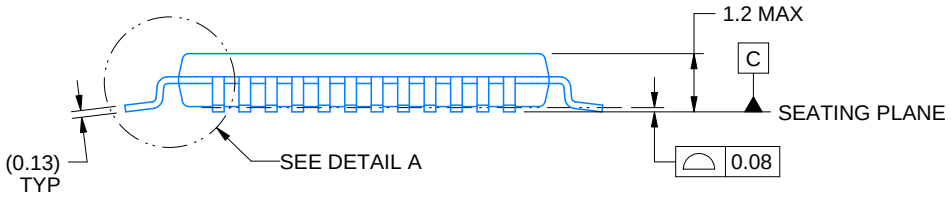
PACKAGE OUTLINE

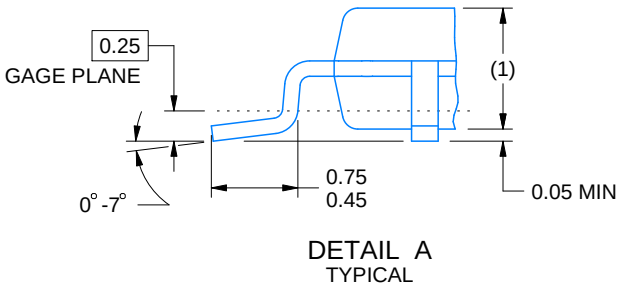
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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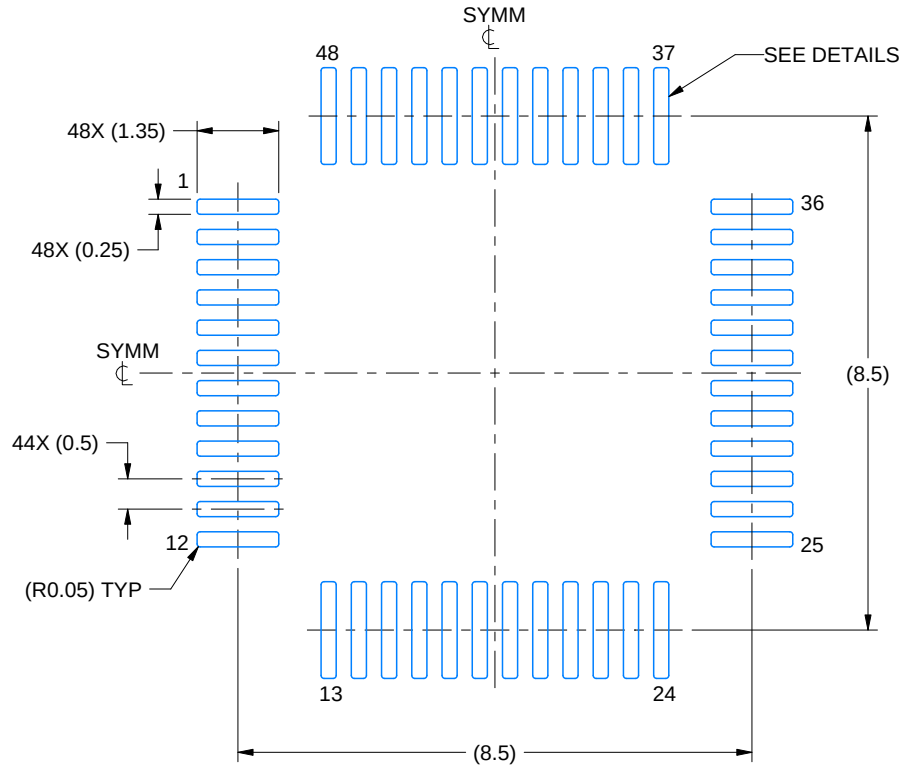
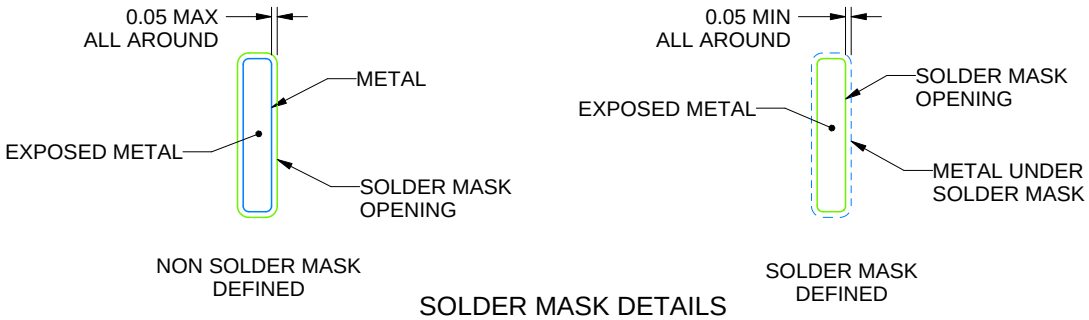
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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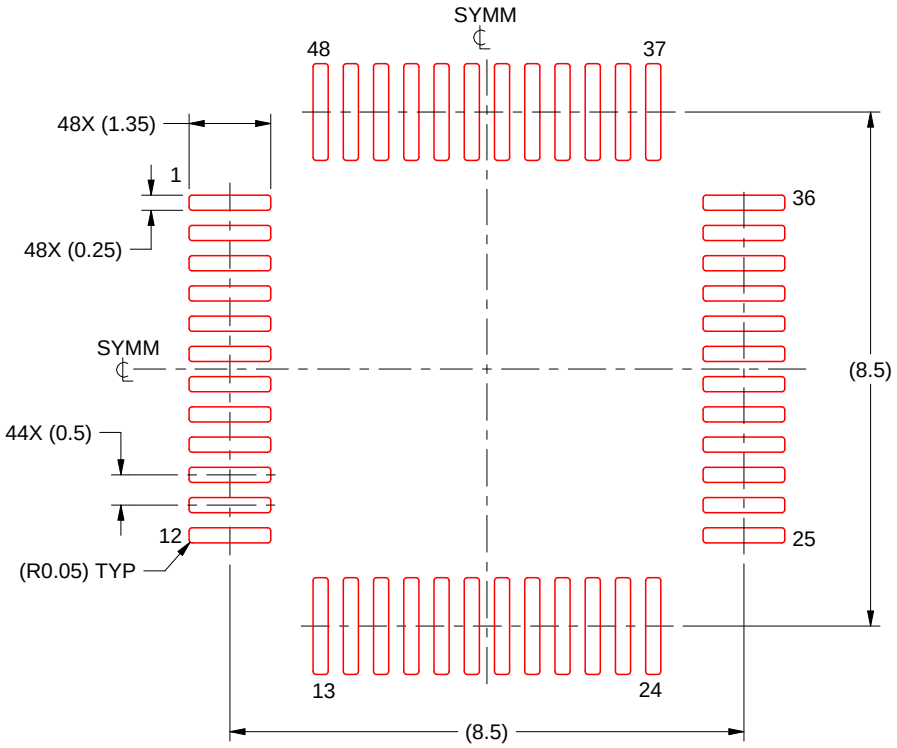
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025