bq2005

Fast-Charge IC for Dual-Battery Packs

Features

- Sequential fast charge and conditioning of two NiCd or NiMH nickel cadmium or nickel-metal hydride battery packs
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off and pulse-trickle charging

General Description

The bq2005 Fast-Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device for sequential charge management in dual battery pack applications.

Integration of closed-loop current control circuitry allows the bq2005 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated dis-charge-before-charge allows bq2005-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2005 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2005 may alternatively be used to gate an externally regulated charging current.

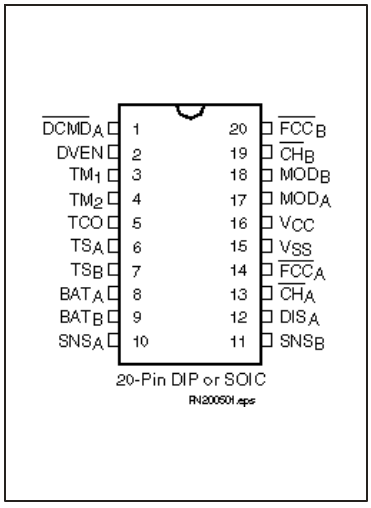
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

Pin Connections



Pin Names

$\overline{DCMD}_A$	Discharge command input, battery A
DVEN	DV enable
TM_1	Timer mode select 1
TM_2	Timer mode select 2
TCO	Temperature cut-off
TS_A, TS_B	Temperature sense input, battery A/B
BAT_A, BAT_B	Battery voltage input, battery A/B
SNSA, SNSB	Sense resistor input, battery A/B
DIS_A	Discharge control output, battery A
$\overline{CH}_A$, $\overline{CH}_B$	Charge status output, battery A/B
$\overline{FCC}_A$, $\overline{FCC}_B$	Fast charge complete output, battery A/B
V_{SS}	System ground
V_{CC}	5.0V ±10% power
MOD_A, MOD_B	Charge current control output, battery A/B

Pin Descriptions

$DCMD_A$ **Discharge-before-charge control input, battery A**

$\overline{DCMD}_A$ controls the discharge-before-charge function of the bq2005. A negative-going pulse on $\overline{DCMD}_A$ initiates a discharge to EDV followed by a charge if conditions allow. By tying $\overline{DCMD}_A$ to ground, automatic discharge-before-charge is enabled on every new charge cycle start.

DVEN **-ΔV enable input**

This input enables/disables -ΔV charge termination. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. The state of DVEN may be changed at any time.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, -ΔV hold-off time, and that enhance/disable top-off. See Table 2.

TCO **Temperature cutoff threshold input**

Input to set maximum allowable battery temperature. If the potential between TS_A and SNS_A or TSB and SNS_B is less than the voltage at the TCO input, then fast charge or top-off charge is terminated for the corresponding battery pack.

TS_A, TS_B **Temperature sense inputs**

Input, referenced to SNS_A or SNS_B, respectively, for an external thermistor monitoring battery temperature.

BAT_A, BAT_B **Voltage inputs**

The battery voltage sense input, referenced to $SNS_{A,B}$, respectively. This is created by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

SNS_A, SNS_B **Charging current sense inputs,**

$SNS_{A,B}$ controls the switching of $MOD_{A,B}$ based on the voltage across an external sense resistor in the current path of the battery. SNS is the reference potential for the TS and BAT pins. If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

DIS_A **Discharge control output**

Push-pull output used to control an external transistor to discharge battery A before charging.

$\overline{CH}_A$, $\overline{CH}_B$ **Charge status outputs**

Push-pull outputs indicating charging status for batteries A and B, respectively. See Figure 1 and Table 2.

$\overline{FCC}_A$, $\overline{FCC}_B$ **Fast charge complete outputs**

Open-drain outputs indicating fast charge complete for batteries A and B, respectively. See Figure 1 and Table 2.

MOD_A, MOD_B **Charge current control outputs**

$MOD_{A,B}$ is a push-pull output that is used to control the charging current to the battery. $MOD_{A,B}$ switches high to enable charging current to flow and low to inhibit charging current flow to batteries A and B, respectively.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

Vss **Ground**

Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2005.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, $BAT_{A,B}$, must be divided down to between $0.95 * V_{CC}$ and $0.475 * V_{CC}$ for proper operation. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

Note: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1MΩ.

A ground-referenced negative temperature coefficient thermistor placed in proximity to the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at $TS_{A,B}$ is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1. Both the $BAT_{A,B}$ and $TS_{A,B}$ inputs are referenced to $SNS_{A,B}$, so the signals used inside the IC are:

$$V_{BAT(A,B)} - V_{SNS(A,B)} = V_{CELL(A,B)}$$

and

$$V_{TS(A,B)} - V_{SNS(A,B)} = V_{TEMP(A,B)}$$

Discharge-Before-Charge

The $\overline{DCMD}_A$ input is used to command discharge-before-charge via the DIS_A output. Once activated, DIS_A becomes active (high) until V_{CELL} falls below V_{EDV} where:

$$V_{EDV} = 0.475 * V_{CC} \pm 30mV$$

at which time DIS_A goes low and a new fast charge cycle begins.

The $\overline{DCMD}_A$ input is internally pulled up to V_{CC} (its inactive state). Leaving the input unconnected, therefore, results in disabling discharge-before-charge. A negative going pulse on $\overline{DCMD}_A$ initiates discharge-before-charge at any time regardless of the current state of the bq2005. If $\overline{DCMD}_A$ is tied to V_{SS}, discharge-before-charge will be the first step in all newly started charge cycles.

Starting A Charge Cycle

A new charge cycle is started by (see Figure 2):

1. V_{CC} rising above 4.5V
2. V_{CELL} falling through the maximum cell voltage, V_{MCV} where:

$$V_{MCV} = 0.95 * V_{CC} \pm 30mV$$

If $\overline{DCMD}_A$ is tied low, a discharge-before-charge will be executed as the first step of the new charge cycle. Otherwise, pre-charge qualification testing will be the first step.

The battery must be within the configured temperature and voltage limits before fast charging begins.

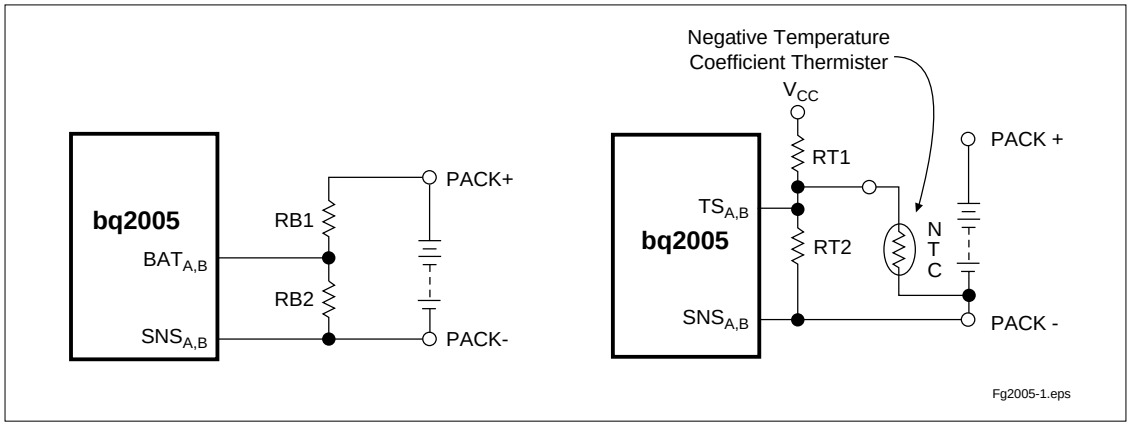


Figure 1. Voltage and Temperature Monitoring

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$. The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to $0.4 * V_{CC}$.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The $MOD_{A,B}$ output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditions are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the five possible termination conditions:

Delta temperature/delta time ($\Delta T/\Delta t$)

Negative delta voltage ($-\Delta V$)

Maximum voltage

Maximum temperature

Maximum time

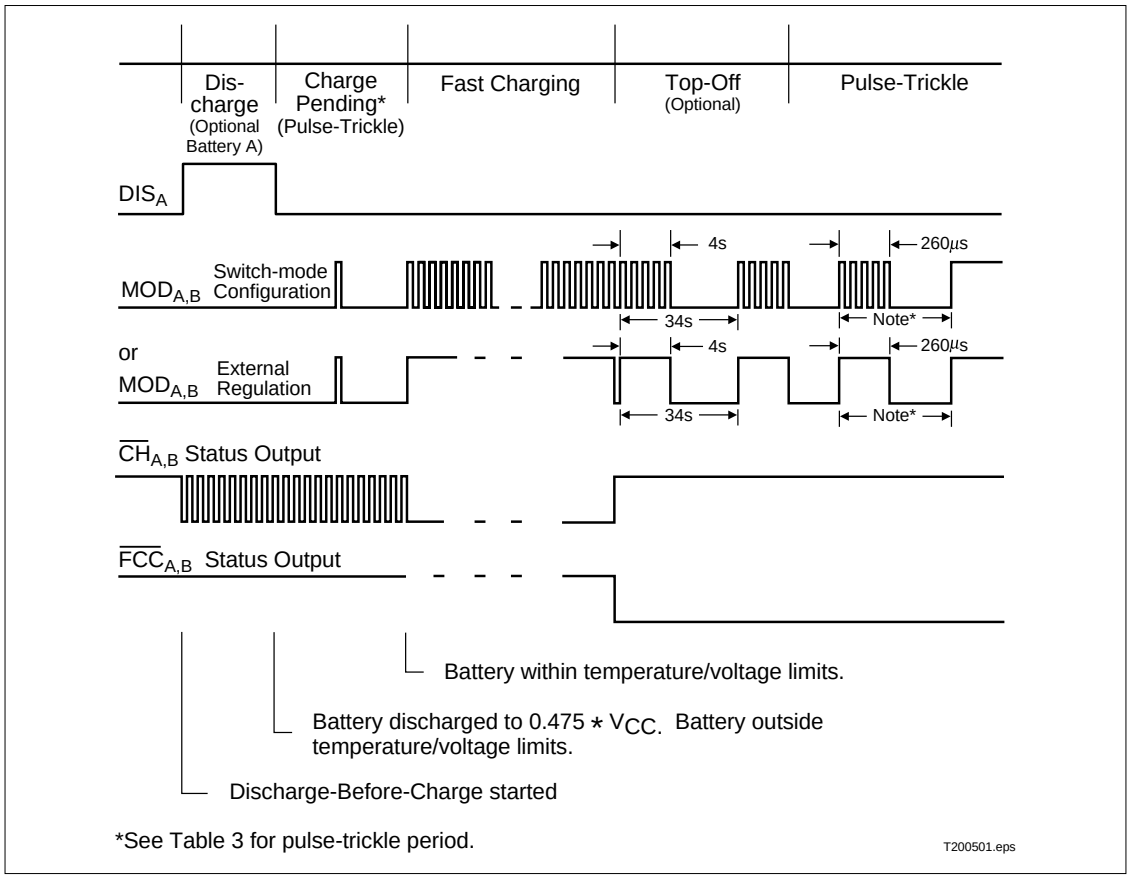


Figure 2. Charge Cycle Phases

Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast-Charge and Top-Off Time Limits	Typical -ΔV/MCV Hold-Off Time (seconds)	Top-Off Rate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

- V Termination

If the DVEN input is high, the bq2005 samples the voltage at the BAT pin once every 34s. If V_{CELL} is lower than any previously measured value by 12mV ±4mV, fast charge is terminated. The -ΔV test is valid in the range $V_{MCV} - (0.2 * V_{CC}) < V_{CELL} < V_{MCV}$.

Voltage Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. ΔT/Δt, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

T/ t Termination

The bq2005 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above $V_{MCV,}$ CHG goes high (the LED goes off) immediately. If the bq2005 is not in the voltage hold-off period, fast charging also ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1s (maximum), the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of $t_{MCV,}$ the bq2005 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold $V_{TCO.}$ Charge will also be terminated if V_{TEMP} rises above the minimum temperature fault threshold, $V_{LTF,}$ after fast charge begins.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other

battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM_1 and TM_2 input pins. (See Table 2.) During top-off, the CC pin is modulated at a duty cycle of 4s active for every 30s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS}.

Charge Status Indication

Charge status is indicated by the CHG output. The state of the CHG output in the various charge cycle phases is shown in Figure 4 and illustrated in Figure 2.

Temperature status is indicated by the TEMP output. TEMP is in the high state whenever V_{TEMP} is within the temperature window defined by the V_{LTF} and V_{HTF} temperature limits, and is low when the battery temperature is outside these limits.

In all cases, if V_{CELL} exceeds the voltage at the MCV pin, both CHG and TEMP outputs are held high regardless of other conditions. CHG and TEMP may both be used to directly drive an LED.

Pack Sequencing

If both batteries A and B are present when a new charge cycle is started, the charge cycle starts on battery B and B remains the active channel until fast charge termination. Then battery A will be fast charged, followed by a top-off phase on B (if selected), a top-off phase on A (if selected), and then maintenance charging on both. If only battery A is present, the charge cycle begins on A and continues until fast charge termination even if a battery is inserted in channel B in the meantime. A new battery insertion in channel B while A is in the top-off phase terminates top-off on A and begins a new charge cycle on B. If A is configured for or commanded to discharge-before-charge, the discharge may take place while channel B is the active charging channel. When the discharge is complete, if B is still the active channel battery A enters the Charge Pending state until A becomes the active channel.

Charge Current Control

The bq2005 controls charge current through the $MOD_{A,B}$ output pin. The current control circuitry is designed to support implementation of a constant-current switching regulator or to gate an externally regulated current source.

When used in switch mode configuration, the nominal regulated current is:

$$I_{REG} = 0.225V/R_{SNS}$$

Charge current is monitored at the $SNS_{A,B}$ input by the voltage drop across a sense resistor, R_{SNS}, between the low side of the battery pack and ground. R_{SNS} is sized to provide the desired fast charge current.

If the voltage at the $SNS_{A,B}$ pin is less than V_{SNSLO}, the $MOD_{A,B}$ output is switched high to pass charge current to the battery.

When the $SNS_{A,B}$ voltage is greater than V_{SNSHI}, the $MOD_{A,B}$ output is switched low—shutting off charging current to the battery.

$$V_{SNSLO} = 0.04 * V_{CC} \pm 25mV$$

$$V_{SNSHI} = 0.05 * V_{CC} \pm 25mV$$

When used to gate an externally regulated current source, the $SNS_{A,B}$ pin is connected to V_{SS}, and no sense resistor is required.

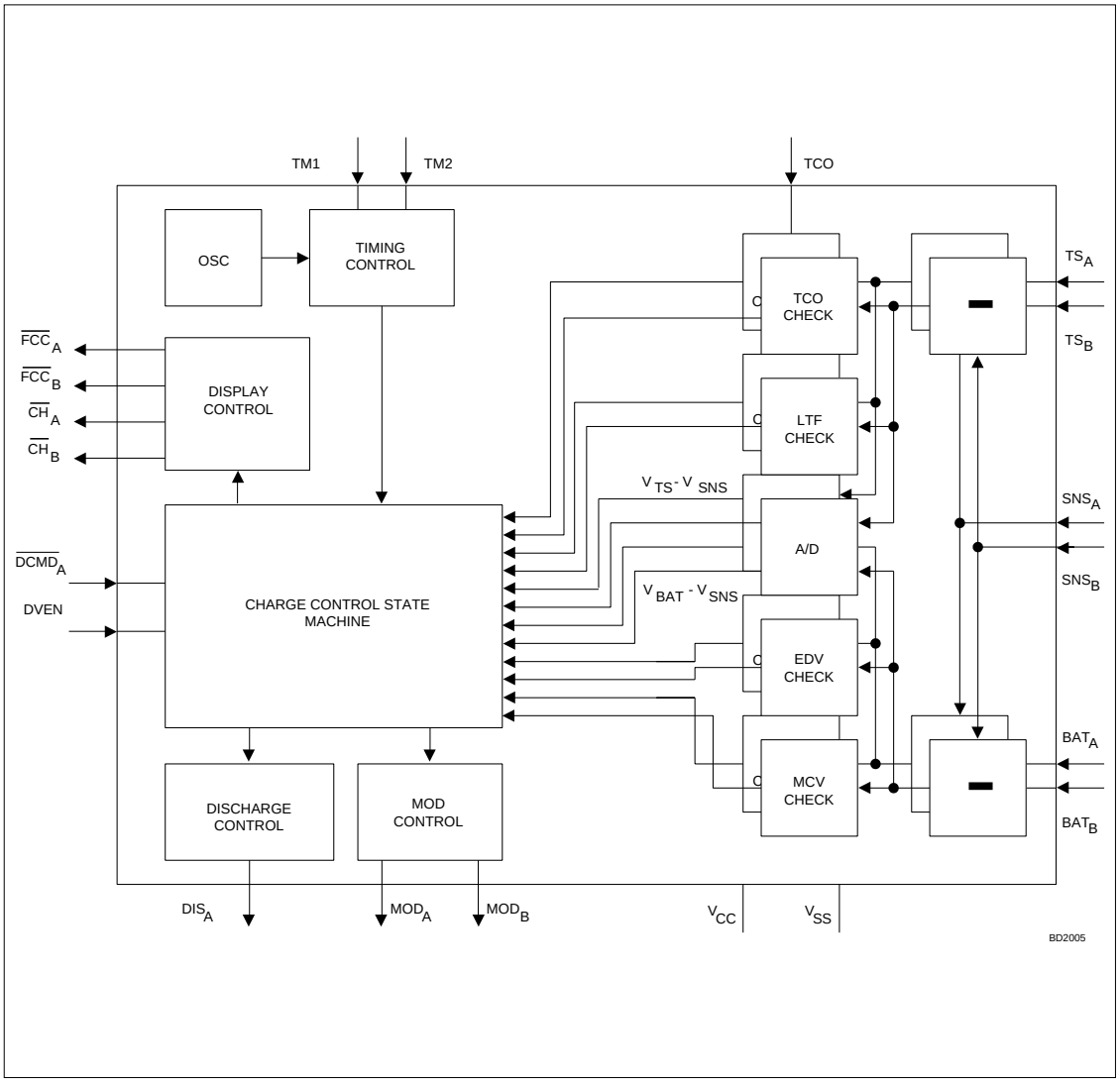


Figure 3. Block Diagram

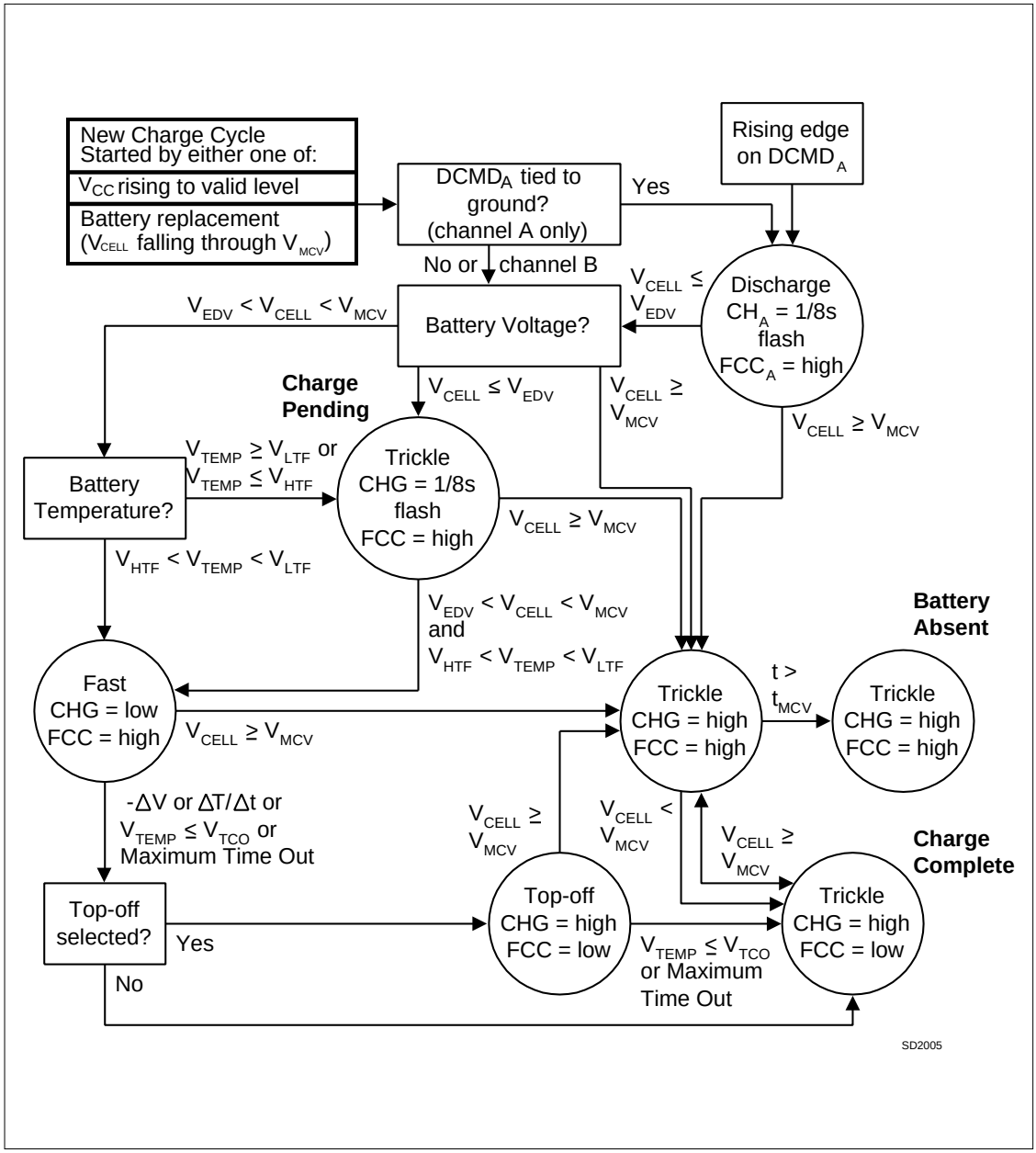


Figure 4. State Diagram

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10s max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = Low	$0.05 * V_{CC}$	±0.025	V	
V_{SNSLO}	Low threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = High	$0.04 * V_{CC}$	±0.010	V	
V_{LTF}	Low-temperature fault	$0.4 * V_{CC}$	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	$(1/4 * V_{LTF}) + (3/4 * V_{TCO})$	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	$0.475 * V_{CC}$	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	$0.95 * V_{CC}$	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	16	±4	mV	
$-\Delta V$	BAT input change for $-\Delta V$ detection	12	±4	mV	

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	0.2 * V_{CC}	-	0.4 * V_{CC}	V	
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}_A$, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}_A$, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS_A, $MOD_{A,B}$, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS_A, $\overline{FCC}_{A,B}$, $\overline{CH}_{A,B}$, $MOD_{A,B}$, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	1.0	3.0	mA	Outputs unloaded
I_{OH}	DIS_A, $MOD_{A,B}$ source	-5.0	-	-	mA	@V_{OH} = V_{CC} - 0.5V
I_{OL}	$\overline{DIS}_A$, $\overline{FCC}_{A,B}$, $MOD_{A,B}$, $\overline{CH}_{A,B}$ sink	5.0	-	-	mA	@V_{OL} = V_{SS} + 0.5V
I_L	Input leakage	-	-	±1	µA	DVEN, V = V_{SS} to V_{CC}
		-	-	-400	µA	$\overline{DCMD}_A$, V = V_{SS}
I_{IL}	Logic input low source	-	-	70.0	µA	TM_1, TM_2, V = V_{SS} to V_{SS} + 0.3V
I_{IH}	Logic input high source	-70.0	-	-	µA	TM_1, TM_2, V = V_{CC} - 0.3V to V_{CC}
I_{IZ}	TM_1, TM_2 tri-state open detection	-2.0	-	2.0	µA	TM_1, TM_2 should be left disconnected (floating) for Z logic input state.
I_{BAT}	Input current to $BAT_{A,B}$ when battery is removed	-	-	-20	µA	V_{CC} = 5.0V; T_A = 25°C; input should be limited to this current when input exceeds V_{CC}.

Note: All voltages relative to V_{SS}, except as noted.

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$R_{BATA,B}$	Battery A/B input impedance	50	-	-	MΩ
$R_{TSA,B}$	$TS_{A,B}$ input impedance	50	-	-	MΩ
R_{TCO}	TCO input impedance	50	-	-	MΩ
$R_{SNSA,B}$	$SNS_{A,B}$ input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{PW}	Pulse width for $\overline{DCMD}_A$, pulse command	1	-	-	µs	Pulse start for discharge-before-charge
d_{FCV}	Time base variation	-16	-	16	%	V_{CC} = 4.5V to 5.5V
t_{REG}	MOD output regulation frequency	-	-	300	kHz	
t_{MCV}	Maximum voltage termination time limit	-	-	1	s	Time limit to distinguish battery removed from charge complete

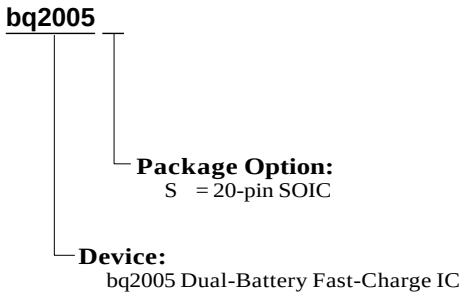
Note: Typical is at T_A = 25°C, V_{CC} = 5.0V.

Data Sheet Revision History

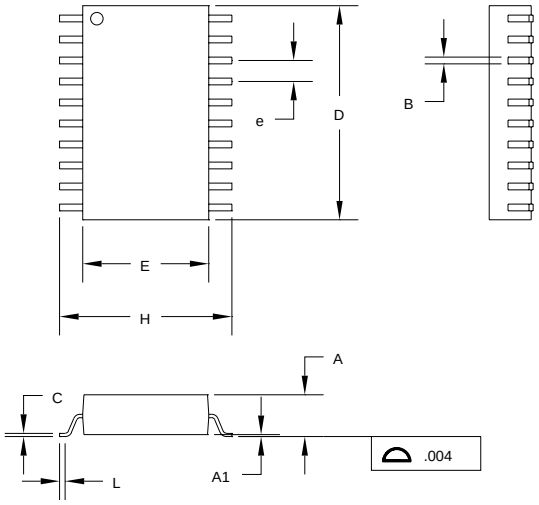
Change No.	Page No.	Description	Nature of Change
3	9	V_{SNSLO} rating	Was V_{SNSHI} - (0.01 * V_{CC}); is 0.04 * V_{CC}
4	5	Corrected sample period	Was: 32s; Is: 34s
4	5, 9	Corrected -ΔV threshold	Was: 13mV Is: 12mV
4	All	Revised and expanded format of this data sheet	Clarification
5	9	T_{OPR}	Deleted industrial temperature range
6	1, 13	Deleted DIP package option	Removed DIP from pinout drawing and Ordering Information; deleted DIP package specifications

Notes: Change 3 = Sept. 1996 D changes from Nov. 1993 C.
Change 4 = Nov. 1997 E changes from Sept. 1996 D.
Change 5 = June 1999 F changes from Nov. 1997 E.
Change 6 = Aug. 2000 G changes from June 1999 F

Ordering Information



S: 20-Pin SOIC



20-Pin S (SOIC)

Dimension	Minimum	Maximum
A	0.095	0.105
A1	0.004	0.012
B	0.013	0.020
C	0.008	0.013
D	0.500	0.515
E	0.290	0.305
e	0.045	0.055
H	0.395	0.415
L	0.020	0.040

All dimensions are in inches.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ2005S	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D
BQ2005S.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D
BQ2005STR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D
BQ2005STR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

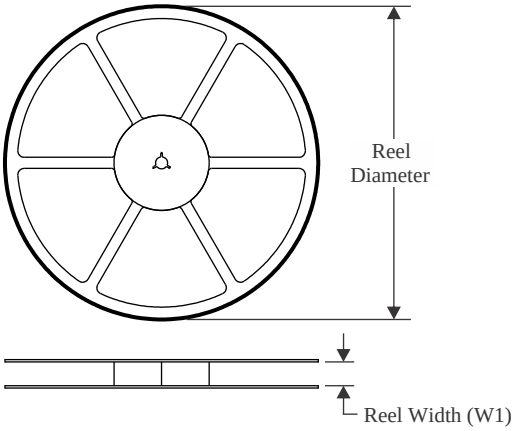
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

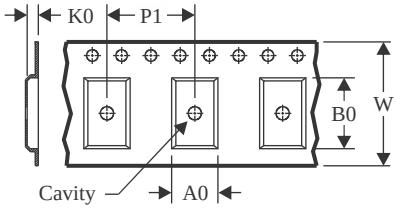
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

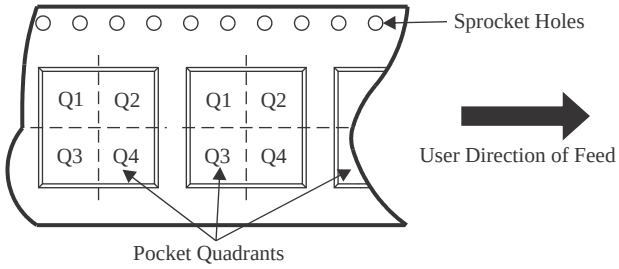


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

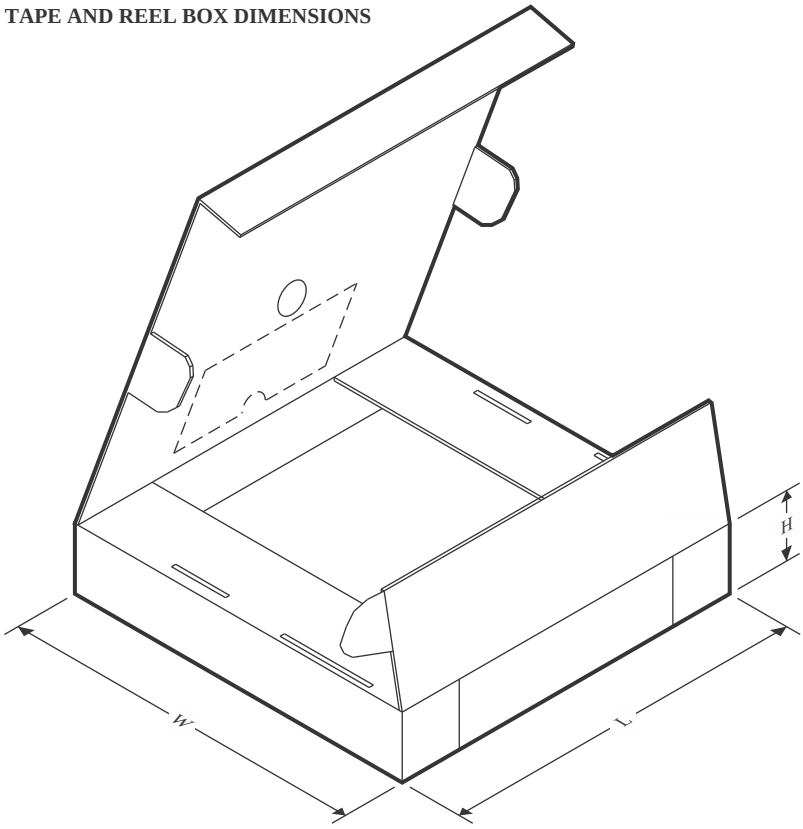
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2005STR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

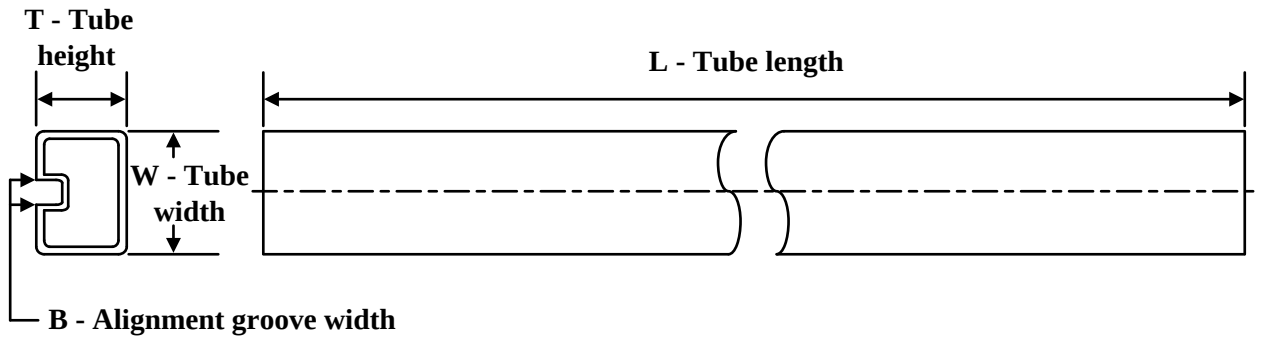
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

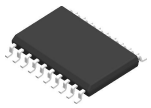
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2005STR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2005S	DW	SOIC	20	25	506.98	12.7	4826	6.6
BQ2005S	DW	SOIC	20	25	507	12.83	5080	6.6
BQ2005S.B	DW	SOIC	20	25	507	12.83	5080	6.6
BQ2005S.B	DW	SOIC	20	25	506.98	12.7	4826	6.6

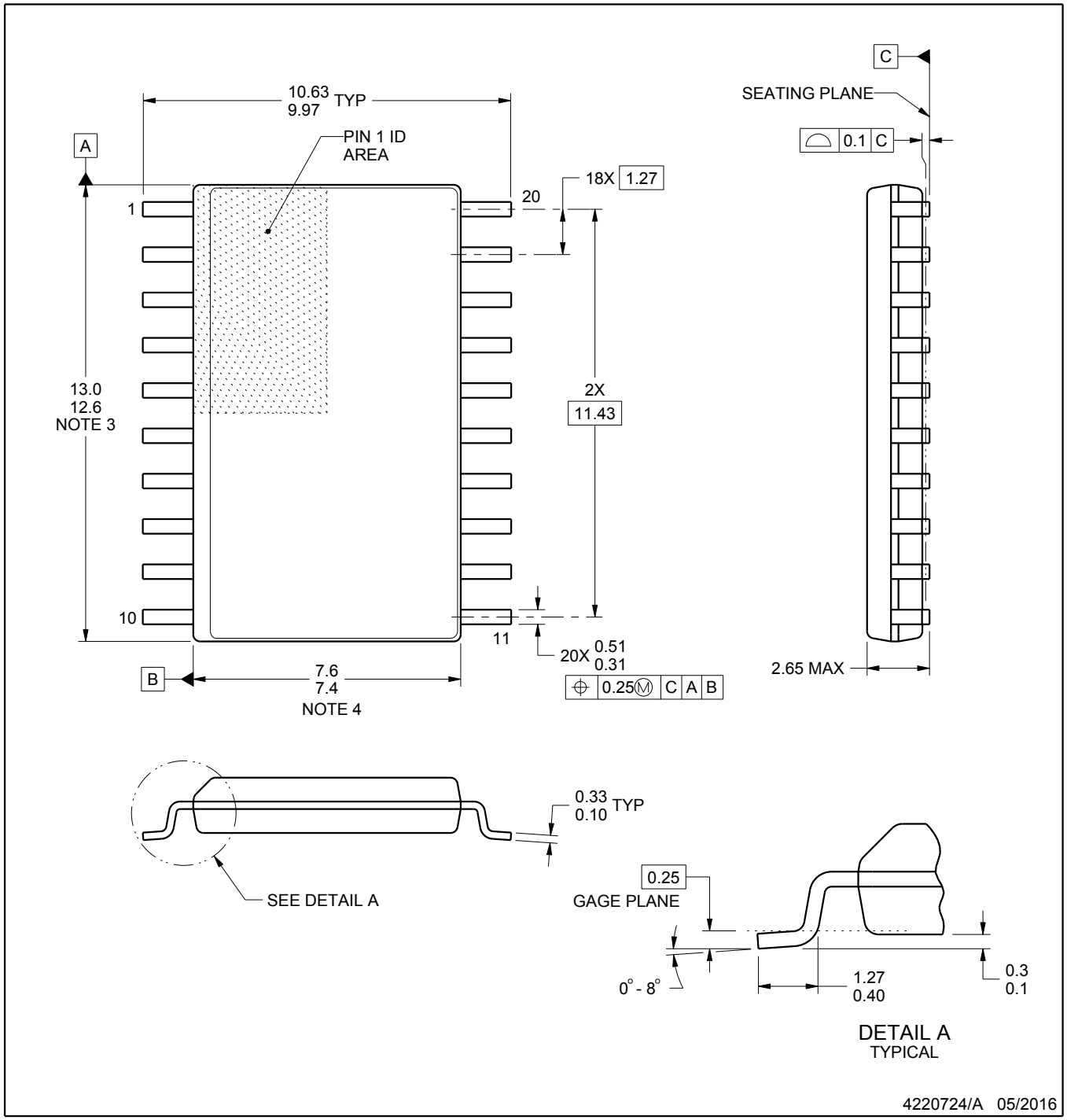


PACKAGE OUTLINE

DW0020A

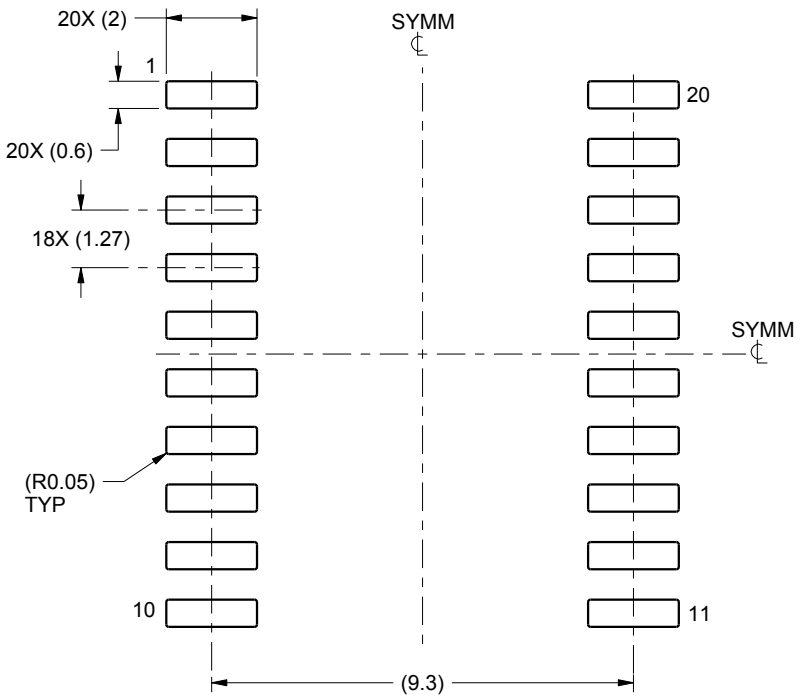
SOIC - 2.65 mm max height

SOIC

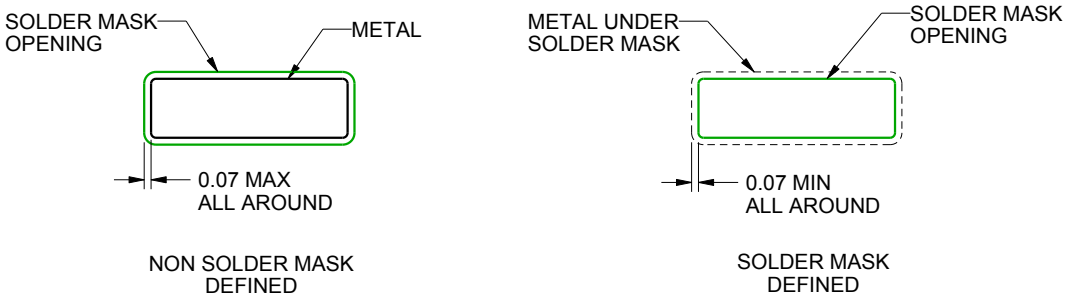


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

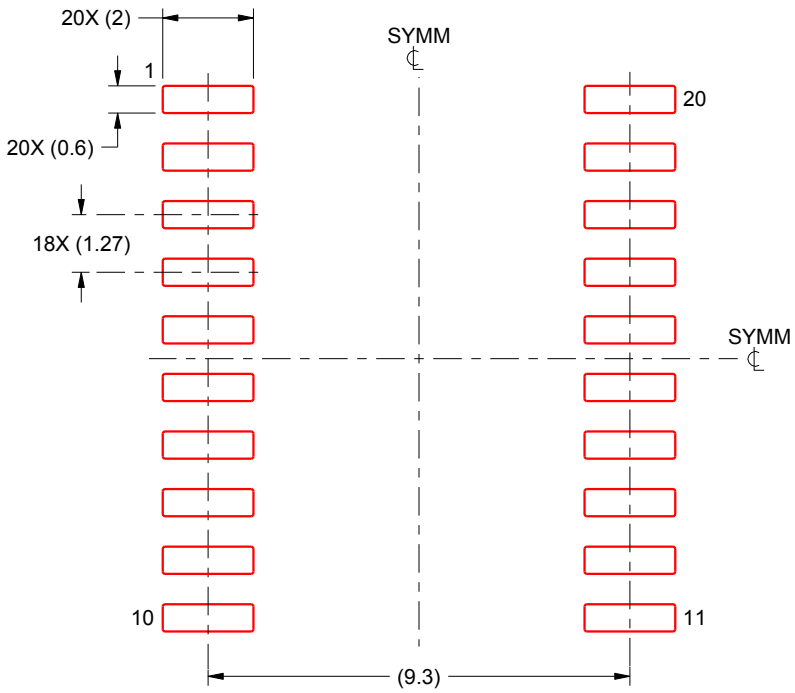


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025