BQ25616/616J Standalone 1-Cell 3.0-A Buck Battery Charger with Power Path and 1.2-A Boost Operation

1 Features

- High-efficiency, 1.5-MHz, synchronous switch-mode buck charger
  - 92% charge efficiency at 2 A from 5-V input
  - ±0.5% charge voltage regulation
  - Adjustable charge voltage from VSET pin supports 4.1 V, 4.2 V, and 4.35 V with ±0.4% regulation accuracy
  - ±6% charge current regulation
  - ±7.5% input current regulation
  - Supports JEITA (BQ25616J) or Hot/Cold (BQ25616) temperature sensing profile
  - 10-hr charging safety timer
- Support USB On-The-Go (OTG)
  - 5-V boost converter with up to 1.2-A output
  - 92% boost efficiency at 1-A output
  - Accurate constant current (CC) limit
  - Soft-start up to 500-μF capacitive load
  - PFM mode for light load operation
- Single input supporting USB input, high-voltage adapter, or wireless power
  - Support 4-V to 13.5-V input voltage range with 22-V absolute max input rating
  - 130-ns fast turn-off input overvoltage protection with optional external OVPFET standing input voltage up to 30 V
  - Programmable input current limit (IINDPM) with ILIM pin
  - VINDPM threshold automatically tracks battery voltage for maximum power
  - Auto detect USB SDP, CDP, DCP and nonstandard adaptors
- Narrow VDC (NVDC) power path management
  - System instant-on with no battery or deeply discharged battery
- Low R_{DSON} 19.5-mΩ BATFET to minimize charging loss and extend battery run time
- 9.5-μA low battery leakage current with system standby
- High integration includes all MOSFETs, current sensing and loop compensation
- Safety Related Certifications:
  - IEC 62368-1 CB Certification

2 Applications

- Electronic Point of Sale (EPOS)
- Wireless speaker
- Industrial, medical, portable electronics

3 Description

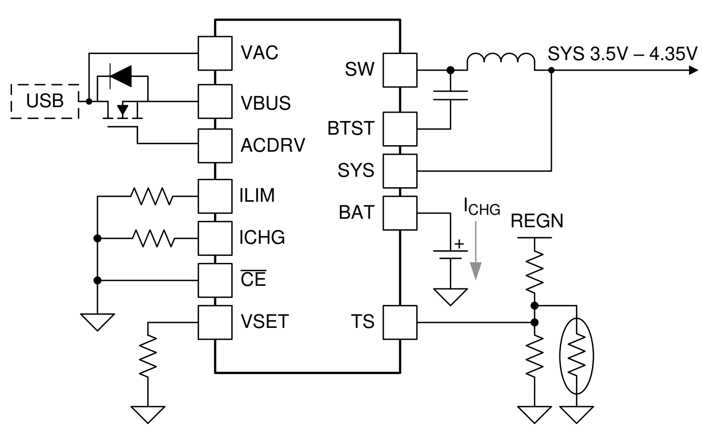
The BQ25616/616J is a highly integrated 3-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer batteries. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery run time during discharging phase.

The BQ25616/616J is a highly integrated 3-A switch-mode battery charge management and system Power Path management device for Li-ion and Li-polymer batteries. It features fast charging with high input voltage support for a wide range of applications including speakers, industrial, and medical portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time, and extends battery run time during discharging phase. Its input voltage and current regulation deliver maximum charging power to the battery.

Device Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
BQ25616/616J	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2020) to Revision A (February 2022) **Page**

- Changed 20-hr charging safety timer to 10-hr charging safety timer in Features......1
- Added Safety Related Certifications: IEC 62368-1 CB Certification......1
- Changed charge safety timer accuracy from 20 hr to 10 hr for BQ25616/J in the Device Comparison Table....4
- Deleted deglitch time and added charge voltage limit in the Device Comparison Table......4
- Changes TS and VAC pin descriptions in Table 7-1......5
- Changed voltage, BAT, SYS (converter not switching) MAX value from 17 V to 7 V in Section 8.1......7
- Added CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE) in Section 8.5......8
- Deleted V_{BST_BAT} and added $V_{BATLOWV\_OTG}$ in Section 8.5......8
- Deleted numerous test conditions in D+/D- Detection section in Section 8.5......8
- Deleted $I_{BST\_OCP\_Q1}$ in Section 8.5......8
- Deleted accuracy from t_{TOP_OFF} and CHG_TIMER = 20hr from t_{SAFETY} in Section 8.6......12
- Changed t_{SAFETY} MIN/TYP/MAX values in Section 8.6......12
- Deleted V_{BATREG} = 4.4 V curve from Figure 8-3......14
- Changed safety timer from 20 hours to 10 hours in Table 9-4......23
- Changed T2 from 20 to 10 in Figure 9-6......24
- Changed Section 9.3.9.5.3......28

5 Description (continued)

The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The hardware setting and status report provides easy configuration to set up the charging solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, USB compliant high voltage adapter and wireless power. It is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device sets default input current limit based on the built-in USB detection through D+/D- pins . When the device built-in USB interface identifies the input adaptor is unknown, the device's input current limit is determined by the ILIM pin setting resistor value.

The device integrates the buck charger and boost regulator into one solution with single inductor. It meets USB On-The-Go (OTG) operation power rating specification by supplying 5V with constant current limit up to 1.2-A.

The Power Path management regulates the system slightly above battery voltage but does not drop below 3.5-V minimum system voltage with adapter applied. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the Power Path management automatically reduces the charge current. As the system load continues to increase, the battery starts to discharge the battery until the system power requirement is met. This supplement mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than the recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and over-current protections. Thermal regulation reduces charge current when the junction temperature exceeds 110°C. The STAT output reports the charging status and any fault conditions.

6 Device Comparison Table

	BQ25606	BQ25616	BQ25616J
Quiescent battery current (BAT, SYS, SW)	58 µA	9.5 µA	9.5 µA
VBUS OVP Reaction-time	200 ns	130 ns	130 ns
Input voltage regulation accuracy	±3%	±2%	±2%
TS profile	JEITA	Hot/Cold	JEITA
Charge safety timer accuracy	10 hr	10 hr	10 hr
Charge voltage limit	4.2 V/4.35 V/4.4 V	4.1 V/4.2 V/4.35 V	4.1 V/4.2 V/4.35 V
Battery voltage regulation	±0.5%	±0.4%	±0.4%
ACDRV	No	Yes	Yes

7 Pin Configuration and Functions

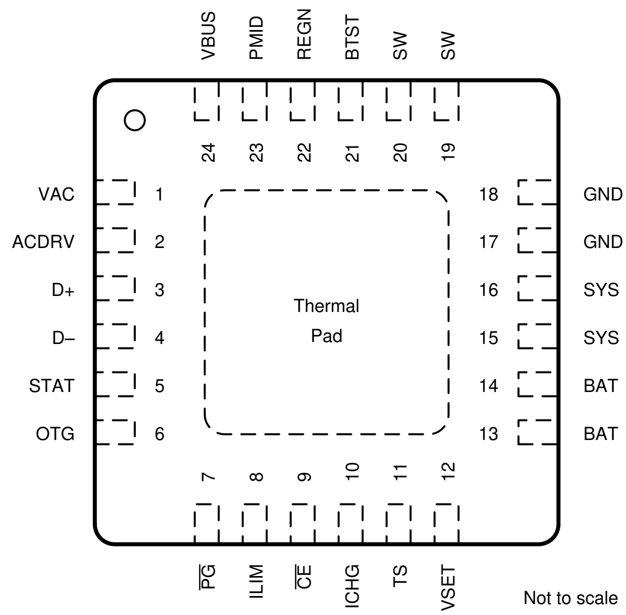


Figure 7-1. RTW Package 24-Pin WQFN Top View

Table 7-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
ACDRV	2	AO	Charge pump output to drive external N-channel MOSFET (ACFET). It provides 6V voltage above VBUS as gate drive to turn on ACFET when VAC voltage is below ACOV threshold (14.2-V) and above UVLO. Leave ACDRV floating if external OVP is not being used.
BAT	13 14	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 µF[2] closely to the BAT pin.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the cathode of the boot-strap diode. Connect the 0.047-µF bootstrap capacitor[2] from SW to BTST.
$\overline{CE}$	9	DI	Charge enable pin. When this pin is driven LOW, battery charging is enabled.
D+	3	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
D–	4	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
GND	17 18	P	Power ground and signal ground
ICHG	10	AI	ICHG pin sets the charge current limit. A resistor is connected from ICHG pin to ground to set charge current limit as ICHG = K_{ICHG}/R_{ICHG}. The acceptable range for charge current is 300 mA – 3000 mA.
ILIM	8	AI	ILIM sets the input current limit when the input adapter is detected as unknown. Otherwise, the input current limit is set by D+/D– detection outcome. A resistor is connected from ILIM pin to ground to set the input current limit as IINDPM = K_{ILIM}/R_{ILIM}. The acceptable range for ILIM current is 500 mA - 3200 mA.
OTG	6	DI	Boost mode enable pin. When this pin is pulled HIGH, boost mode is enabled. OTG pin cannot be floating.
$\overline{PG}$	7	DO	Open drain active low power good indicator. Connect to the pull up rail through 10 kΩ resistor. LOW indicates a good input if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and input current limit is above 30 mA.

Table 7-1. Pin Functions (continued)

PIN NAME	PIN NO.	TYPE[(1)]	DESCRIPTION
PMID	23	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Place a 10-µF capacitor[(2)] on PMID to GND.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boot-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor[(2)] from REGN to analog GND. The capacitor should be placed close to the IC.
STAT	5	DO	Open-drain interrupt output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): Blink at 1Hz
SW	19 20	P	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-µF bootstrap capacitor from SW to BTST.
SYS	15 16	P	System output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 µF (min) capacitor[(2)] close to the SYS pin.
TS	11	AI	Battery temperature qualification voltage input. Connect a negative temperature coefficient thermistor (NTC). Program temperature window with a resistor divider from REGN to TS to GND. Charge and boost mode suspend when TS pin voltage is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and a 10-kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor. BQ25616 supports hot/cold profile and BQ25616J supports JEITA profile.
VAC	1	P	Charger input voltage sensing. Optional external n-channel ACFET is placed between VAC and VBUS. When VAC voltage is below ACOV threshold (14.2-V) and above UVLO, ACFET turns on to connect VAC to VBUS, and power up the charger IC. Connect VAC and VBUS if ACFET is not to be used.
VBUS	24	P	Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor[(2)] from VBUS to GND and place it as close as possible to the device.
VSET	12	AI	VSET pin sets default battery charge voltage . Program battery regulation voltage with a resistor pull-down from VSET to GND. R_{VSET} > 50kΩ (float pin) = 4.208 V R_{VSET} < 500Ω (short to GND) = 4.352 V 5kΩ < R_{VSET} < 25kΩ = 4.100 V
Thermal Pad	—	P	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power
(2) All capacitors are ceramic unless otherwise specified

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage	VAC (converter not switching)	–2	30	V
Voltage	VBUS (converter not switching)	-2	22	V
Voltage	PMID (converter not switching)	–0.3	22	V
Voltage	SW	–0.3	16	V
Voltage	BAT, SYS (converter not switching)	–0.3	7	V
Voltage	BTST	–0.3	22	V
Voltage	ACDRV	–0.3	40	V
Voltage	D+. D-, STAT, OTG, $\overline{PG}$, ILIM, $\overline{CE}$, ICHG, TS, VSET	–0.3	7	V
Output Sink Current	STAT, $\overline{PG}$		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	4		13.5	V
V_{BAT}	Battery voltage			4.35	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			3.2	A
I_{BAT}	Fast charging current			3	A
	RMS discharge current			6	A
T_A	Ambient temperature	–40		85	°C

8.4 Thermal Information

THERMAL METRIC[(1)]		BQ25616/BQ25616J	UNIT
		RTW (WQFN)	
		24 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[(1)])	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.2	°C/W

8.4 Thermal Information (continued)

THERMAL METRIC[1]		BQ25616/BQ25616J RTW (WQFN) 24 Pins	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BAT, SYS, SW)	VBAT = 4.5V, VBUS floating or VBUS = 0V - 5V, SCL, SDA = 0V or 1.8V, T_J < 85 °C, BATFET on.		9.5	15	µA
I_{VBUS}	Input current (VBUS) in buck mode when converter is switching	VBUS=5V, charge disabled, converter switching, ISYS = 0A		2.3		mA
I_{BST}	Quiescent battery current (BAT, SYS, SW) in boost mode when converter is switching	VBAT = 4.5V, VBUS = 4.9V, boost mode enabled, converter switching, I_{VBUS} = 0A		2.4		mA
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		4		13.5	V
V_{VAC_UVLOZ}	VAC rising for ACFET turnon, no battery	VAC rising		3.55	3.85	V
V_{VAC_UVLO}	VAC falling for ACFET turnoff, no battery	VAC falling		3.25	3.55	V
V_{ACDRV}	External ACFET gate drive voltage with minimum 8nF CGS			10		V
V_{VBUS_UVLOZ}	VBUS rising for active bias, no battery	VBUS rising		3.3	3.7	V
V_{VBUS_UVLO}	VBUS falling to turnoff bias, no battery	VBUS falling		3	3.3	V
$V_{VBUS\_PRESENT}$	VBUS to enable REGN	VBUS rising		3.65	3.9	V
$V_{VBUS\_PRESENTZ}$	VBUS to disable REGN	VBUS falling		3.15	3.4	V
V_{SLEEP}	Enter Sleep mode threshold	VBUS falling, VBUS - VBAT, VBAT = 4V	15	60	110	mV
V_{SLEEPZ}	Exit Sleep mode threshold	VBUS rising, VBUS - VBAT, VBAT = 4V	115	220	340	mV
V_{ACOV}	VAC overvoltage rising threshold to turnoff ACFET and switching	VAC rising	13.5	14.2	14.85	V
	VAC overvoltage falling threshold to turnon ACFET and switching	VAC falling,	13	13.9	14.5	V
V_{BAT_UVLOZ}	BAT voltage for active bias, no VBUS	VBAT rising	2.5			V
V_{BAT_DPLZ}	BAT depletion rising threshold to turn on BATFET	VBAT rising	2.35		2.8	V
V_{BAT_DPL}	BAT depletion falling threshold to turn off BATFET	VBAT falling	2.18		2.62	V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.75	3.9	4.0	V
POWER PATH MANAGEMENT						
V_{SYS_MIN}	Typical minimum system regulation voltage	VBAT=3.2V < SYS_MIN = 3.5V, ISYS = 0A	3.5	3.65		V
V_{SYS_OVP}	System overvoltage threshold	VREG = 4.35V, Charge disabled, ISYS = 0A		4.7		V
R_{ON_RBFET}	Blocking FET on-resistance			45		mΩ

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON_HSFET}	High-side switching FET on-resistance			62		mΩ
R_{ON_LSFET}	Low-side switching FET on-resistance			71		mΩ
V_{BATFET_FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10mA, converter running		30		mV
BATTERY CHARGER						
V_{REG_ACC}	Charge voltage accuracy	VREG = 4.1V, R_{VSET}=10kΩ, T_J = 0°C - 85°C	4.0836	4.1	4.1164	V
		VREG = 4.2V, R_{VSET}>50kΩ, T_J = 0°C - 85°C	4.1832	4.2	4.2168	V
		VREG = 4.35V, R_{VSET}<500Ω, T_J = 0°C - 85°C	4.3326	4.35	4.3674	V
I_{CHG_RANGE}	Typical charge current regulation range		0		3	A
K_{ICHG}	ICHG pin setting ratio	ICHG=K_{ICHG}/R_{ICHG}, VBAT = 3.1V, T_J = –40°C - 85°C	639	677	715	AxΩ
		ICHG=K_{ICHG}/R_{ICHG}, VBAT = 3.8V, T_J = –40°C - 85°C	639	677	715	AxΩ
I_{CHG_ACC}	Fast charge current regulation accuracy	R_{ICHG} = 1100 Ω, VBAT = 3.1V or 3.8V, T_J = –40°C - 85°C	0.516	0.615	0.715	A
		R_{ICHG} = 562 Ω, VBAT = 3.1V or 3.8V, T_J = –40°C - 85°C	1.14	1.205	1.28	A
		R_{ICHG} = 372 Ω, VBAT = 3.1V or 3.8V, T_J = –40°C - 85°C	1.715	1.82	1.89	A
I_{PRECHG_RATIO}	Precharge current accuracy	As percentage of ICHG, VBAT = 2.6V		5		%
I_{PRECHG_ACC}	Precharge current accuracy	R_{ICHG} = 1100 Ω, VBAT = 2.6V, T_J = –40°C - 85°C	21	30	38	mA
		R_{ICHG} = 562 Ω, VBAT = 2.6V, T_J = –40°C - 85°C	48	60	67	mA
		R_{ICHG} = 372 Ω, VBAT = 2.6V, T_J = –40°C - 85°C	76	90	97	mA
I_{TERM_RATIO}	Termination current accuracy	As percentage of ICHG, VBAT = 4.35V, (char, all codes)		5		%
I_{TERM_ACC}	Termination current accuracy	R_{ICHG} = 1100 Ω, VBAT = 4.35V, T_J = 0°C - 85°C	9	31	57	mA
		R_{ICHG} = 562 Ω, VBAT = 4.35V, T_J = 0°C - 85°C	36	60	85	mA
		R_{ICHG} = 372 Ω, VBAT = 4.35V, T_J = 0°C - 85°C	56	91	126	mA
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising	2.13	2.25	2.35	V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling	1.85	2	2.15	V
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}	70	90	110	mA
$V_{BATLOWV}$	Battery LOWV rising threshold to start fast-charge	VBAT rising	3	3.12	3.24	V
	Battery LOWV falling threshold to stop fast-charge	VBAT falling	2.7	2.8	2.9	V
V_{RECHG}	Battery recharge threshold	VBAT falling	90	100	150	mV
I_{SYS_LOAD}	System discharge load current during SYSOVP			30		mA

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON_BATFET}	Battery FET on-resistance	T_J = -40°C - 85°C		19.5	26	mΩ
		T_J = -40°C - 125°C		19.5	30	mΩ
BATTERY OVERVOLTAGE PROTECTION						
V_{BAT_OVP}	Battery overvoltage rising threshold	VBAT rising, as percentage of VREG	103	104	105	%
	Battery overvoltage falling threshold	VBAT falling, as percentage of VREG	101	102	103	%
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_ACC}	Typical input voltage regulation accuracy		4.171	4.3	4.429	V
V_{INDPM_TRACK}	VINDPM threshold to track battery voltage	VBAT = 4.35V	4.45	4.55	4.74	V
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA (T_J=-40°C - 85°C)	450	465	500	mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 900mA (T_J=-40°C-85°C)	750	835	900	mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 1500mA (T_J=-40°C-85°C)	1300	1390	1500	mA
K_{ILIM}	ILIM pin setting ratio		459	478	500	A x Ω
D+ / D- DETECTION						
V_{DP_SRC}	D+ line source voltage		500	600	700	mV
I_{DP_SRC}	D+ line data contact detect current source	VD+ = 200 mV	7	10	14	µA
I_{DP_SINK}	D+ line sink current	VD+ = 500 mV	50	100	150	µA
$V_{DP\_DAT\_REF}$	D+ line data detect voltage	D+ pin Rising	250		400	mV
$V_{DP\_LGC\_LOW}$	D+ line logic low.	D+ pin Rising			800	mV
R_{DP_DWN}	D+ line pull-down resistance	VD+ = 500 mV	14.25		24.8	kΩ
I_{D+_LKG}	Leakage current into D+ line	Pull up to 1.8 V	–1		1	µA
V_{DM_SRC}	D- line source voltage		500	600	700	mV
I_{DM_SINK}	D- line sink current	VD- = 500 mV	50	100	150	µA
$V_{DM\_DAT\_REF}$	D- line data detect voltage	D- pin Rising	250		400	mV
R_{DM_DWN}	D- line pull-down resistance	VD- = 500 mV	14.25		24.8	kΩ
I_{D-_LKG}	Leakage current into D- line	Pull up to 1.8 V	–1		1	µA
$V_{D+\_2p8\_hi}$	D+ High comparator threshold for 2.8V detection	D+ pin rising	2.85	3	3.1	V
$V_{D+\_2p8\_lo}$	D+ Low comparator threshold for 2.8V detection	D+ pin rising	2.35	2.45	2.55	V
V_{D+_2p8}	D+ comparator threshold for non-standard adapter		2.55		2.85	V
$V_{D-\_2p8\_hi}$	D- High comparator threshold for 2.8V detection	D- pin rising	2.85	3	3.1	V
$V_{D-\_2p8\_lo}$	D- Low comparator threshold for 2.8V detection	D- pin rising	2.35	2.45	2.55	V
V_{D-_2p8}	D- comparator threshold for non-standard adapter		2.55		2.85	V
$V_{D+\_2p0\_hi}$	D+ High comparator threshold for 2.0V detection	D+ pin rising	2.15	2.25	2.35	V
$V_{D+\_2p0\_lo}$	D+ Low comparator threshold for 2.0V detection	D+ pin rising	1.6	1.7	1.85	V
V_{D+_2p0}	D+ comparator threshold for non-standard adapter		1.85		2.15	V
$V_{D-\_2p0\_hi}$	D- High comparator threshold for 2.0V detection	D- pin rising	2.15	2.25	2.35	V

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{D-\_2p0\_lo}$	D- Low comparator threshold for 2.0V detection	D- pin rising	1.6	1.7	1.85	V
V_{D-_2p0}	D- comparator threshold for non-standard adapter		1.85		2.15	V
$V_{D+\_1p2\_hi}$	D+ High comparator threshold for 1.2V detection	D+ pin rising	1.35	1.5	1.6	V
$V_{D+\_1p2\_lo}$	D+ Low comparator threshold for 1.2V detection	D+ pin rising	0.85	0.95	1.05	V
V_{D+_1p2}	D+ comparator threshold for non-standard adapter		1.05		1.35	V
$V_{D-\_1p2\_hi}$	D- High comparator threshold for 1.2V detection	D- pin rising	1.35	1.5	1.6	V
$V_{D-\_1p2\_lo}$	D- Low comparator threshold for 1.2V detection	D- pin rising	0.85	0.95	1.05	V
V_{D-_1p2}	D- comparator threshold for non-standard adapter		1.05		1.35	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy			110		°C
T_{SHUT}	Thermal Shutdown Rising threshold	Temperature Increasing		150		°C
	Thermal Shutdown Falling threshold	Temperature Decreasing		130		°C
CHARGE MODE THERMISTOR COMPARATOR (JEITA 616J or HOT/COLD 616)						
$V_{T1\_RISE\%}$	TS pin voltage rising threshold, Charge suspended above this voltage.	As Percentage to REGN (0°C w/ 103AT)	72.4	73.3	74.2	%
$V_{T1\_FALL\%}$	TS pin voltage falling threshold. Charge re-enabled to 20% of ICHG and VREG below this voltage.	As Percentage to REGN	71.5	72	72.5	%
$V_{T2\_RISE\ \%}$	TS pin voltage rising threshold, Charge back to 20% of ICHG and VREG above this voltage (616J).	As Percentage to REGN (10°C w/ 103AT)	67.75	68.25	68.75	%
$V_{T2\_FALL\%}$	TS pin voltage falling threshold. Charge back to ICHG and VREG below this voltage (616J)	As Percentage to REGN	66.45	66.95	67.45	%
$V_{T3\_FALL\%}$	TS pin voltage falling threshold. Charge back to ICHG and VREG below this voltage (616J)	As Percentage to REGN (45°C w/ 103AT)	44.25	44.75	45.25	%
$V_{T3\_RISE\%}$	TS pin voltage rising threshold. Charge back to ICHG and VREG above this voltage. (616J)	As Percentage to REGN	45.55	46.05	46.55	%
$V_{T5\_FALL\%}$	TS pin voltage falling threshold, charge suspended below this voltage.	As Percentage to REGN (60°C w/ 103AT)	33.7	34.2	35.1	%
$V_{T5\_RISE\%}$	TS pin voltage rising threshold. Charge back to ICHG and 4.1V above this voltage.	As Percentage to REGN	35	35.5	36	%
$V_{T1\_RISE\_HC\%}$	TS pin voltage rising threshold. Charge suspended above this voltage. (616)	As Percentage to REGN (0°C w/ 103AT)	72.4	73.3	74.2	%
$V_{T1\_FALL\_HC\%}$	TS pin voltage falling threshold. Charge back to ICHG and VREG below this voltage. (616)	As Percentage to REGN	71	72	73	%

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{T3\_FALL\_HC\%}$	TS pin voltage falling threshold. Charge suspended below this voltage. (616)	As Percentage to REGN (45°C w/ 103AT)	44.25	44.75	45.25	%
$V_{T3\_RISE\_HC\%}$	TS pin voltage rising threshold. Charge back to ICHG and VREG above this voltage. (616)	As Percentage to REGN	45.55	46.05	46.55	%
BOOST MODE THERMISTOR COMPARATOR (HOT/COLD)						
$V_{BCOLD\_RISE\%}$	TS pin voltage rising threshold, boost mode is suspended above this voltage.	As Percentage to REGN (–19.5°C w/ 103AT)	79.5	80	80.5	%
$V_{BCOLD\_FALL\%}$	TS pin voltage falling threshold	As Percentage to REGN (0°C w/ 103AT)		72		%
$V_{BHOT\_FALL\%}$	TS pin voltage threshold. boost mode is suspended below this voltage.	As Percentage to REGN, (64°C w/ 103AT)	30.2	31.2	32.2	%
$V_{BHOT\_RISE\%}$	TS pin voltage rising threshold	As Percentage to REGN, (45°C w/ 103AT)		44		%
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{HSFET_OCP}	HSFET cycle-by-cycle overcurrent threshold		5.2		8.0	A
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.32	1.5	1.68	MHz
D_{MAX}	Maximum PWM Duty Cycle			97		%
BOOST MODE CONVERTER						
$V_{BATLOWV\_OTG}$	Battery voltage exiting boost mode	V_{VBAT} falling	2.6	2.8	2.9	V
	Battery voltage entering boost mode	V_{VBAT} rising	2.9	3.0	3.15	V
V_{BST_ACC}	Boost mode voltage regulation accuracy	IVBUS = 0A, BOOST_V = 5V	4.85	5	5.15	V
I_{BST_ACC}	Boost mode current regulation accuracy		1.2	1.4	1.6	A
$I_{SYS\_OCP\_Q4}$	Boost mode battery discharge current clamp on BATFET Q4		9	10		A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 20mA	4.58	4.7	4.8	V
		V_{VBUS} = 9V, I_{REGN} = 20mA	5.6	6	6.5	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5V, V_{REGN} = 3.8V	50			mA
LOGIC INPUT PIN						
V_{IH}	Input high threshold level (/CE)		1.3			V
V_{IL}	Input low threshold level (/CE)				0.4	V
I_{IN_BIAS}	High-level leakage current (/CE)	Pull up rail 1.8V			1	µA
LOGIC OUTPUT PIN						
V_{OL}	Output low threshold level (STAT, /PG)	Sink current = 5mA			0.4	V
I_{OUT_BIAS}	High-level leakage current (STAT, /PG)	Pull up rail 1.8V			1	µA

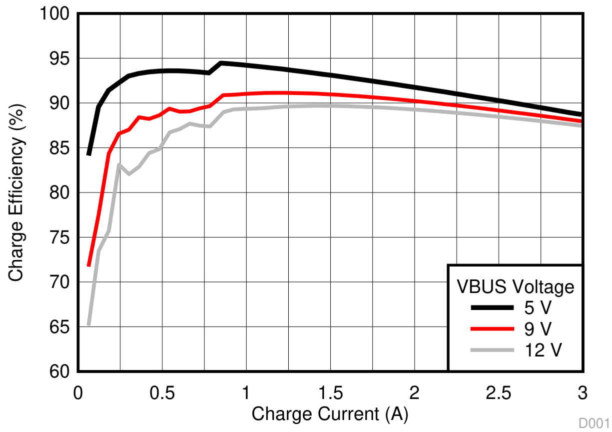
8.6 Timing Requirements

		MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP					
$t_{POORSRC}$	Bad adapter detection duration		30		ms

8.6 Timing Requirements (continued)

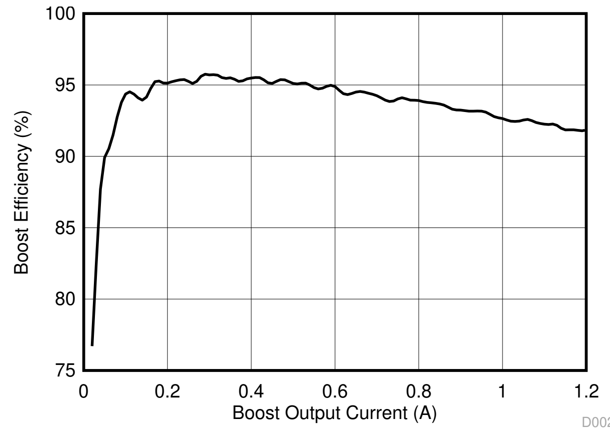
		MIN	NOM	MAX	UNIT
$t_{POORSRC\_RETRY}$	Bad adapter detection retry wait time		2		s
BATTERY CHARGER					
t_{TERM_DGL}	Deglitch time for charge termination		30		ms
t_{RECHG_DGL}	Deglitch time for recharge threshold		30		ms
t_{TOP_OFF}	Typical top-off timer		30		min
t_{SAFETY}	Charge safety timer accuracy	8	10	12	hr

8.7 Typical Characteristics



f_{SW} = 1.5 MHz Inductor DCR = 18 mΩ
V_{BAT} = 3.8 V

Figure 8-1. Charge Efficiency vs. Charge Current



V_{OTG} = 5.0 V inductor DCR = 18 mΩ
V_{BAT} = 3.8 V

Figure 8-2. Efficiency vs. OTG Current

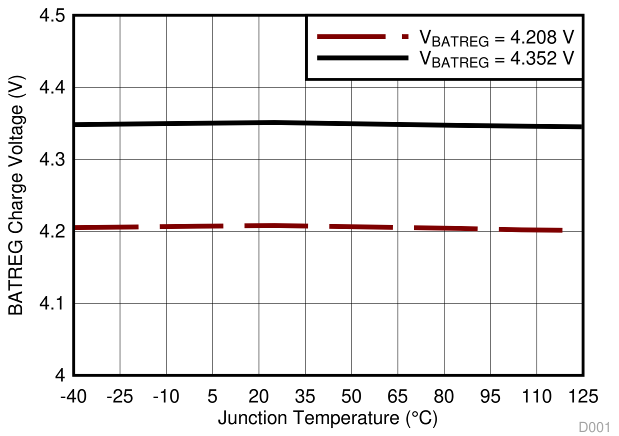
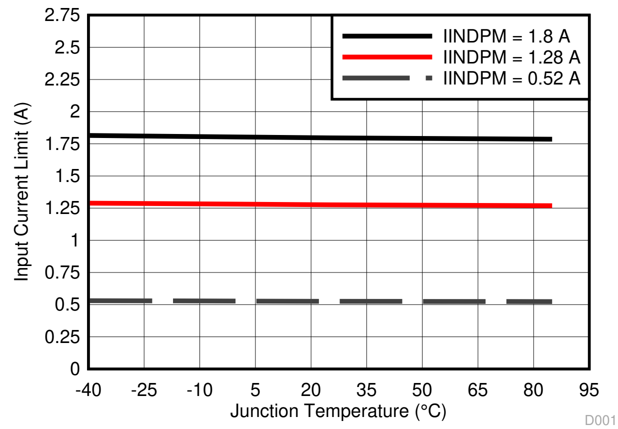
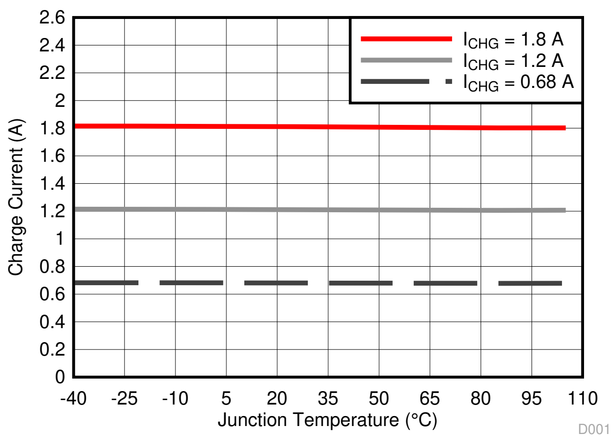


Figure 8-3. BATREG Charge Voltage vs. Junction Temperature



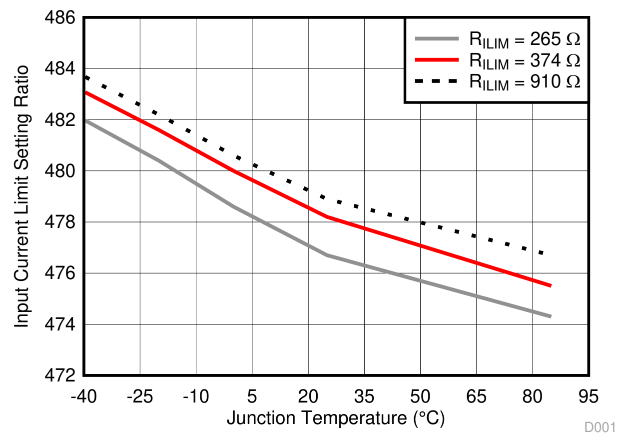
V_{VBUS} = 5 V

Figure 8-4. Input Current Limit vs. Junction Temperature



V_{VBUS} = 5 V V_{BAT} = 3.8 V

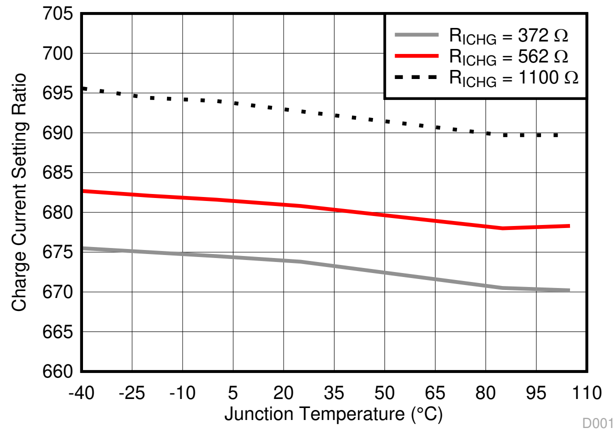
Figure 8-5. Charge Current vs. Junction Temperature



V_{VBUS} = 5 V V_{BAT} = 3.8 V

Figure 8-6. Input Current Limit Setting Ratio vs. Junction Temperature

8.7 Typical Characteristics (continued)



V_{VBUS} = 5 V
V_{BAT} = 3.8 V

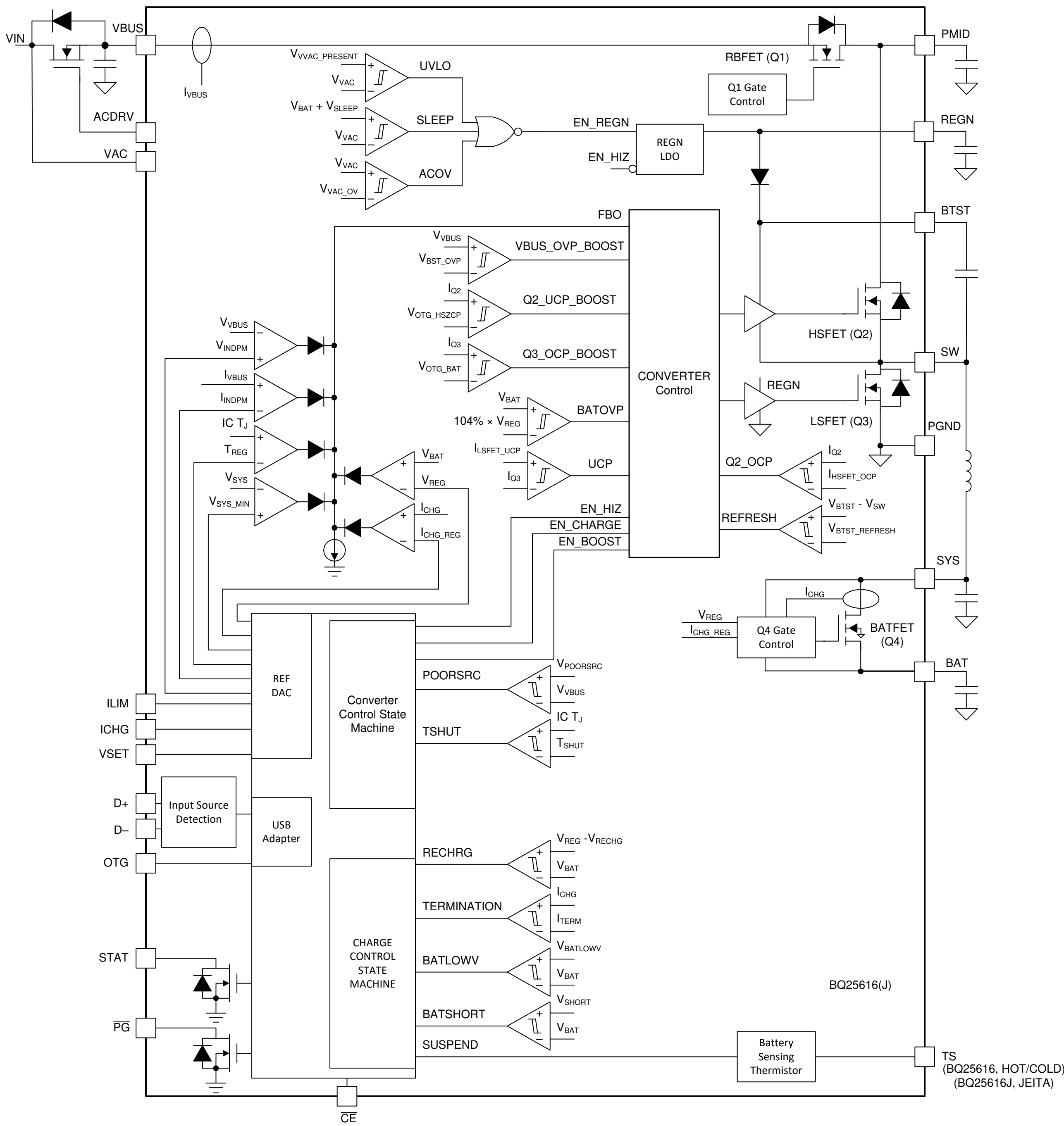
Figure 8-7. Charge Current Setting Ratio vs. Junction Temperature

9 Detailed Description

9.1 Overview

The BQ25616/616J device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-ion and Li-polymer battery. It includes an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When V_{VBUS} rises above V_{VBUS_UVLOZ} or V_{BAT} rises above V_{BAT_UVLOZ}, the sleep comparator, battery depletion comparator, and BATFET driver are active.

9.3.2 Device Power Up From Battery Without Input Source

If only the battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects the battery to the system. The REGN stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through the BATFET. When the system is overloaded or shorted ($I_{BAT} > I_{SYS\_OCP\_Q4}$), the device turns off BATFET immediately until the input source plugs in again.

9.3.3 Power Up From Input Source

When an input source is plugged in, the device checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power-up sequence from input source is as listed:

1. Power Up ACFET, see Section 9.3.3.1 (optional)
2. Power Up REGN LDO, see Section 9.3.3.2
3. Poor Source Qualification, see Section 9.3.3.3
4. Input Source Type Detection is based on D+/D– to set default input current limit (IINDPM threshold), see Section 9.3.3.4
5. Input Voltage Limit Threshold Setting (VINDPM threshold), see Section 9.3.3.5
6. Power Up Converter, see Section 9.3.3.6

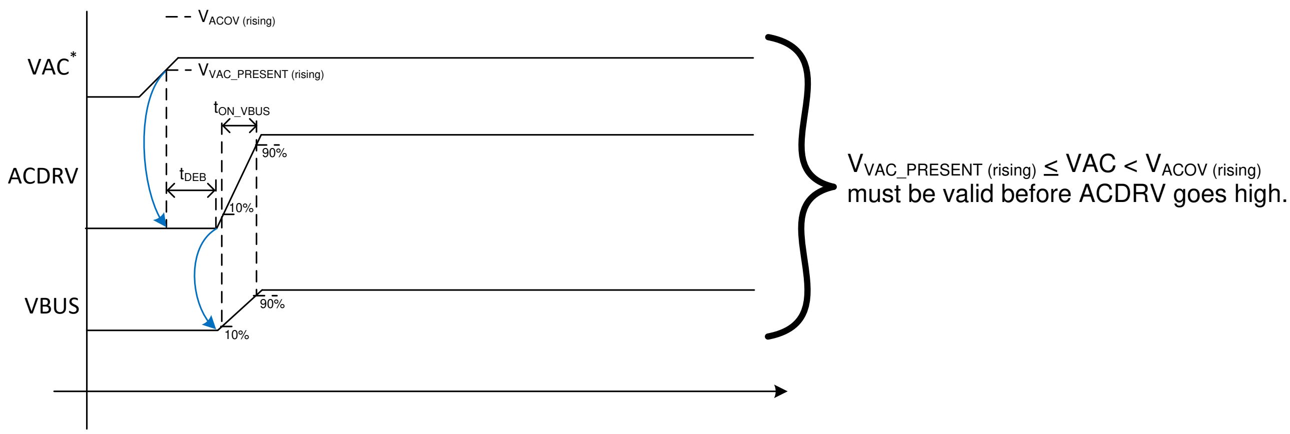
9.3.3.1 Power Up ACFET

The external ACFET provides an additional layer of voltage protection for the device. During input surge up to 30 V, the charger turns off ACFET and converter with 130-ns response time to disconnect VBUS from VAC. If users don't need ACFET, they shall connect VAC to VBUS and keep ACDRV pin floating. The ACFET is enabled when all the below conditions are valid.

The ACFET is enabled when all the below conditions are valid.

- $V_{VAC\_PRESENT} < V_{VAC} < V_{ACOV}$.
- After t_{DEB} (15 ms typ) delay is completed

If one of the above conditions is not valid, ACFET keeps off. The battery powers the system If it is present.



(*) Stimulus from application
Note: beginning of blue lines indicate the trigger, and the arrow end of the blue line indicates the action

Figure 9-1. ACFET Startup Control

9.3.3.2 Power Up REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. It also provides the bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN LDO is enabled when all the below conditions are valid:

- $V_{VBUS} > V_{VBUS\_UVLOZ}$
- In buck mode, ACFET turns on, $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$
- In boost mode, $V_{VBUS} < V_{BAT} + V_{SLEEPZ}$
- After 220-ms delay is completed

During high impedance mode , REGN LDO turns off. The battery powers up the system.

9.3.3.3 Poor Source Qualification

After the REGN LDO powers up, the device starts to check current capability of the input source. The first step is poor source detection.

- VBUS voltage above $V_{POORSRC}$ when pulling I_{BADSRC} (typical 30 mA)

If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

9.3.3.4 Input Source Type Detection (IINDPM Threshold)

After poor source detection, the device runs input source detection through D+/D– lines . The D+/D– detection follows the USB Battery Charging Specification 1.2 (BC1.2) to detect standard (SDP/CDP/DCP) and non-standard adapters through USB D+/D– lines.

9.3.3.4.1 D+/D– Detection Sets Input Current Limit

The device contains a D+/D– based input source detection to set the input current limit when a 5-V adapter is plugged-in. The D+/D– detection includes standard USB BC1.2 and non-standard adapters. When an input source is plugged in, the device starts standard USB BC1.2 detection. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is set at 2.4-A. If an adapter is detected as unknown, the input current limit is set by ILIM pin .

The D+/D– automatically runs when adapter plugs in. The D+/D– detection contains three steps, DCD (Data Contact Detection), primary detection, and secondary detection.

DCD (Data Contact Detection) uses a current source to detect when the D+/D– pins have made contact during an attach event. The protocol for data contact detect is as follows:

- Detect VBUS present and VBUS_GD (pass poor source detection)
- Turn on D+ I_{DP_SRC} and the D– pull-down resistor R_{DM_DWN} for 13 ms
- If the USB connector is properly attached, the D+ line goes from HIGH to LOW, wait up to 0.5 sec. When the DCD timer of 0.5 sec is expired, the non-standard adapter detection is applied to set the input current limit.
- Turn off I_{DP_SRC} and disconnect R_{DM_DWN}

The primary detection is used to distinguish between USB host (Standard Down Stream Port, or SDP) and different type of charging ports (Charging Down Stream Port, or CDP, and Dedicated Charging Port, or DCP). The protocol for primary detection is as follows:

- Turn on V_{DP_SRC} on D+ and I_{DM_Sink} on D– for 40 ms
- If portable device is attached to a USB host (SDP), the D– is below V_{REF_DAT}. Otherwise, it is attached to either CDP or DCP.
- Turn off V_{DP_SRC} and I_{DM_Sink}

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). The protocol for secondary detection is as follows:

- Turn on V_{DM_SRC} on D- and I_{DP_Sink} on D+ for 40 ms
- If portable device is attached to a Charging Downstream Port (CDP), the D+ is below V_{DAT_REF}. Otherwise, it is attached to DCP.
- Turn off V_{DM_SRC} and I_{DP_Sink}

Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port will power cycle back to SDP even the D+/D– detection indicates CDP.

Table 9-1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within $V_{D+/D-\_2p8}$	V_{D-} within $V_{D+/D-\_2p0}$	2.1
Divider 2	V_{D+} within $V_{D+/D-\_1p2}$	V_{D-} within $V_{D+/D-\_1p2}$	2
Divider 3	V_{D+} within $V_{D+/D-\_2p0}$	V_{D-} within $V_{D+/D-\_2p8}$	1
Divider 4	V_{D+} within $V_{D+/D-\_2p8}$	V_{D-} within $V_{D+/D-\_2p8}$	2.4

Table 9-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINDPM)
USB CDP	1.5 A
USB DCP	2.4 A
Divider 1	2.1 A
Divider 2	2.0 A
Divider 3	1.0 A
Divider 4	2.4 A
Unknown 5-V Adapter	Set by ILIM pin

9.3.3.5 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device has two modes to set the VINDPM threshold.

- Fixed VINDPM threshold. VINDPM is set at 4.3 V.
- VINDPM threshold tracks the battery voltage to optimize the converter headroom between input and output. The actual input voltage limit is the higher of the VINDPM setting (4.3-V) and V_{BAT} + 200 mV.

9.3.3.6 Power Up Converter in Buck Mode

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. The system voltage is powered from the converter instead of the battery. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery.

The device provides soft start when the system rail is ramping up. When the system rail is below V_{BAT_SHORT}, the input current is limited to 200 mA . The system load should be appropriately planned not to exceed the 200-mA IINDPM limit. After the system rises above V_{BAT_SHORTZ}, the device input current limit is the value set the by ILIM pin .

As a battery charger, the device deploys a highly efficient 1.5-MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature simplifying output filter design.

The converter supports PFM operation by default for fast transient response during system voltage regulation and better light load efficiency.

9.3.4 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through a USB port. The output voltage is regulated at 5 V and output current is up to 1.2 A with constant current regulation.

Boost operation is enabled if the conditions below are valid:

1. OTG pin HIGH
2. VBUS less than V_{BAT} + V_{SLEEP} (in sleep mode) before converter starts.
3. Voltage at TS (thermistor) pin, as a percentage of V_{REGN}, is within acceptable range ($V_{BHOT\_RISE\%} < V_{TS\%} < V_{BCOLD\_FALL\%}$)
4. After 30-ms delay from boost mode enable .
5. Not in any fault such as $I_{SYS\_OCP\_Q4}$, TSHUT, ACOV or VBUS OV.

The converter supports PFM operation at light load in Boost mode.

9.3.5 Standalone Charger

The BQ25616/616J is a standalone device without host control. Any change on $\overline{\text{CE}}$, ICHG and ILIM pins will cause a real time internal reference change. Charging is enabled or disabled via the $\overline{\text{CE}}$ pin. D+/D– and ILIM pins control the input current limit settings. D+/D– detection and VSET pin setting only takes effect upon adapter plug-in.

Charge current must be programmed to a value within a range of 300 mA to 3000 mA with a pull-down resistor on the ICHG pin. The charge current is set as:

$$I_{ICHG} = K_{ICHG}/R_{ICHG} \tag{1}$$

Input current limit must be programmed to a value within a range of 500 mA to 3200 mA with a pull-down resistor on the ILIM pin. The input current limit is set as:

$$I_{IINDPM} = K_{ILIM}/R_{ILIM} \tag{2}$$

The battery regulation voltage is programmed with a pull-down resistor on the VSET pin as follows:

- R_{VSET} > 50 kΩ (float pin): V_{REG} = 4.20 V
- R_{VSET} < 500 Ω (short pin): V_{REG} = 4.35 V
- 5kΩ < R_{VSET} < 25 kΩ: V_{REG} = 4.10 V

Table 9-3. Standalone Device Configuration

	BQ25616/616J
USB OTG	5 V/1.2 A
USB Detection	D+/D–
VINDPM	4.3 V and V_{BAT} + 200 mV
VBUS Operating Range	4 V - 13.5 V
V_{REG}	VSET pin (4.20 V, 4.35 V, or 4.10 V)
Safety Timer	10 hr fast charge

Table 9-3. Standalone Device Configuration (continued)

	BQ25616/616J
Pre-charge Timer	2 hr
I_{PRECHG}	5% of I_{CHG}
I_{TERM}	5% of I_{CHG}
Charging Temperature Profile	JEITA 0-60°C (BQ25616J), Hot/Cold 0-45°C (BQ25616)
OTG Temperature Profile	–20°C to +60°C

If a fault is detected, the STAT pin will blink at 1 Hz. STAT pin will stop blinking when the fault goes away. All faults will be reset upon adapter re-connection. A boost mode fault will be cleared either by adapter re-connection or toggling of the OTG pin.

9.3.6 Power Path Management

The device accommodates a wide range of input sources such as USB, wall adapter, or car charger. The device provides automatic power path selection to supply the system (SYS) from the input source (VBUS), battery (BAT), or both.

9.3.6.1 Narrow VDC Architecture

When the battery is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of the BATFET.

When battery charging is disabled and above the minimum system voltage setting or charging is terminated, the system is always regulated at typically 50 mV above the battery voltage.

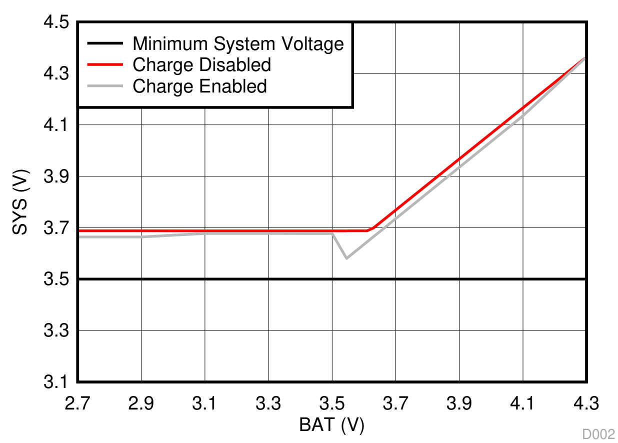


Figure 9-2. System Voltage vs Battery Voltage

9.3.6.2 Dynamic Power Management

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit or the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

Figure 9-3 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

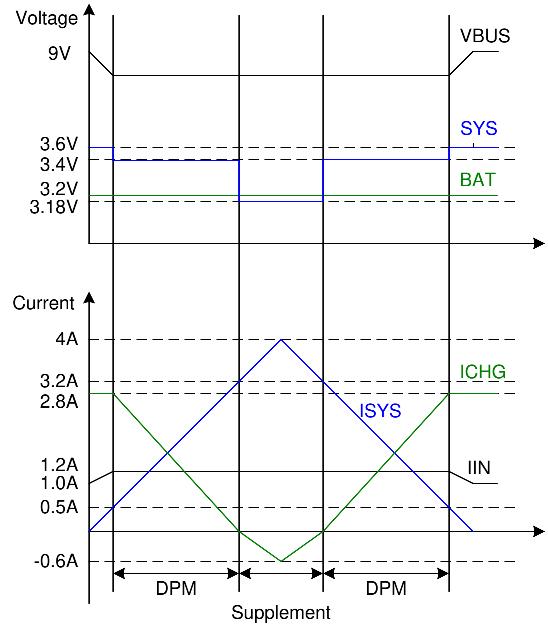


Figure 9-3. DPM Response

9.3.6.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. Figure 9-4 shows the V-I curve of the BATFET gate regulation operation. The BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

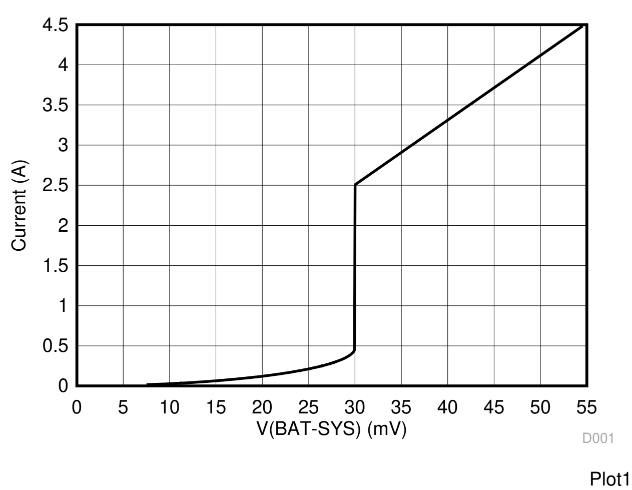


Figure 9-4. BAFET V-I Curve

9.3.7 Battery Charging Management

The device charges a 1-cell Li-ion battery with up to 3.0-A charge current for a high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

9.3.7.1 Autonomous Charging Cycle

When battery charging is enabled ($\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle. The device default charging parameters are listed in Table 9-4.

Table 9-4. Charging Parameter Default Settings

DEFAULT MODE	BQ25616/616J
Charging voltage	VSET pin, 4.10 V/4.20 V/4.35 V
Charging current	I_{CHG} pin
Pre-charge current	5% of I_{CHG}
Termination current	5% of I_{CHG}
Temperature profile	JEITA (BQ25616J), Hot/Cold (BQ25616)
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled ($\overline{CE}$ is low)
- No thermistor fault on TS.
- No safety timer fault

The device automatically terminates the charging cycle when the charging current is below the termination threshold, the battery voltage is above the recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold, the device automatically starts a new charging cycle. After the charge is done, a toggle of the $\overline{CE}$ pin initiates a new charging cycle. Adapter removal and replug will also restart a charging cycle.

The STAT output indicates charging status: charging (LOW), charging complete or charge disable (HIGH), or charging fault (blinking).

9.3.7.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage, and top-off trickle charging. At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

Table 9-5. Charging Current Setting

V_{BAT}	CHARGING CURRENT	DEFAULT SETTING
< 2.2 V	I_{BAT_SHORT}	100 mA
2.2 V to 3 V	I_{PRECHG}	5% of ICHG pin setting
> 3 V	I_{CHG}	ICHG pin setting

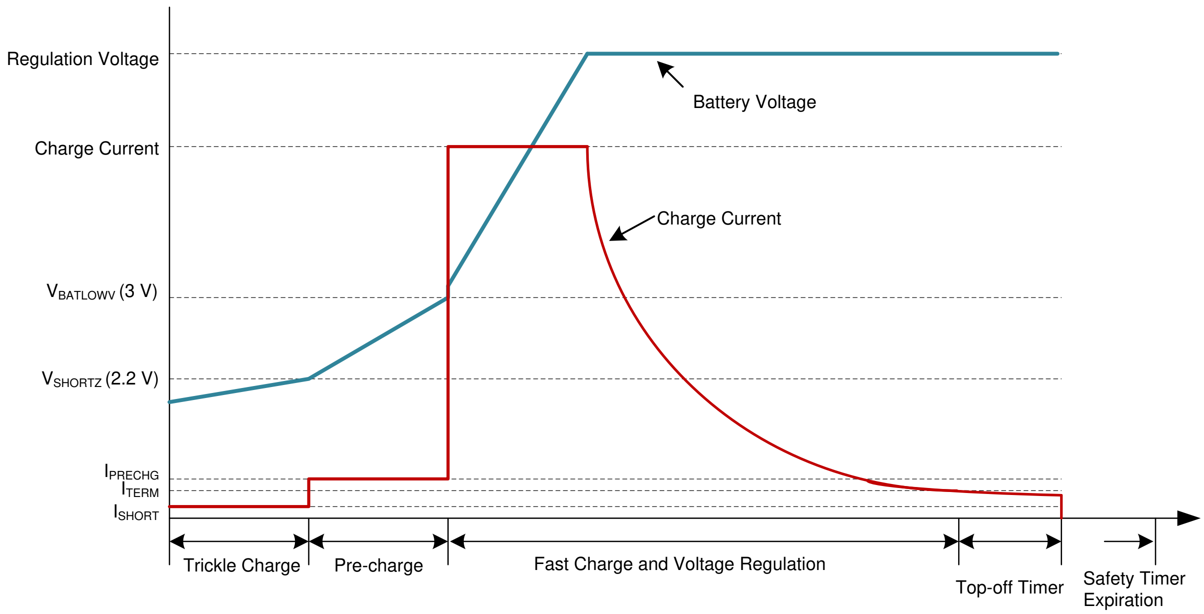


Figure 9-5. Battery Charging Profile

9.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, and the current is below termination current. After the charging cycle has completed, the BATFET turns off. STAT is asserted HIGH to indicate charging is done. The converter keeps running to power the system, and BATFET can turn on again to engage Section 9.3.6.3.

If the device is in IINDPM/VINDPM regulation, or thermal regulation, the actual charging current will be less than the termination value. In this case, termination is temporarily disabled.

When termination occurs, the STAT pin goes HIGH.

The top-off timer is reset at one of the following conditions:

1. Charge disable to enable
2. Charger enters termination

9.3.7.4 Thermistor Qualification

The device provides a single thermistor input for battery temperature monitoring.

9.3.7.4.1 JEITA Guideline Compliance During Charging Mode (BQ25616J)

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin, as a percentage of V_{REGN}, must be within the $V_{T1\_FALL\%}$ to $V_{T5\_RISE\%}$ thresholds. If the TS voltage percentage exceeds the T1-T5 range, the controller suspends charging, a TS fault is reported and waits until the battery temperature is within the T1-T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to 20% of I_{CHG}. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V.

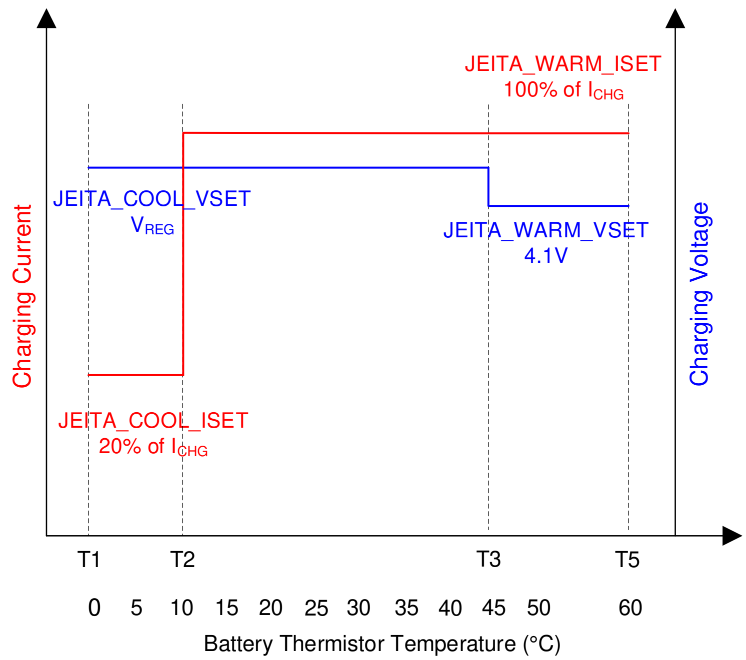


Figure 9-6. JEITA Profile (BQ25616J)

Equation 3 through Equation 4 describe how to calculate resistor divider values on the TS pin.

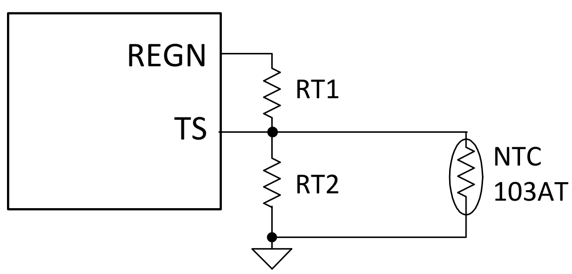


Figure 9-7. TS Pin Resistor Network

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \tag{3}$$

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - 1\right)} \tag{4}$$

In the equations above, $R_{NTC,\ T1}$ is the NTC thermistor resistance value at temperature T1 and $R_{NTC,\ T5}$ is the NTC thermistor resistance value at temperature T5. Selecting a 0°C to 60°C range for a Li-ion or Li-polymer battery then:

- $R_{NTC,T1}$ = 27.28 kΩ (0°C)
- $R_{NTC,T5}$ = 3.02 kΩ (60°C)
- RT1 = 5.3 kΩ
- RT2 = 31.14 kΩ

9.3.7.4.2 Hot/Cold Temperature Window During Charging Mode (BQ25616)

The BQ25616 provides simple Hot/Cold window T1-T3 with V_{REG} and I_{CHG} set on the pins. When RT1 is 5.3 KΩ and RT2 is 31.14 KΩ, T1 is 0°C and T3 is 45°C.

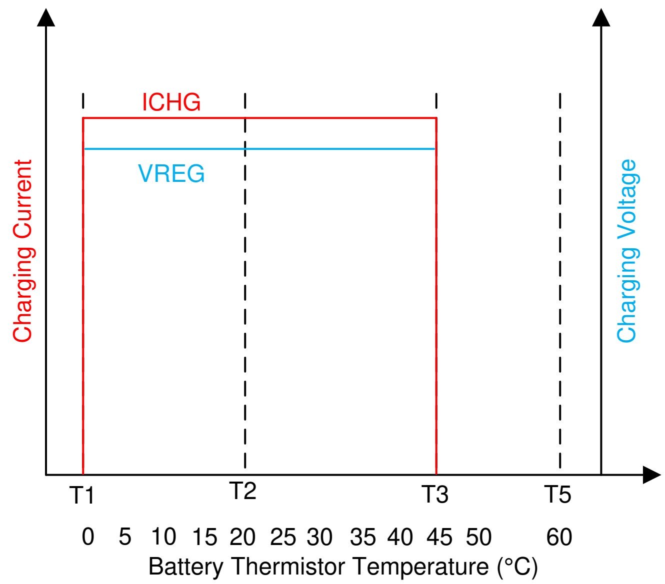


Figure 9-8. Hot/Cold Profile (BQ25616)

9.3.7.4.3 Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during Boost mode, the device monitors battery temperature to be within the V_{BCOLD} and V_{BHOT} thresholds. When RT1 is 5.3 kΩ and RT2 is 31.14 kΩ, T_{BCOLD} default is -19.5°C and T_{BHOT} default is 64°C. When the temperature is outside of the temperature thresholds, Boost mode is suspended.

9.3.7.5 Charging Safety Timer

The device has a built-in safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below the $V_{BATLOWV}$ threshold and 10 hours when the battery is higher than the $V_{BATLOWV}$ threshold. When the safety timer expires, the STAT pin is blinking at 1 Hz to report a safety timer expiration fault.

During IINDPM/VINDPM regulation, or thermal regulation, the safety timer counts at a half clock rate, because the actual charge current is likely below the setting. For example, if the charger is in input current regulation throughout the whole charging cycle, and the safety time is set to 10 hours, the safety timer will expire in 20 hours.

During faults of BAT_FAULT, NTC_FAULT that lead to charging suspend, the safety timer is suspended as well. Once the fault goes away, the timer resumes. If the user stops the current charging cycle, and starts it again, the timer gets reset (toggle of $\overline{CE}$ pin).

9.3.8 Status Outputs ($\overline{PG}$, STAT)

9.3.8.1 Power Good Indicator ($\overline{PG}$ Pin)

The $\overline{PG}$ pin goes LOW to indicate a good input source when:

- V_{VBUS} above V_{VBUS_UVLO}
- V_{VBUS} above battery (not in sleep)

- V_{VBUS} below V_{ACOV} threshold
- V_{VBUS} above $V_{POORSRC}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Completed Section 9.3.3.4

9.3.8.2 Charging Status Indicator (STAT)

The device indicates the charging state on the open drain STAT pin. The STAT pin can drive an LED.

Table 9-6. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging termination (top off timer may be running)	HIGH
Sleep mode, charge disable, Boost mode	HIGH
Charge suspend (input overvoltage, TS fault, safety timer fault, or system overvoltage)	Blinking at 1 Hz

9.3.9 Protections

9.3.9.1 Input Current Limit

The device's ILIM pin is to program maximum input current when D+/D– detection identifies an unknown adaptor plugged in. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INDPM} = \frac{K_{ILIM}}{R_{ILIM}} \tag{5}$$

9.3.9.2 Voltage and Current Monitoring in Buck Mode

9.3.9.2.1 Input Overvoltage Protection (ACOV)

This device integrates the functionality of an overvoltage protector. The device can be paired with an external N-channel FET to block input voltages in excess of the VBUS rating. For correct operation, connect the cathode of the body diode to the VAC node. Back-to-back body diodes between VAC and VBUS are not recommended and will prevent correct operation. The input voltage is sensed via the VAC pin and the ACDRV pin is used to control the external FET gate for protection. The default OVP threshold is 14.2 V. The ACOV circuit has a reaction time of 130 ns (typical) to turn off the external ACFET. Note that turning off the external ACFET takes longer and depends on its gate capacitance. In addition to turning off the external ACFET, an ACOV event immediately stops converter switching whether in buck or Boost mode. The device automatically resumes normal operation once the input voltage drops back below the OVP threshold. During ACOV, REGN LDO is on, and the device does not enter HIZ mode.

9.3.9.2.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during a load transient so that the components connected to the system are not damaged due to high voltage. The V_{SYS_OVP} threshold is about 300 mV above battery regulation voltage when battery charging is terminated. Upon SYSOVP, the converter stops switching immediately to clamp the overshoot. The charger pulls 30-mA I_{SYS_LOAD} discharge current to bring down the system voltage.

9.3.9.3 Voltage and Current Monitoring in Boost Mode

9.3.9.3.1 Boost Mode Overvoltage Protection

When PMID voltage rises above the regulation target and exceeds V_{BST_OVP}, the device stops switching immediately and the device exits Boost mode after the Boost mode OVP lasts for 12 ms. Meanwhile, if VAC (and VBUS when shorted to VAC) voltage exceeds V_{ACOV}, the device exits Boost mode as well.

9.3.9.4 Thermal Regulation and Thermal Shutdown

9.3.9.4.1 Thermal Protection in Buck Mode

Besides the battery temperature monitor on the TS pin, the device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds the thermal regulation limit (110°C), the device lowers down the charge current.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate.

Additionally, the device has thermal shutdown to turn off the converter and the BATFET when the IC surface temperature exceeds T_{SHUT} 150°C. The BATFET and converter are enabled to recover when IC temperature is 130°C.

9.3.9.4.2 Thermal Protection in Boost Mode

Besides the battery temperature monitor on the TS pin, the device monitors the internal junction temperature to provide thermal shutdown during Boost mode. When the IC junction temperature exceeds T_{SHUT} 150°C, Boost mode is disabled . When the IC junction temperature is below 145°C, the host can re-enable Boost mode.

9.3.9.5 Battery Protection

9.3.9.5.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above battery regulation voltage. When battery overvoltage occurs, the charger device immediately stops switching.

9.3.9.5.2 Battery Overdischarge Protection

When the battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET latches off to protect the battery from overdischarge. To recover from overdischarge latch-off, an input source plug-in is required at VAC/VBUS.

9.3.9.5.3 System Overcurrent Protection

When the system is shorted or significantly overloaded (I_{BAT} > I_{BATOP}) and the current exceeds BATFET overcurrent limit, the BATFET latched off. The BATFET latch can be reset with VBUS plug-in.

9.4 Device Functional Modes

The BQ25616/616J is a standalone device and therefore does not have I^2C functions.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

A typical application consists of the device configured as a stand-alone power path management device and a single cell battery charger for Li-ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

External ACFET is optional. When external OVP is not used, short the VBUS and VAC pins and allow the ACDRV pin to float.

10.2 Typical Applications

10.2.1 BQ25616/616J Application without External OVP

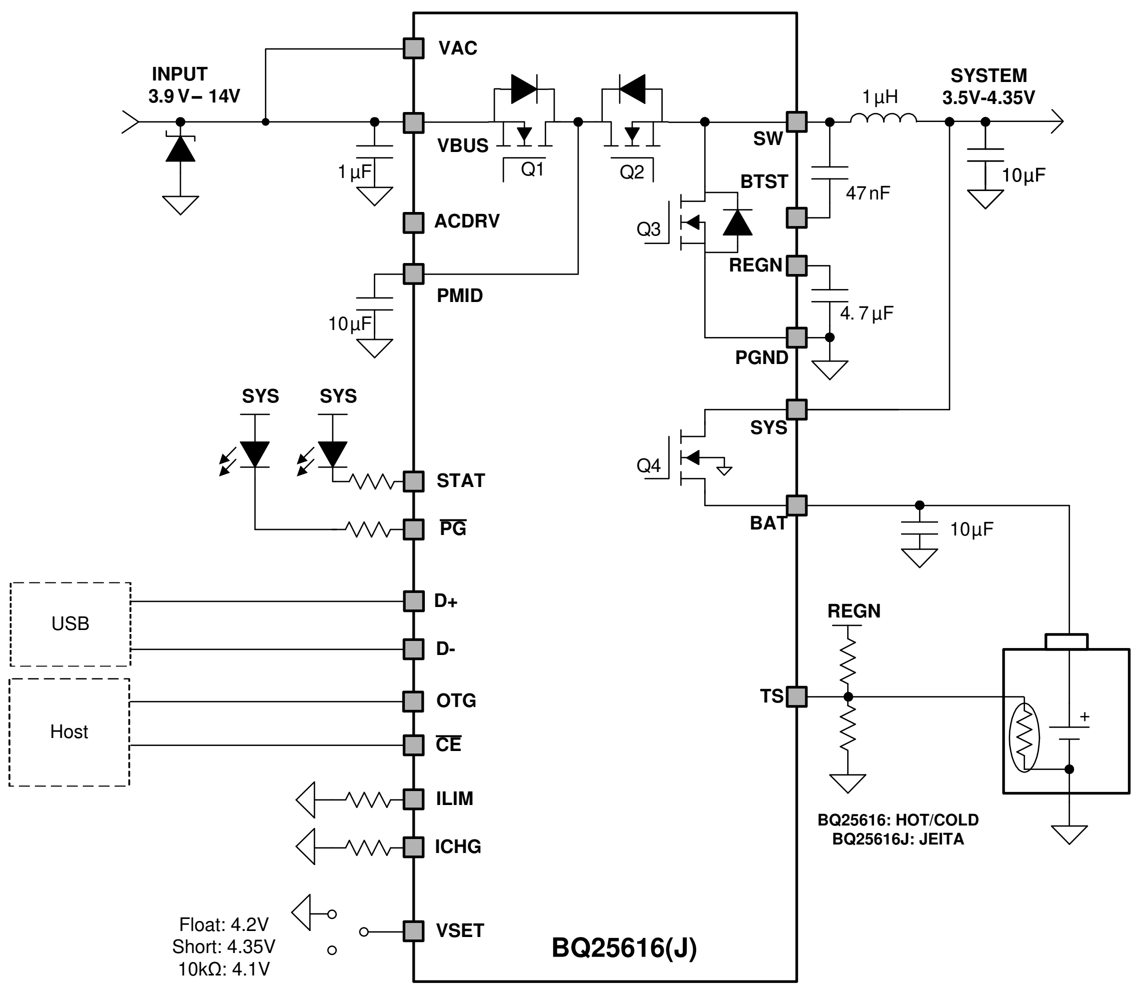


Figure 10-1. BQ25616/616J Application Diagram without External OVP

10.2.1.1 Design Requirements

For this design example, use the parameters shown in the table below.

Table 10-1. Design Parameters

PARAMETER	VALUE
V_{VBUS} voltage range	4-V to 13.5-V
Input current limit (D+/D– Detection)	2.4-A
Fast charge current limit (ICHG pin)	ICHG pin
Minimum system voltage	3.5-V
Battery regulation voltage (VSET pin)	4.2-V

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{6}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle (D = V_{BAT}/V_{VBUS}), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{fs \times L} \tag{7}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.1.2.2 Input Capacitor and Resistor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated using Equation 8.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \tag{8}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 12-V input voltage. Capacitance of minimum 10 µF is suggested for typical of 3-A charging current.

During high current output over 700 mA in boost mode, a 10 kΩ pull-down resistor on VBUS is recommended to keep VBUS low in case Q1 RBFET leakage gets high.

10.2.1.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 9 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{9}$$

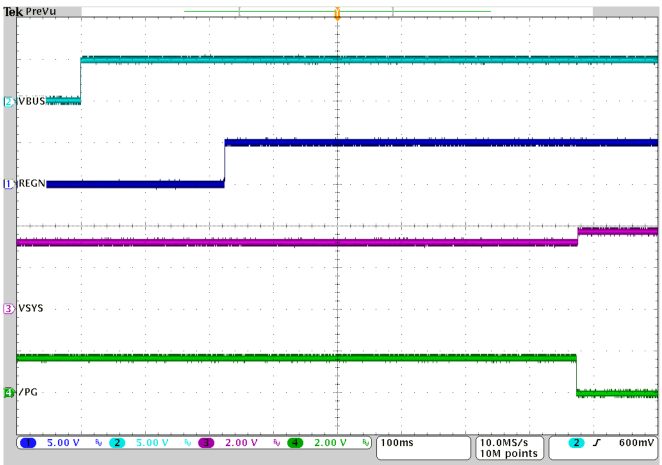
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

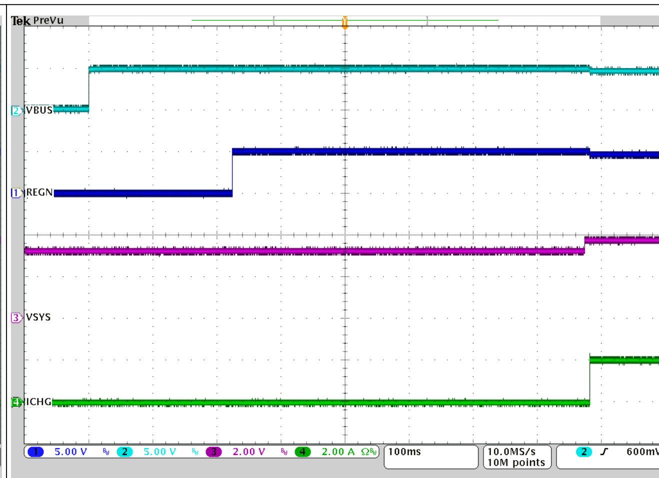
The charger device has internal loop compensation optimized for >10-μF ceramic output capacitance. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

10.2.1.3 Application Curves



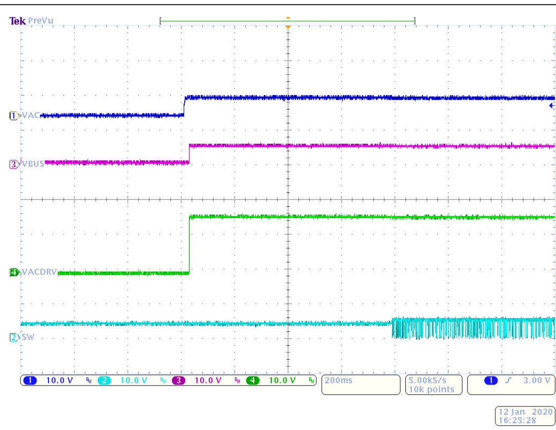
V_{VBUS} = 5 V V_{VBAT} = 3.2 V

Figure 10-2. Power-Up with Charge Disabled



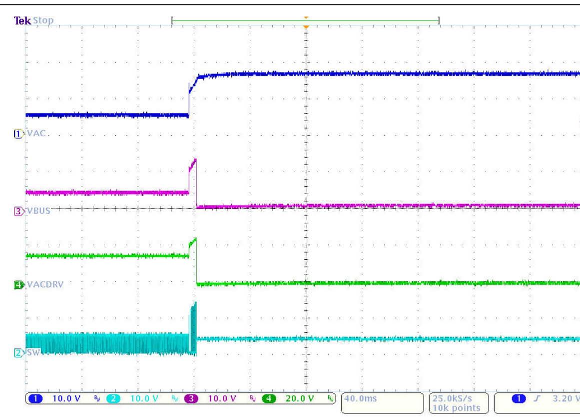
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

Figure 10-3. Power-Up with Charge Enabled



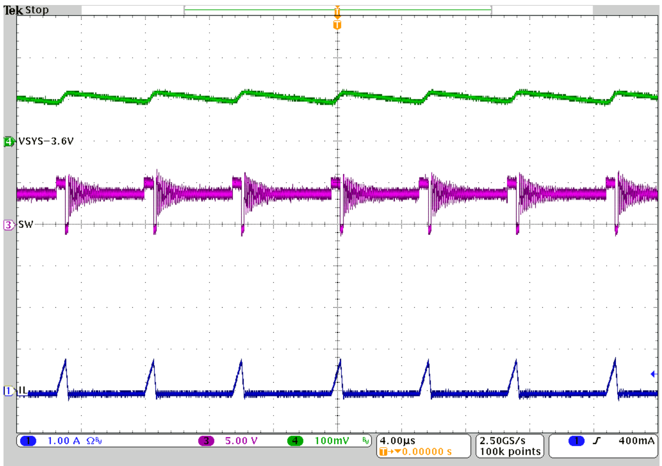
V_{VBUS} = 5 V V_{VBAT} = 3.2 V

Figure 10-4. OVPFET Turn-on during Power-Up



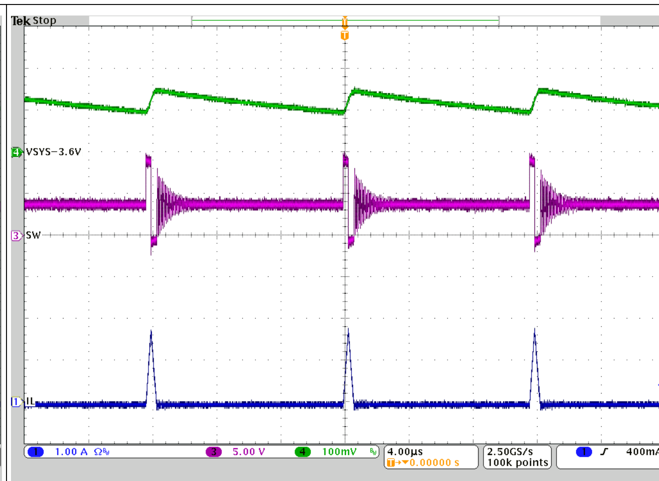
V_{VBUS} = 5 V to 17V V_{VBAT} = 3.2 V

Figure 10-5. OVPFET Turn-off during Input OVP



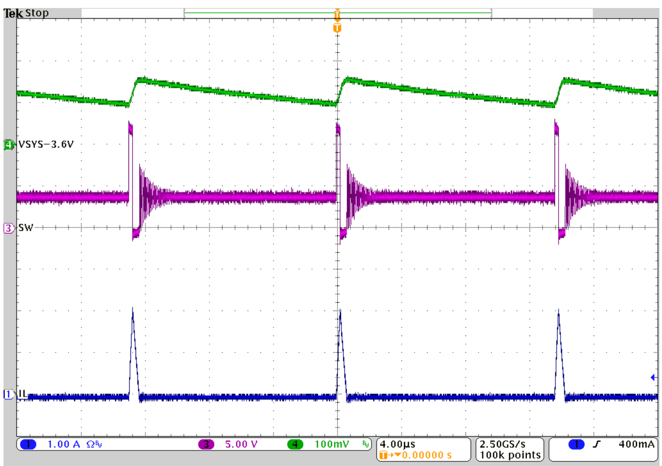
V_{VBUS} = 5 V
I_{SYS} = 50 mA
Charge Disabled

Figure 10-6. PFM Switching in Buck Mode



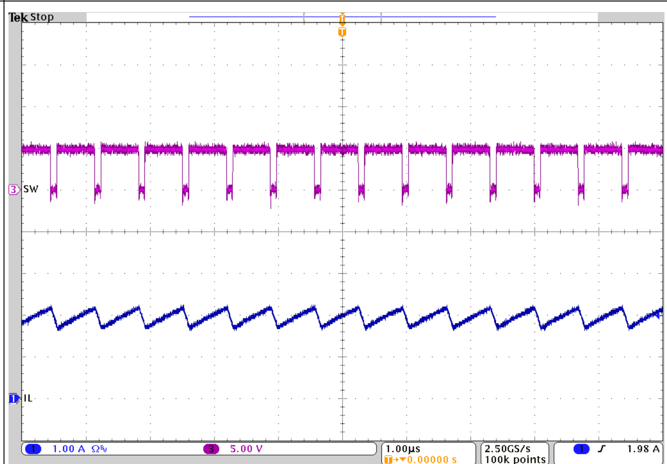
V_{VBUS} = 9 V
I_{SYS} = 50 mA
Charge Disabled

Figure 10-7. PFM Switching in Buck Mode



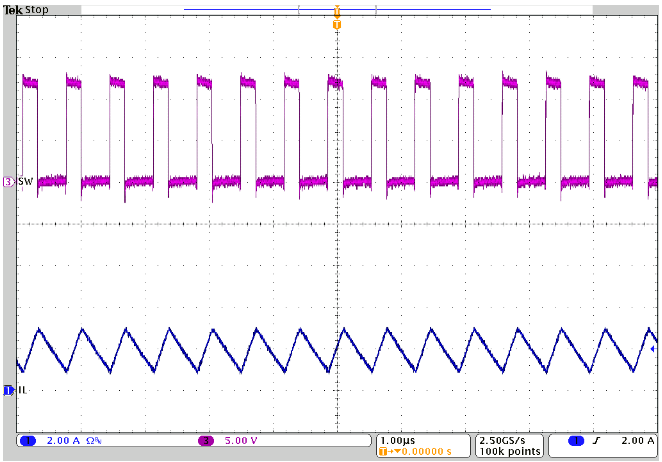
V_{VBUS} = 12 V
I_{SYS} = 50 mA
Charge Disabled

Figure 10-8. PFM Switching in Buck Mode



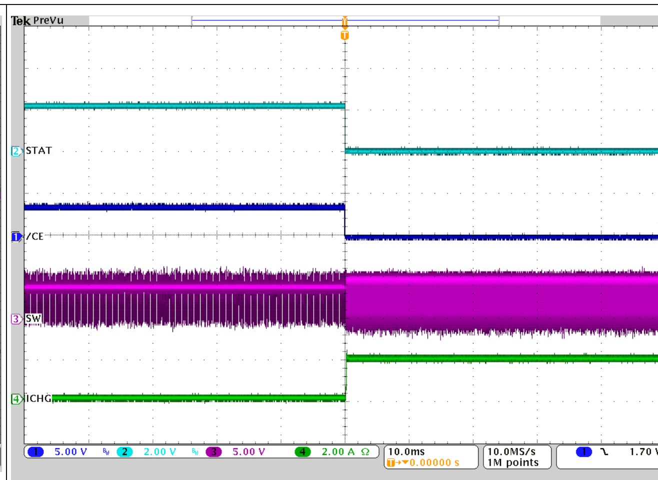
V_{VBUS} = 5 V
V_{VBAT} = 3.8 V
I_{CHG} = 2 A

Figure 10-9. PWM Switching in Buck Mode



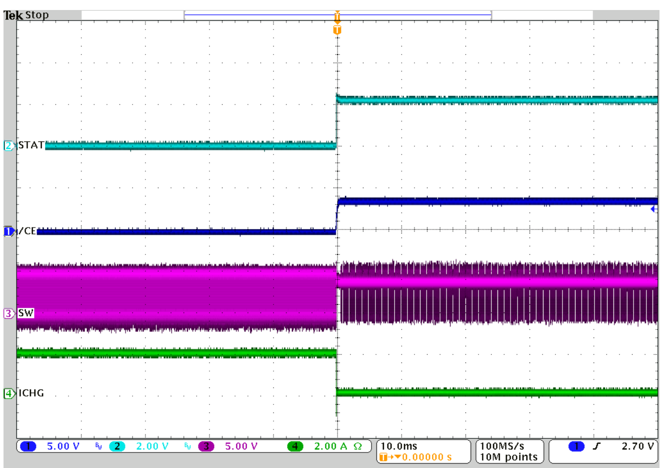
V_{VBUS} = 12 V V_{VBAT} = 3.8 V
I_{CHG} = 2 A

Figure 10-10. PWM Switching in Buck mode



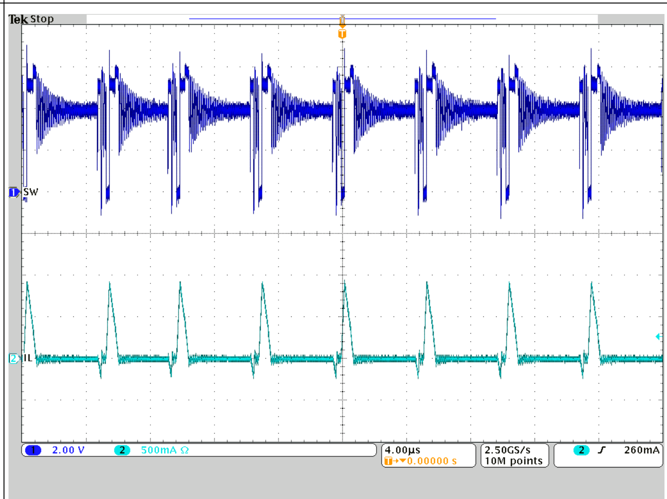
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

Figure 10-11. Charge Enable



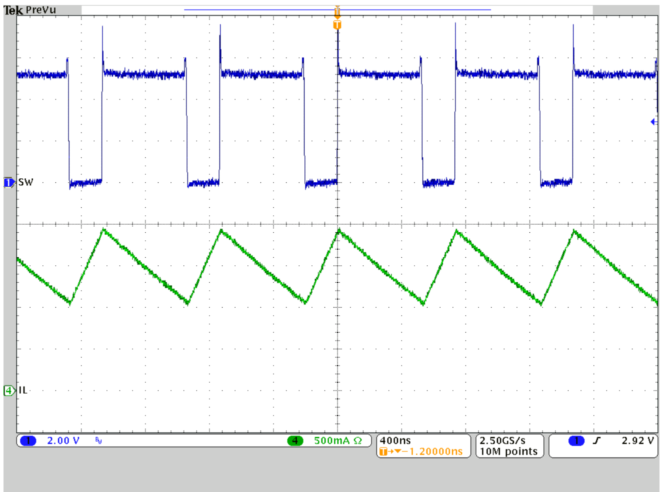
V_{VBUS} = 5 V V_{VBAT} = 3.2 V
I_{CHG} = 2 A

Figure 10-12. Charge Disable



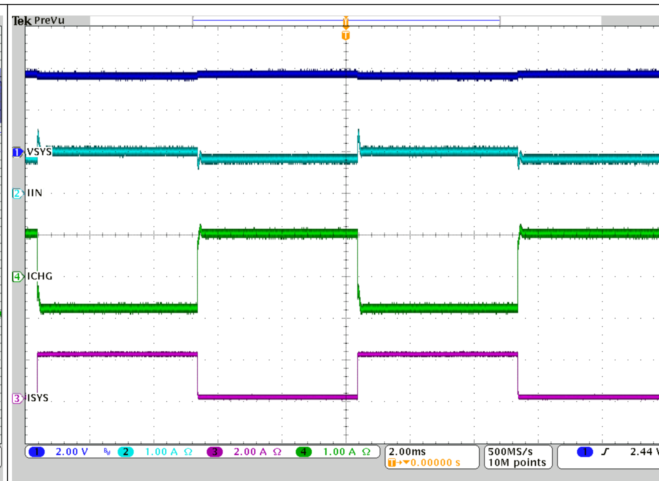
V_{VBAT} = 4 V
I_{LOAD}= 50 mA PFM Enabled

Figure 10-13. OTG Switching



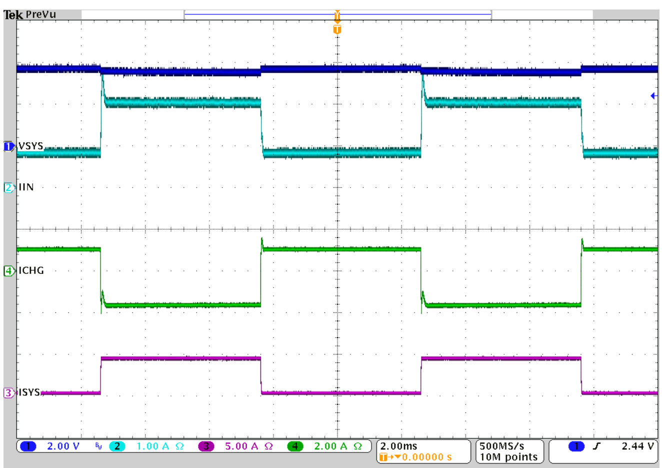
V_{VBAT} = 4 V
I_{LOAD}= 1 A
PFM Enabled

Figure 10-14. OTG Switching



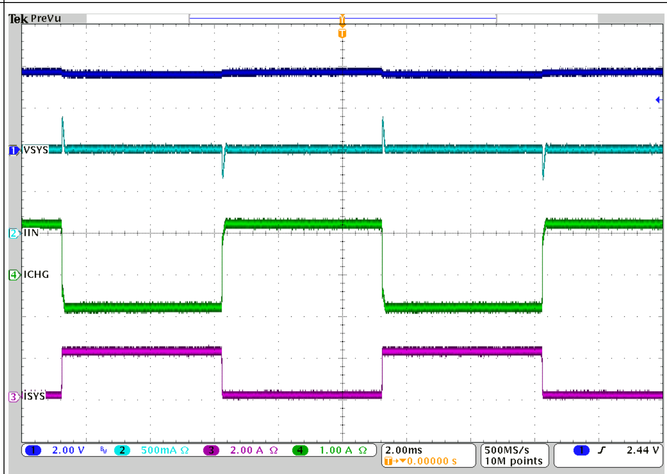
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 1 A

Figure 10-15. System Load Transient



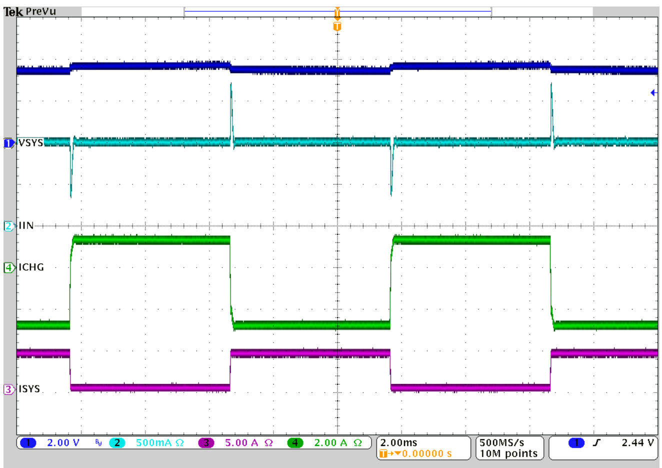
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 1 A

Figure 10-16. System Load Transient



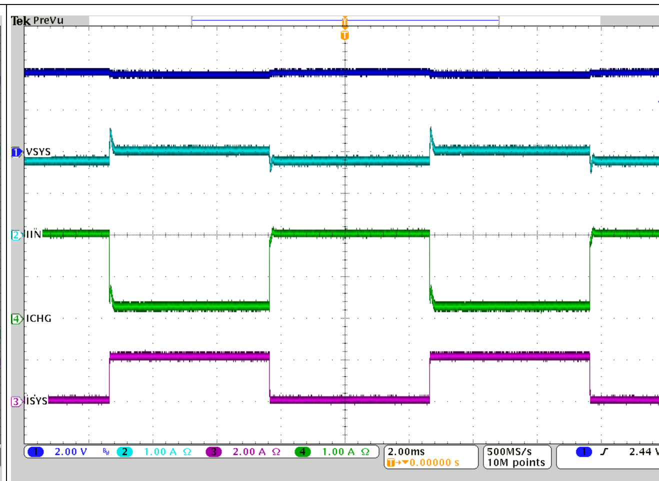
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

Figure 10-17. System Load Transient



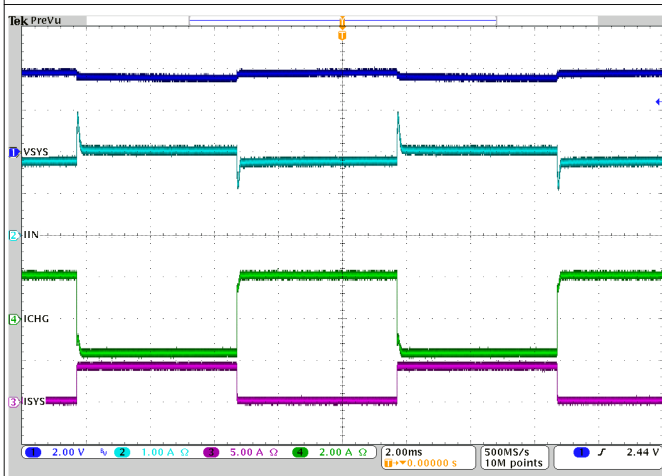
V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 1 A
I_{CHG} = 2 A

Figure 10-18. System Load Transient



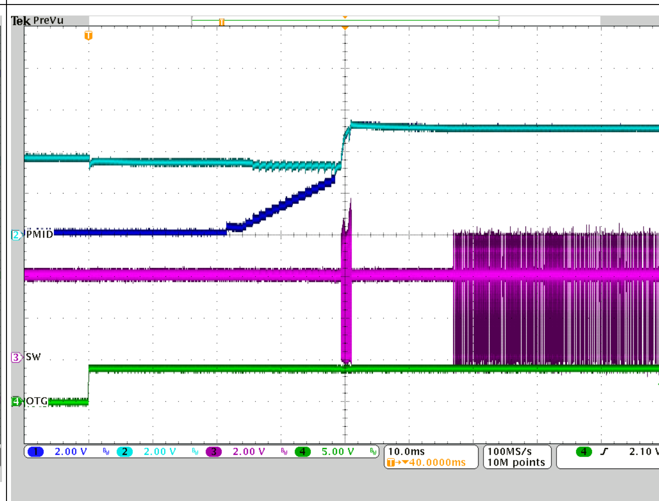
V_{VBUS} = 5 V
I_{SYS} from 0 A to 2 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 2 A

Figure 10-19. System Load Transient



V_{VBUS} = 5 V
I_{SYS} from 0 A to 4 A
V_{BAT} = 3.7 V
I_{INDPM} = 2 A
I_{CHG} = 2 A

Figure 10-20. System Load Transient



V_{BAT} = 3.8 V
C_{LOAD} = 470 µF

Figure 10-21. OTG Start-Up

10.2.2 BQ25616/616J Application with External OVP

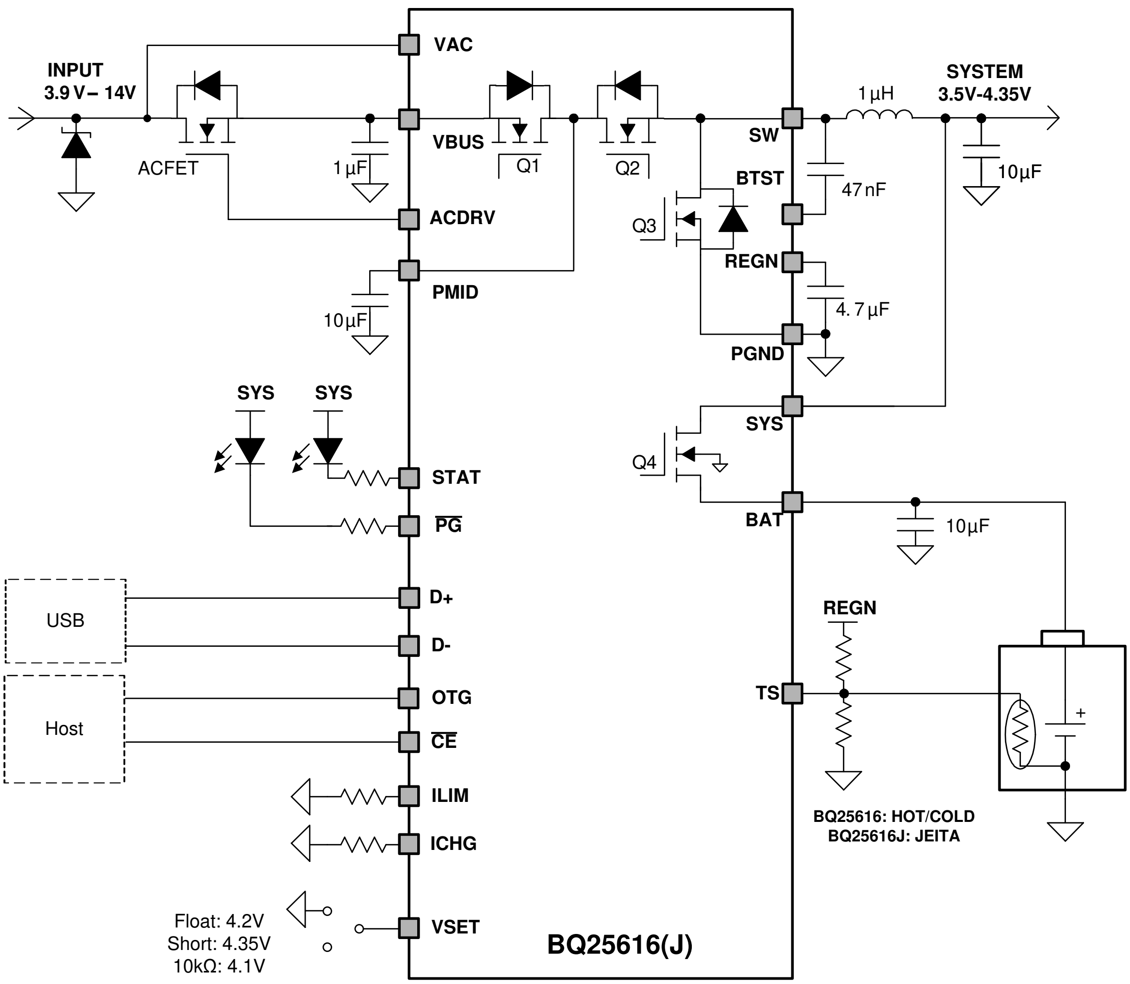


Figure 10-22. BQ25616/616J Application Diagram with External OVP

10.2.2.1 Design Requirements

Refer to Section 10.2.1.1 for design requirements.

10.2.2.2 Detailed Design Procedure

Refer to Section 10.2.1.2 for detailed design procedure.

10.2.2.3 Application Curves

Refer to Section 10.2.1.3 for application curves.

11 Power Supply Recommendations

In order to provide an output voltage on SYS, the battery charger requires a power supply between 4 V and 13.5 V input with at least a 100-mA current rating connected to VBUS and a single-cell Li-ion battery with battery voltage greater than V_{BAT_UVLOZ} connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize the high frequency current path loop (see Figure 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place an input capacitor as close as possible to the PMID pin and GND pin connections and use the shortest copper trace connection or GND plane. Add a 1-nF small size (such as 0402 or 0201) decoupling cap for the high frequency noise filter and EMI improvement.
2. Place the inductor input pin as close as possible to SW pin. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put the output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route the analog ground separately from power ground. Connect the analog ground and connect power ground separately. Connect the analog ground and power ground together using the thermal pad as the single ground connection point. Or use a 0-Ω resistor to tie the analog ground to power ground.
5. Use a single ground connection to tie the charger power ground to the charger analog ground just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place the decoupling capacitors next to the IC pins and make the trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

See the *BQ25618 BMS024 Evaluation Module User's Guide* and *BQ25619 BMS025 Evaluation Module EVM User's Guide* for the recommended component placement with trace and via locations. For the VQFN information, refer to *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

12.2 Layout Example

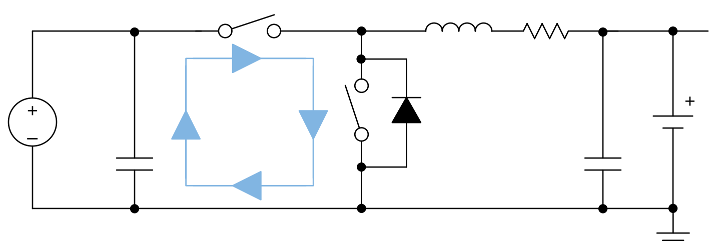


Figure 12-1. High Frequency Current Path

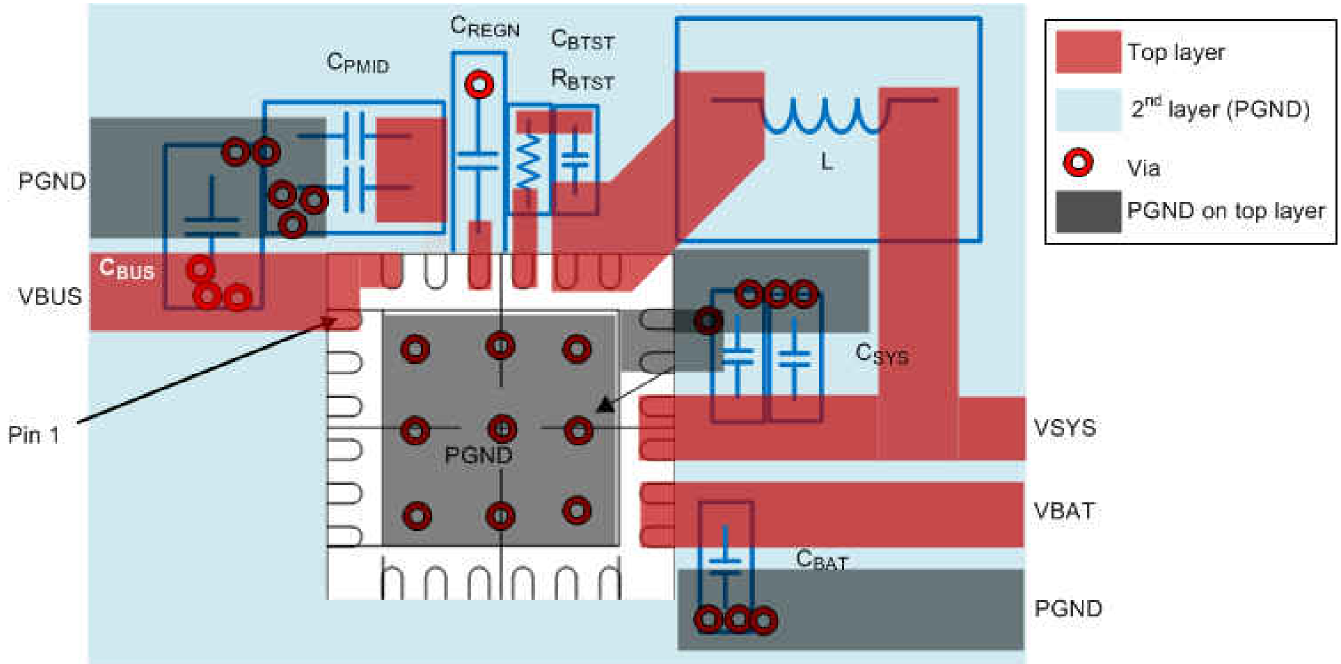


Figure 12-2. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *BQ25619 BMS025 Evaluation Module User's Guide*
- *BQ25618 BMS024 Evaluation Module User's Guide*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25616JRTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25616J	Samples
BQ25616JRTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25616J	Samples
BQ25616RTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25616	Samples
BQ25616RTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25616	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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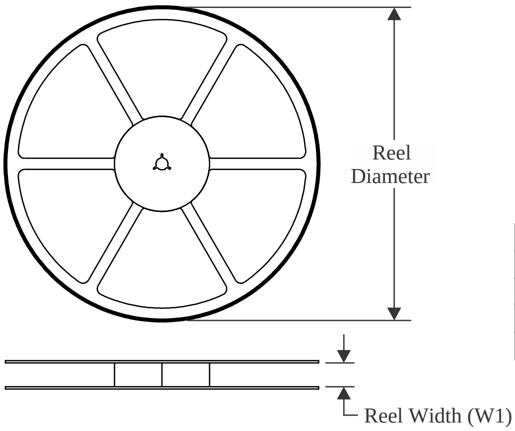
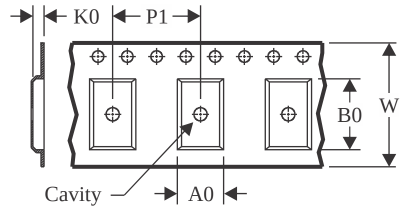
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

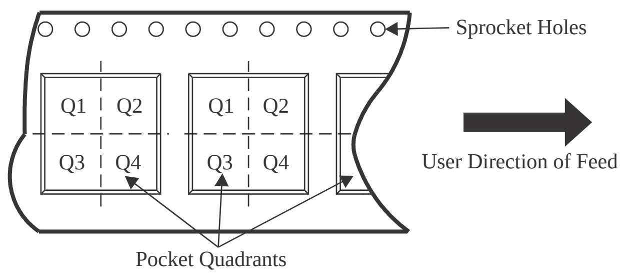


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

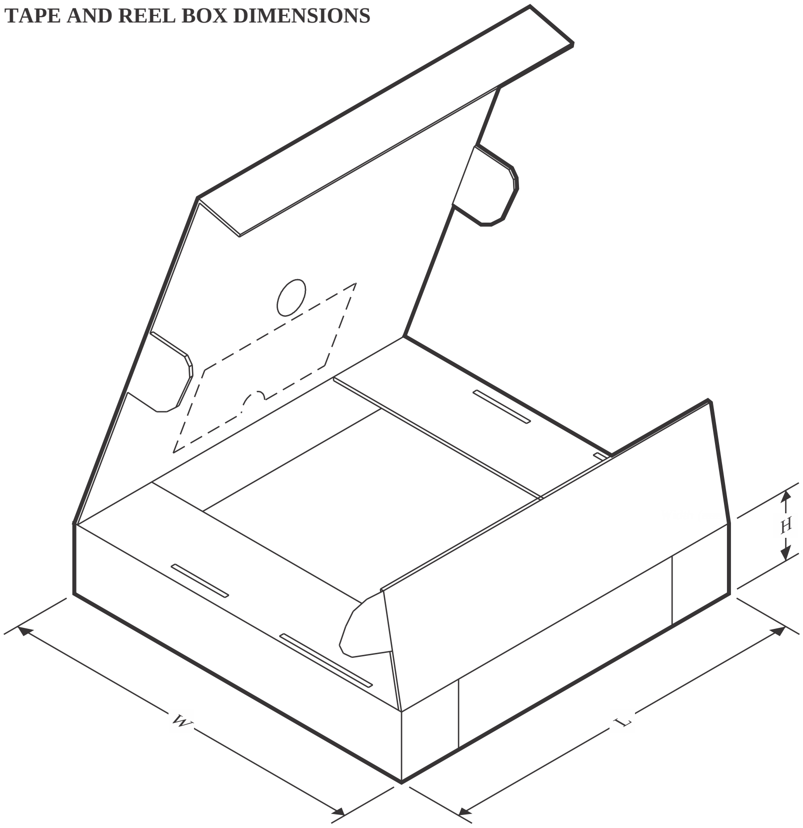
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25616JRTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25616JRTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25616RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25616RTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

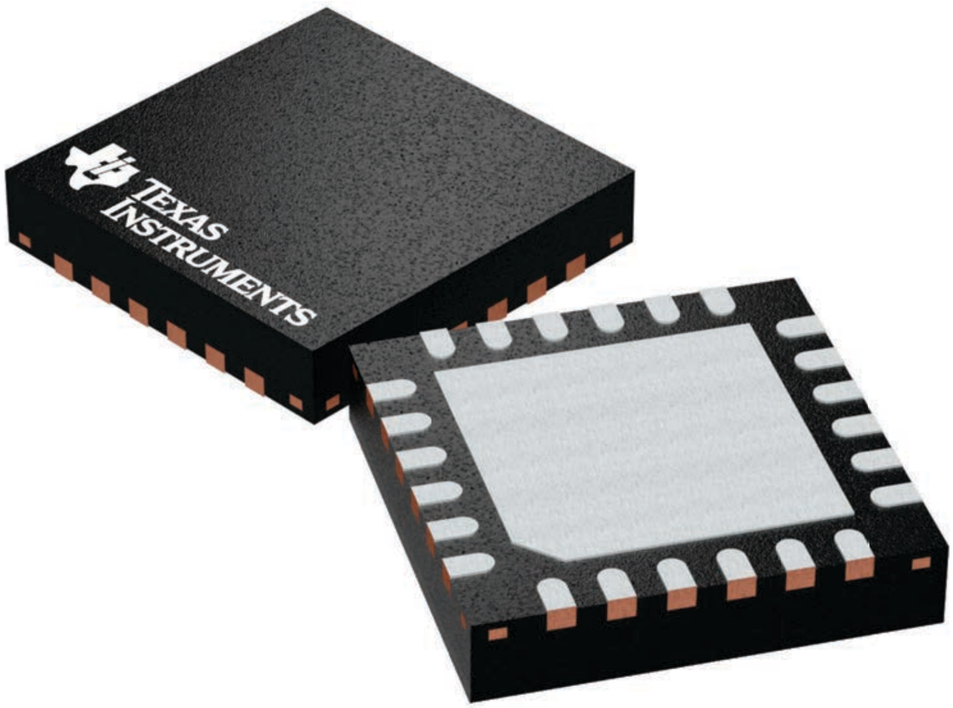
TAPE AND REEL BOX DIMENSIONS



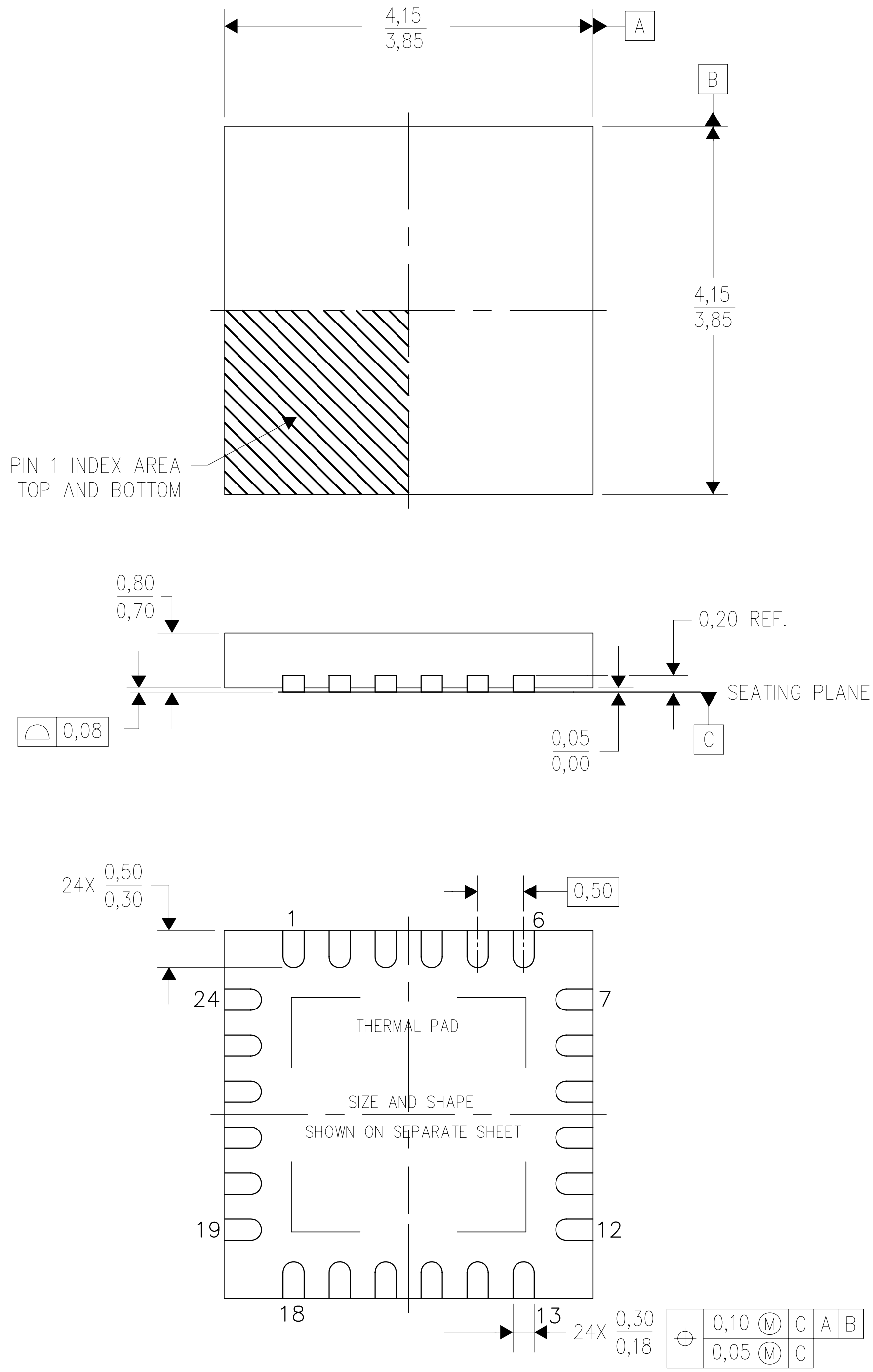
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25616JRTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
BQ25616JRTWT	WQFN	RTW	24	250	210.0	185.0	35.0
BQ25616RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
BQ25616RTWT	WQFN	RTW	24	250	210.0	185.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

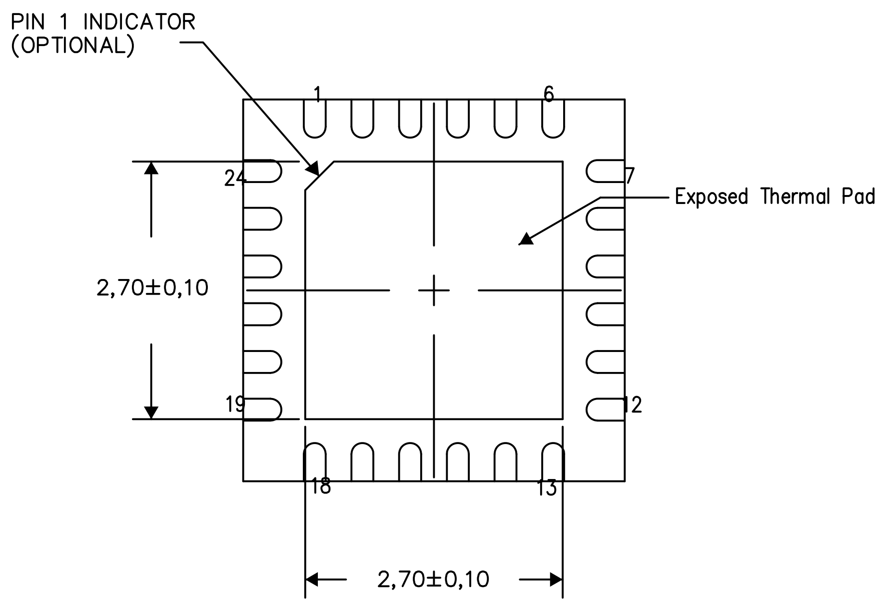
RTW (S-PWQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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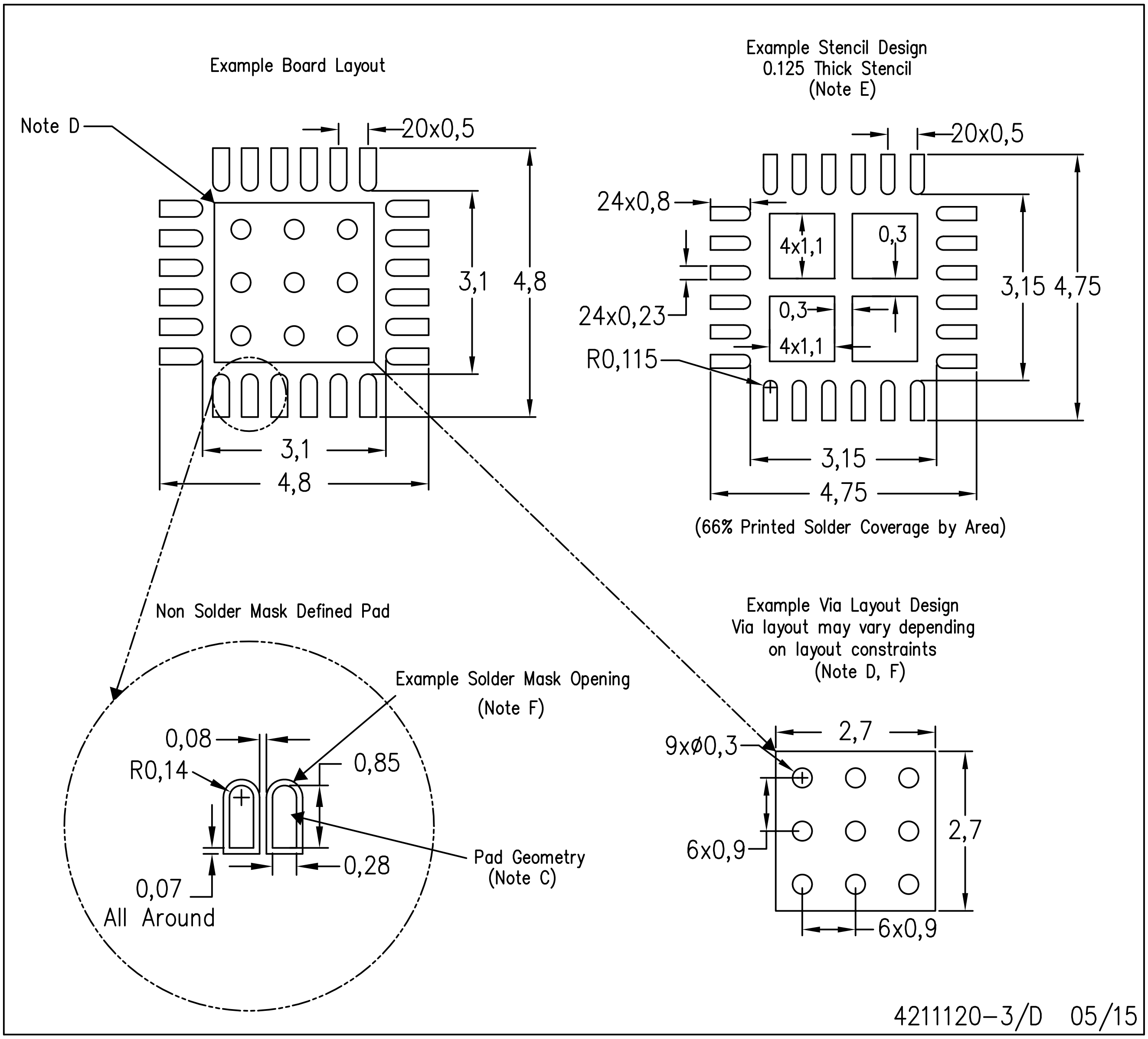
NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.