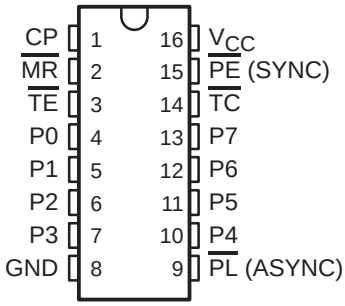
CD74HC40103-EP
HIGH-SPEED CMOS LOGIC
8-STAGE SYNCHRONOUS DOWN COUNTER

SCLS548 − DECEMBER 2003

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Synchronous or Asynchronous Preset**
- **Cascadable in Synchronous or Ripple Mode**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . 15 LSTTL Loads**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **V_{CC} Voltage = 2 V to 6 V**
- **High Noise Immunity N_{IL} or N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

M PACKAGE
(TOP VIEW)



description/ordering information

The CD74HC40103 is manufactured with high-speed silicon-gate technology and consists of an 8-stage synchronous down counter with a single output, which is active when the internal count is zero. The device contains a single 8-bit binary counter. Each device has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count ($\overline{TC}$) output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the clock (CP) output. Counting is inhibited when the terminal enable ($\overline{TE}$) input is high. $\overline{TC}$ goes low when the count reaches zero, if $\overline{TE}$ is low, and remains low for one full clock period.

When the synchronous preset enable ($\overline{PE}$) input is low, data at the P0−P7 inputs are clocked into the counter on the next positive clock transition, regardless of the state of $\overline{TE}$. When the asynchronous preset enable ($\overline{PL}$) input is low, data at the P0−P7 inputs asynchronously are forced into the counter, regardless of the state of the $\overline{PE}$, $\overline{TE}$, or CP inputs. Inputs P0−P7 represent a single 8-bit binary word for the CD74HC40103. When the master reset ($\overline{MR}$) input is low, the counter asynchronously is cleared to its maximum count of 255_{10}, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC − M	Tape and reel	CD74HC40103QM96EP	HC40103QEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

If all control inputs except $\overline{TE}$ are high at the time of zero count, the counters jump to the maximum count, giving a counting sequence of 100_{16} or 256_{10} clock pulses long.

The CD74HC40103 may be cascaded using the $\overline{TE}$ input and the $\overline{TC}$ output in either synchronous or ripple mode. These circuits have the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits and can drive up to ten LSTTL loads.

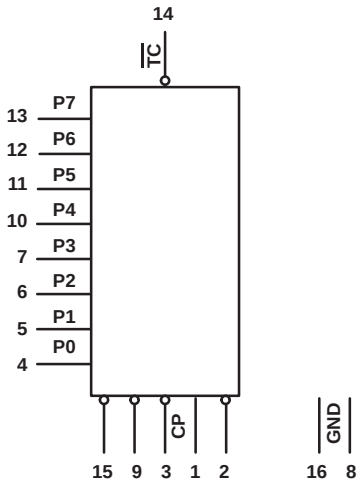
FUNCTION TABLE†

CONTROL INPUTS				PRESET MODE	ACTION
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
H	H	H	H	Synchronous	Inhibit counter
H	H	H	L		Count down
H	H	L	X		Preset on next positive clock transition
H	L	X	X	Asynchronous	Preset asynchronously
L	X	X	X		Clear to maximum count

† See Figure 2 for timing diagram.

NOTE: H = high voltage level, L = low voltage level, X = don't care
Clock connected to clock input
Synchronous operation: changes occur on negative-to-positive clock transitions.
Load inputs: MSB = P7, LSB = P0

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . . ±20 mA
Source or sink current per output pin, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 73°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		−40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I_O (mA)	V_{CC}	T_A = 25°C		MIN	MAX	UNIT
					MIN	MAX			
V_{OH}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	−0.02	2 V	1.9		1.9		V
			−0.02	4.5 V	4.4		4.4		
			−0.02	6 V	5.9		5.9		
		TTL loads	−4	4.5 V	3.98		3.7		
			−5.2	6 V	5.48		5.2		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	CMOS loads	0.02	2 V		0.1		0.1	V
			0.02	4.5 V		0.1		0.1	
			0.02	6 V		0.1		0.1	
		TTL loads	4	4.5 V		0.26		0.4	
			5.2	6 V		0.26		0.4	
I_I	$V_I = V_{CC}$ or GND			6 V		±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND		0	6 V		8		160	µA
C_{IN}	C_L = 50 pF					10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			V_{CC}	T_A = 25°C		MIN	MAX	UNIT
				MIN	MAX			
t_w	Pulse duration	CP	2 V	165		250		ns
			4.5 V	33		50		
			6 V	28		43		
		$\overline{PL}$	2 V	125		190		
			4.5 V	25		38		
			6 V	21		32		
		$\overline{MR}$	2 V	125		190		
			4.5 V	25		38		
			6 V	21		32		
f_{max}	CP frequency (see Note 4)		2 V	3		2		MHz
			4.5 V	15		10		
			6 V	18		12		
t_{su}	Setup time	P to CP	2 V	100		150		ns
			4.5 V	20		30		
			6 V	17		26		
		$\overline{PE}$ to CP	2 V	75		110		
			4.5 V	15		22		
			6 V	13		19		
		$\overline{TE}$ to CP	2 V	150		225		
			4.5 V	30		45		
			6 V	26		38		
		To CP, $\overline{MR}$ inactive	2 V	50		75		
			4.5 V	10		15		
			6 V	9		13		
t_h	Hold time	P to CP	2 V	5		5		ns
			4.5 V	5		5		
			6 V	5		5		
		$\overline{TE}$ to CP	2 V	0		0		
			4.5 V	0		0		
			6 V	0		0		
		$\overline{PE}$ to CP	2 V	2		2		
			4.5 V	2		2		
			6 V	2		2		

NOTE 4: Noncascaded operation only. With cascaded counters, clock-to-terminal count propagation delays, count enables ($\overline{PE}$ or $\overline{TE}$) to clock setup times, and count enables ($\overline{PE}$ or $\overline{TE}$) to clock hold times determine maximum clock frequency. For example, with these HC devices:

$$\text{CP } f_{max} = \frac{1}{\text{CP to } \overline{TC} \text{ prop delay} + \overline{TE} \text{ to CP setup time} + \overline{TE} \text{ to CP hold time}} = \frac{1}{60 + 30 + 0} \approx 11 \text{ MHz}$$

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

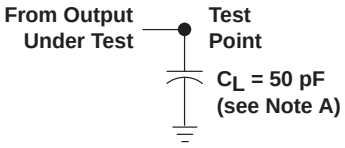
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
					MIN	TYP	MAX			
t_{pd}	CP	$\overline{TC}$ (asynchronous preset)	C_L = 50 pF	2 V			300		450	ns
				4.5 V			60		90	
				6 V			51		77	
			C_L = 15 pF	5 V		25				
		$\overline{TC}$ (synchronous preset)	C_L = 50 pF	2 V			300		450	
				4.5 V			60		90	
				6 V			51		77	
			C_L = 15 pF	5 V		25				
	$\overline{TE}$	$\overline{TC}$	C_L = 50 pF	2 V			200		300	
				4.5 V			40		60	
				6 V			34		51	
			C_L = 15 pF	5 V		17				
	$\overline{PL}$	$\overline{TC}$	C_L = 50 pF	2 V			275		415	
				4.5 V			55		83	
				6 V			47		71	
			C_L = 15 pF	5 V		23				
	$\overline{MR}$	$\overline{TC}$	C_L = 50 pF	2 V			275		415	
				4.5 V			55		83	
				6 V			47		71	
			C_L = 15 pF	5 V		23				
t_t			C_L = 50 pF	2 V			75		110	ns
				4.5 V			15		22	
				6 V			13		19	
f_{max}	CP		C_L = 15 pF	5 V		25				MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

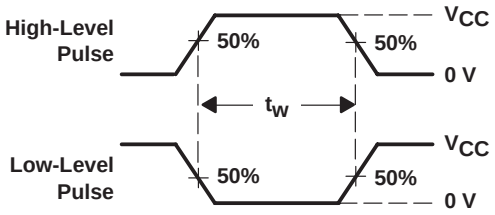
PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 5)	25	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_i) + (C_L \times V_{CC}^2 \times f_O)$
f_I = input frequency
f_O = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

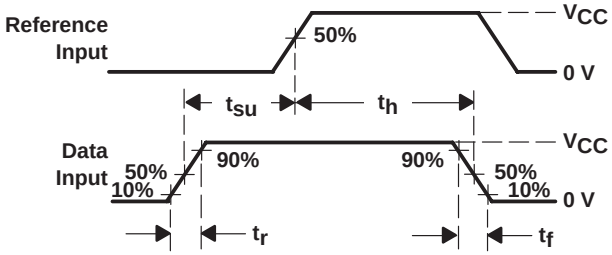
PARAMETER MEASUREMENT INFORMATION



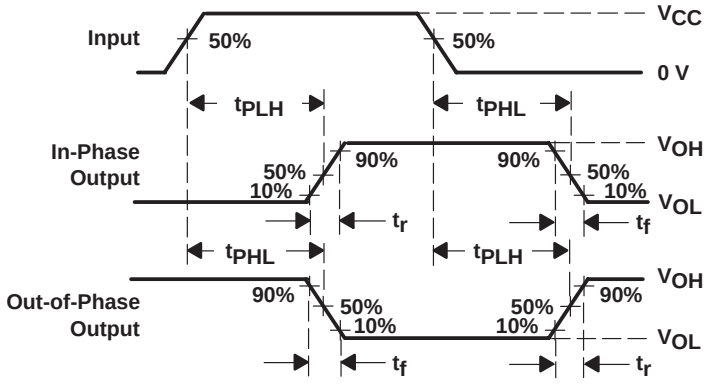
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

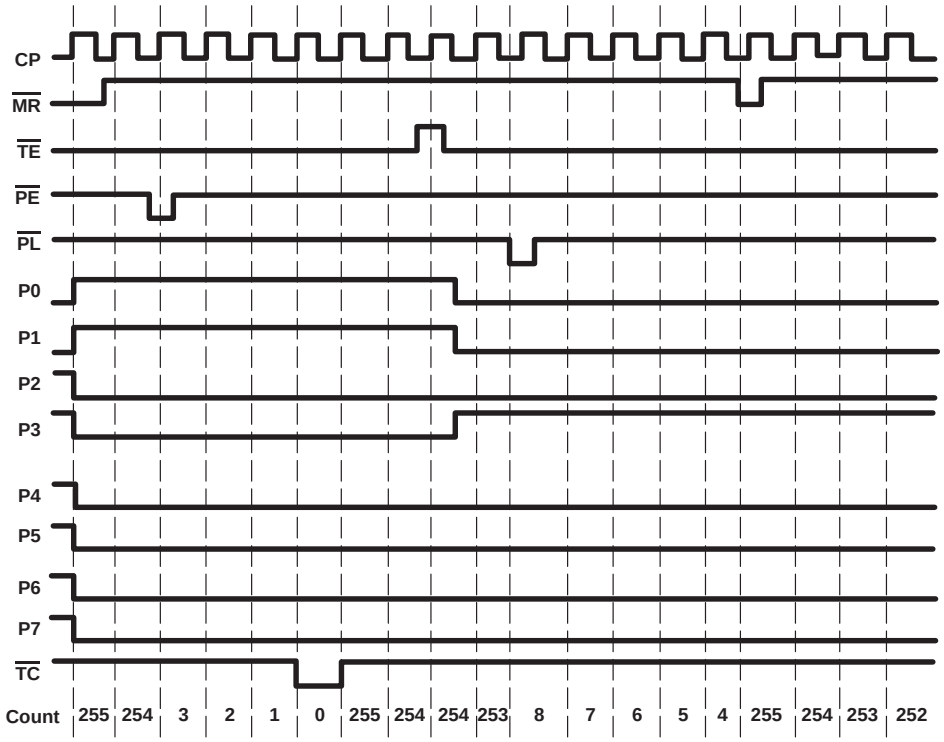


Figure 2. Timing Diagram

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC40103QM96EP	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC40103QEP
CD74HC40103QM96EP.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC40103QEP
V62/04702-01XE	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC40103QEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD74HC40103-EP :

- Catalog : CD74HC40103

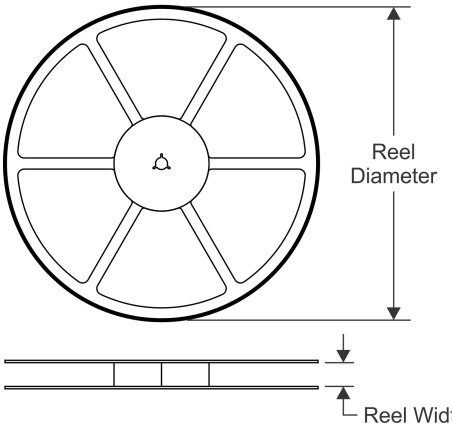
- Military : CD54HC40103

NOTE: Qualified Version Definitions:

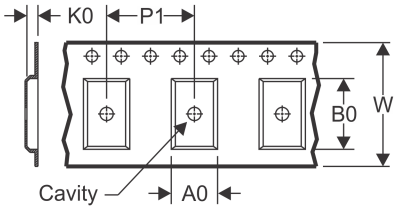
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

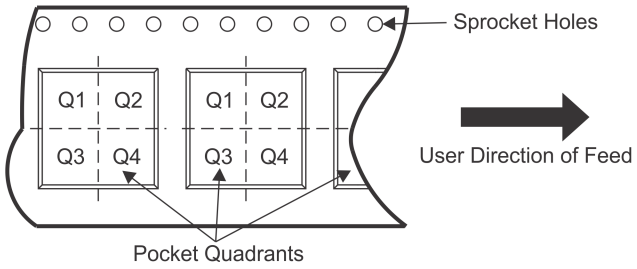


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

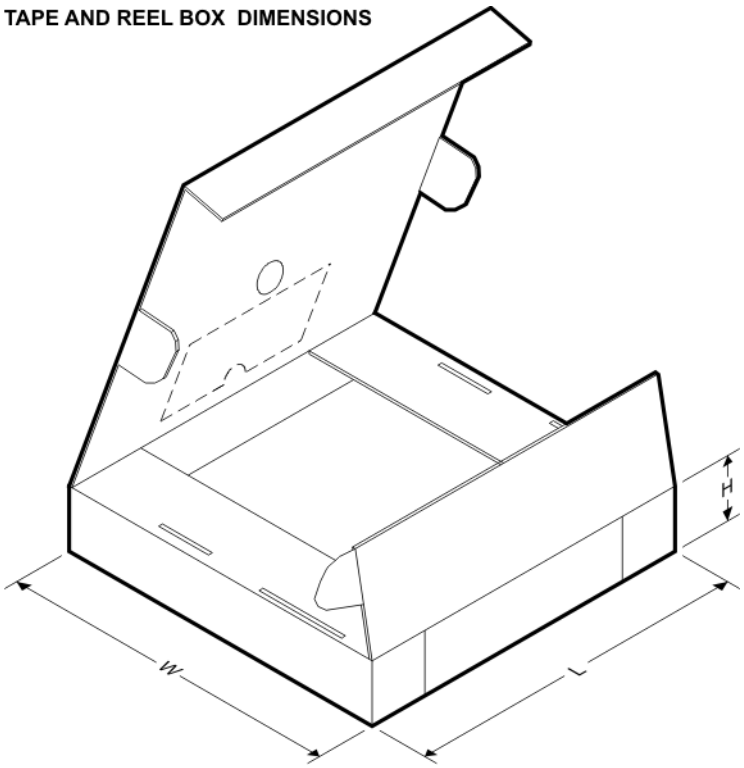
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103QM96EP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

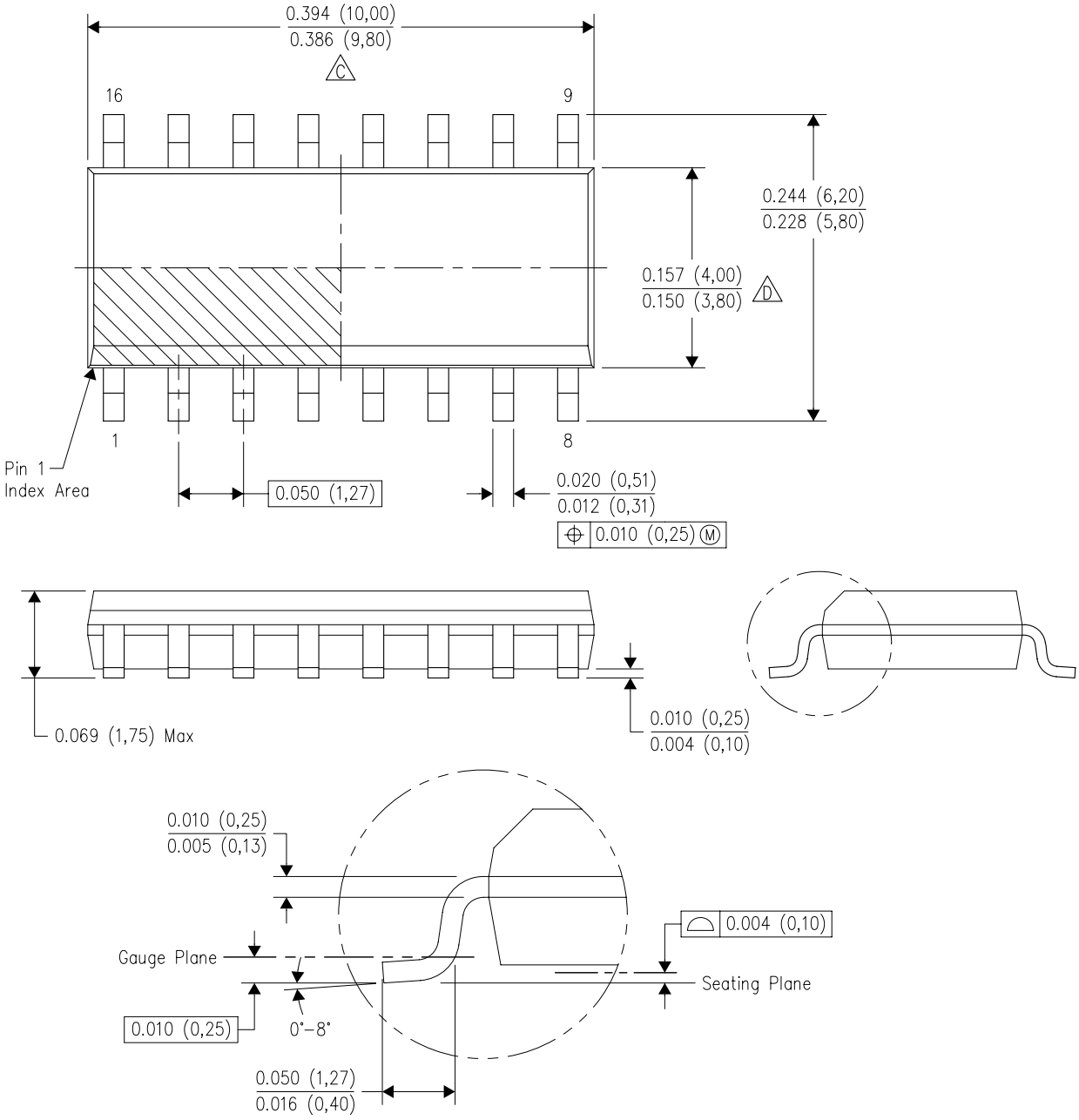
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40103QM96EP	SOIC	D	16	2500	340.5	336.1	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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