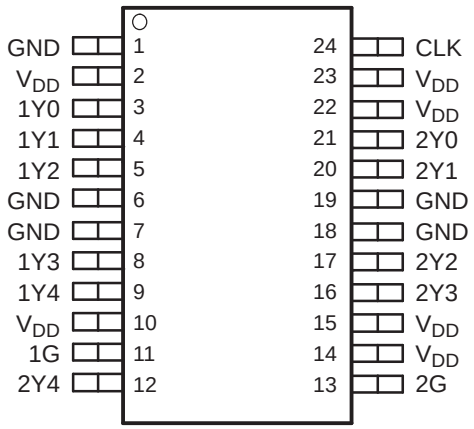
2.5-V TO 3.3-V HIGH-PERFORMANCE CLOCK BUFFER

Check for Samples: CDCVF2310-EP

FEATURES

- **High-Performance 1:10 Clock Driver**
- **Operates up to 200 MHz at V_{DD} 3.3 V**
- **Pin-to-Pin Skew < 100 ps at V_{DD} 3.3 V**
- **V_{DD} Range: 2.3 V to 3.6 V**
- **Output Enable Glitch Suppression**
- **Distributes One Clock Input to Two Banks of Five Outputs**
- **25-Ω On-Chip Series Damping Resistors**
- **Packaged in 24-Pin TSSOP**

PW PACKAGE
(TOP VIEW)



APPLICATIONS

- **General-Purpose Applications**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Military (–55°C to 125°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

(1) Custom temperature ranges available

DESCRIPTION

The CDCVF2310 is a high-performance, low-skew clock buffer that operates up to 200 MHz. Two banks of five outputs each provide low-skew copies of CLK. After power up, the default state of the outputs is low regardless of the state of the control pins. For normal operation, the outputs of bank 1Y[0:4] or 2Y[0:4] can be placed in a low state when the control pins (1G or 2G, respectively) are held low and a negative clock edge is detected on the CLK input. The outputs of bank 1Y[0:4] or 2Y[0:4] can be switched into the buffer mode when the control pins (1G and 2G) are held high and a negative clock edge is detected on the CLK input. The device operates in a 2.5-V and 3.3-V environment. The built-in output enable glitch suppression ensures a synchronized output enable sequence to distribute full period clock signals.

The CDCVF2310 is characterized for operation from –55°C to 125°C.

Table 1. ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	TSSOP - PW	CDCVF2310MPWREP	CKV2310EP	V62/13603-01XE
		CDCVF2310MPWEP	CKV2310EP	V62/13603-01XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

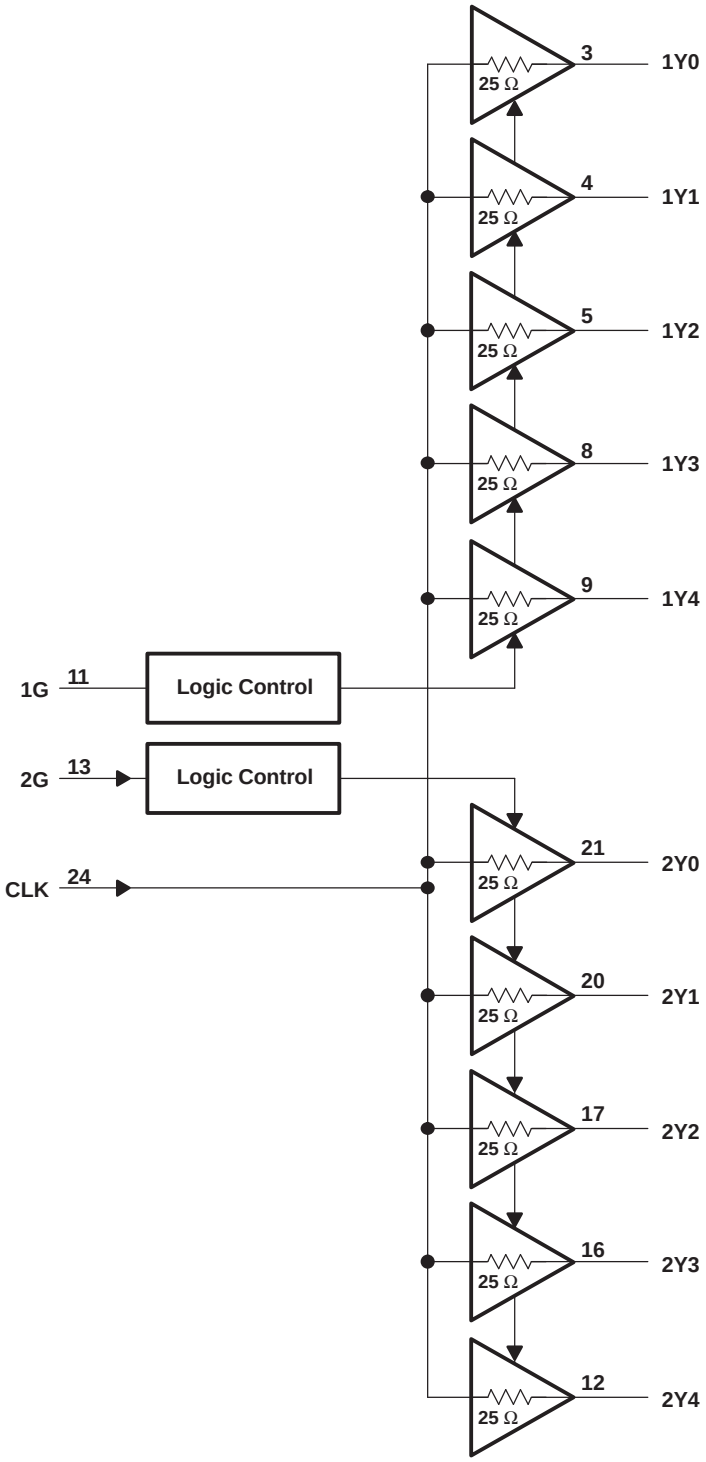


Table 2. FUNCTION TABLE

INPUT			OUTPUT	
1G	**2G**	**CLK**	**1Y[0:4]**	**2Y[0:4]**
L	L	↓	L	L
H	L	↓	CLK(1)	L
L	H	↓	L	CLK(1)
H	H	↓	CLK(1)	CLK(1)

(1) After detecting one negative edge on the CLK input, the output follows the input CLK if the control pin is held high.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
1G	11	I	Output enable control for 1Y[0:4] outputs. This output enable is active-high, meaning the 1Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
2G	13	I	Output enable control for 2Y[0:4] outputs. This output enable is active-high, meaning the 2Y[0:4] clock outputs follow the input clock (CLK) if this pin is logic high.
1Y[0:4]	3, 4, 5, 8, 9	O	Buffered output clocks
2Y[0:4]	21, 20, 17, 16, 12	O	Buffered output clocks
CLK	24	I	Input reference frequency
GND	1, 6, 7, 18, 19		Ground
V_{DD}	2, 10, 14, 15, 22, 23		DC power supply, 2.3 V – 3.6 V

ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted) (1)

Supply voltage range, V_{DD}	–0.5 V to 4.6 V
Input voltage range, V_I (2) (3)	–0.5 V to V_{DD} + 0.5 V
Output voltage range, V_O (2) (3)	–0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I> V_{DD})	±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD})	±50 mA
Storage temperature range T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This value is limited to 4.6 V maximum.

THERMAL INFORMATION

THERMAL METRIC[1]		CDCVF2310 PW 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	91.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	31.2	
θ_{JB}	Junction-to-board thermal resistance[4]	46.4	
ψ_{JT}	Junction-to-top characterization parameter[5]	1.5	
ψ_{JB}	Junction-to-board characterization parameter[6]	45.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS [1]

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.3	2.5		V
			3.3	3.6	
Low-level input voltage, V_{IL}	V_{DD} = 3 V to 3.6 V			0.8	V
	V_{DD} = 2.3 V to 2.7 V			0.7	
High-level input voltage, V_{IH}	V_{DD} = 3 V to 3.6 V	2			V
	V_{DD} = 2.3 V to 2.7 V	1.7			
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Low-level output current, I_{OL}	V_{DD} = 3 V to 3.6 V			12	mA
	V_{DD} = 2.3 V to 2.7 V			6	
Operating junction temperature, T_J		–55		125	°C

(1) Unused inputs must be held high or low to prevent them from floating.

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = –18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	µA
I_{DD} (2)	Static device current	CLK = 0 V or V_{DD},	I_O = 0 mA			100	µA
C_I	Input capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.5		pF
C_O	Output capacitance	V_{DD} = 2.3 V to 3.6 V,	V_I = 0 V or V_{DD}		2.8		pF
V_{DD} = 3.3 V ±0.3 V							
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V	I_{OH} = –12 mA	2.1			
			I_{OH} = –6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = –100 µA			0.2	V
		V_{DD} = 3 V	I_{OL} = 12 mA			0.8	
			I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–36		
		V_{DD} = 3.6 V,	V_O = 3.135 V			–14	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	28			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		36		
		V_{DD} = 3.6 V,	V_O = 0.4 V			14	
V_{DD} = 2.5 V ±0.2 V							
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = –100 µA	V_{DD} – 0.2			V
		V_{DD} = 2.3 V	I_{OH} = –6 mA	1.8			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 µA			0.2	V
		V_{DD} = 2.3 V	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 2.3 V,	V_O = 1 V	–15			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		–25		
		V_{DD} = 2.7 V,	V_O = 2.375 V			–10	
I_{OL}	Low-level output current	V_{DD} = 2.3 V,	V_O = 1.2 V	15			mA
		V_{DD} = 2.5 V,	V_O = 1.25 V		25		
		V_{DD} = 2.7 V,	V_O = 0.3 V			10	

(1) All typical values are at respective nominal V_{DD}.
(2) For I_{CC} over frequency, see Figure 6.

TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating junction temperature

			MIN	NOM	MAX	UNIT
f_{clk}	Clock frequency	V_{DD} = 3 V to 3.6 V	0		200	MHz
		V_{DD} = 2.3 V to 2.7 V	0		170	

JITTER CHARACTERISTICS

Characterized using CDCVF2310 Performance EVM when V_{DD}=3.3 V. Outputs not under test are terminated to 50 Ω.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{jitter}	Additive phase jitter from input to output 1Y0	12 kHz to 5 MHz, f_{out} = 30.72 MHz		52		fs rms
		12 kHz to 20 MHz, f_{out} = 125 MHz		45		

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD} = 3.3 V ±0.3 V (see Figure 2)						
t_{PLH} / t_{PHL}	CLK to Yn	f = 0 MHz to 200 MHz For circuit load, see Figure 2.	1.3		3.3	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)				100	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				570	ps
$t_{sk(pp)}$	Part-to-part skew				500	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 2 V	0.7		2.2	V/ns
t_f	Fall time (see Figure 3)	V_O = 2 V to 0.4 V	0.7		2.2	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns
V_{DD} = 2.5 V ±0.2 V (see Figure 2)						
t_{PLH} / t_{PHL}	CLK to Yn	f = 0 MHz to 170 MHz For circuit load, see Figure 2.	1.5		4	ns
$t_{sk(o)}$	Output skew (Ym to Yn) (1) (see Figure 4)				170	ps
$t_{sk(p)}$	Pulse skew (see Figure 5)				680	ps
$t_{sk(pp)}$	Part-to-part skew				600	ps
t_r	Rise time (see Figure 3)	V_O = 0.4 V to 1.7 V	0.5		1.4	V/ns
t_f	Fall time (see Figure 3)	V_O = 1.7 V to 0.4 V	0.5		1.4	V/ns
$t_{su(en)}$	Enable setup time, G_high before CLK ↓		0.1			ns
$t_{su(dis)}$	Disable setup time, G_low before CLK ↓		0.1			ns
$t_{h(en)}$	Enable hold time, G_high after CLK ↓		0.4			ns
$t_{h(dis)}$	Disable hold time, G_low after CLK ↓		0.4			ns

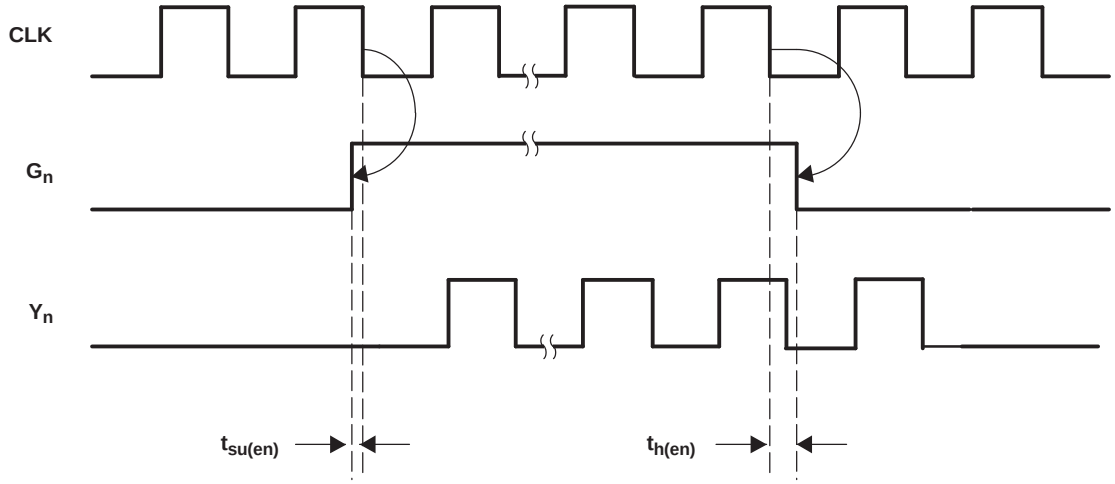
(1) The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

DETAILED DESCRIPTION

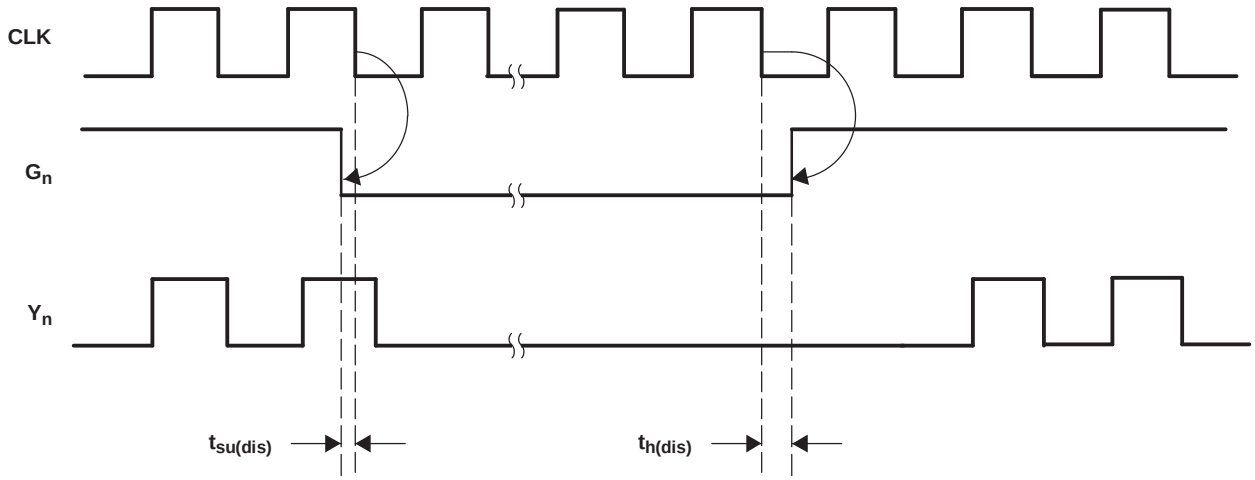
Output Enable Glitch Suppression Circuit

The purpose of the glitch suppression circuitry is to ensure the output enable sequence is synchronized with the clock input such that the output buffer is enabled or disabled on the next full period of the input clock (negative edge triggered by the input clock) (see Figure 1).

The G input must fulfill the timing requirements (t_{su}, t_h) according to the *Switching Characteristics* table for predictable operation.



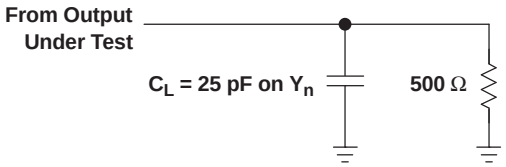
a) Enable Mode



b) Disable Mode

Figure 1. Enable and Disable Mode Relative to CLK↓

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 200 MHz, Z_O = 50 Ω, t_r < 1.2 ns, t_f < 1.2 ns.

Figure 2. Test Load Circuit

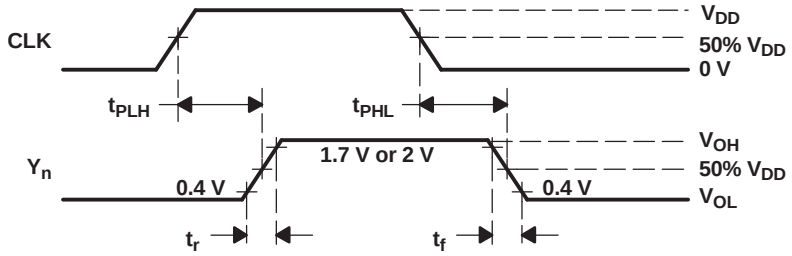


Figure 3. Voltage Waveforms Propagation Delay Times

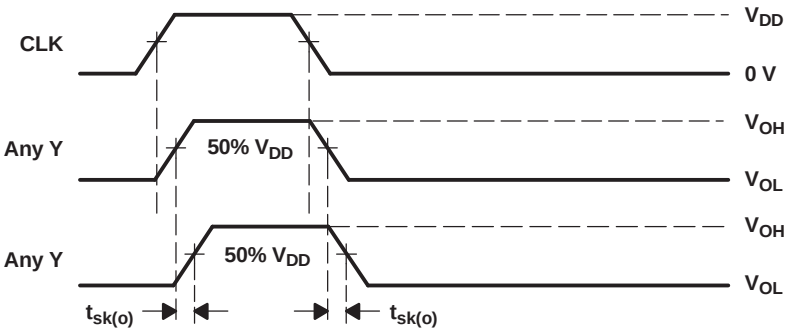
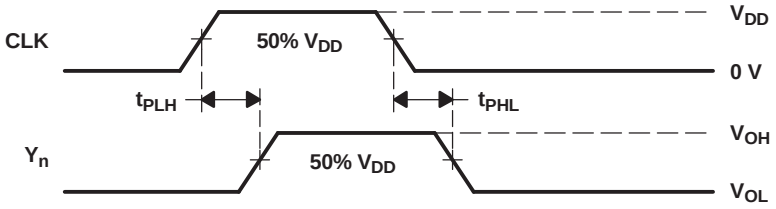


Figure 4. Output Skew



NOTE: $t_{sk(p)} = | t_{PLH} - t_{PHL} |$

Figure 5. Pulse Skew

PARAMETER MEASUREMENT INFORMATION (continued)

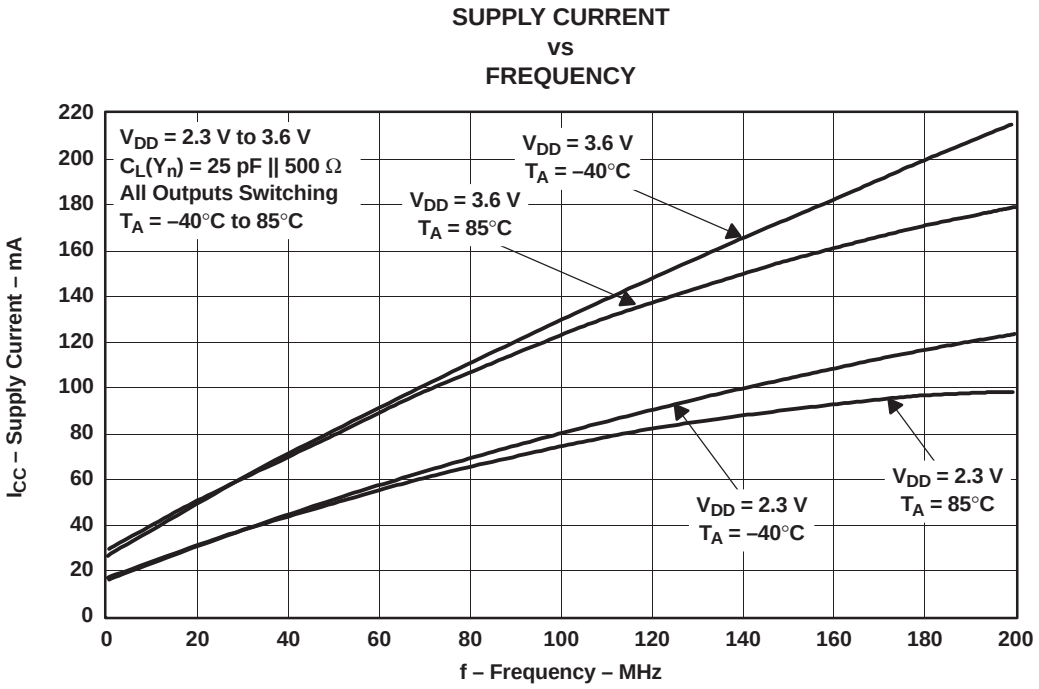


Figure 6.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCVF2310MPWEP	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP
CDCVF2310MPWREP	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP
V62/13603-01XE	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP
V62/13603-01XE-T	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CKV2310EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CDCVF2310-EP :

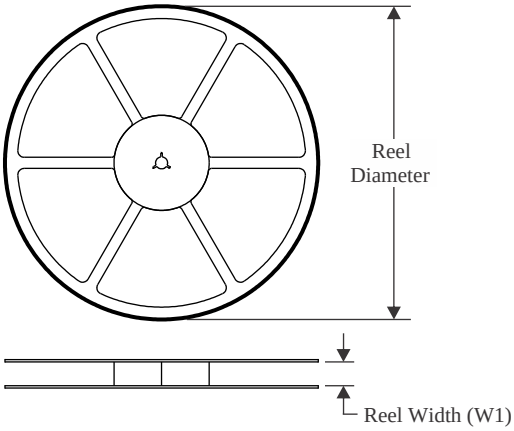
- Catalog : CDCVF2310

NOTE: Qualified Version Definitions:

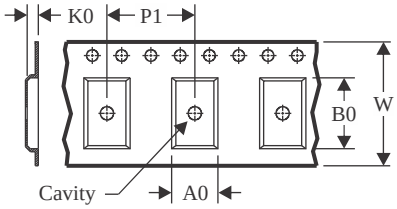
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

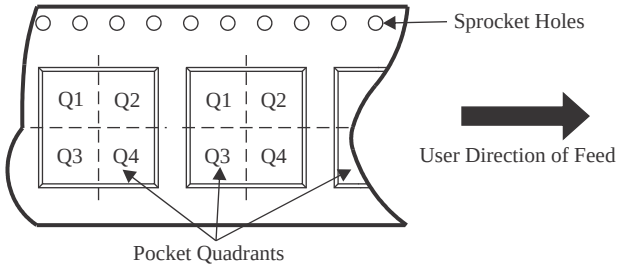


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

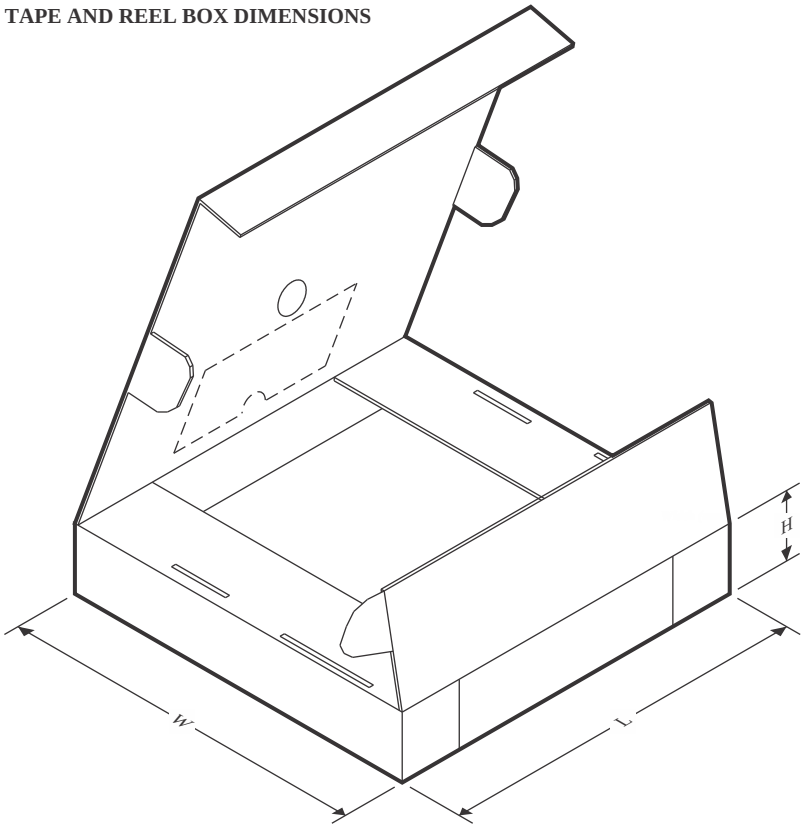
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF2310MPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

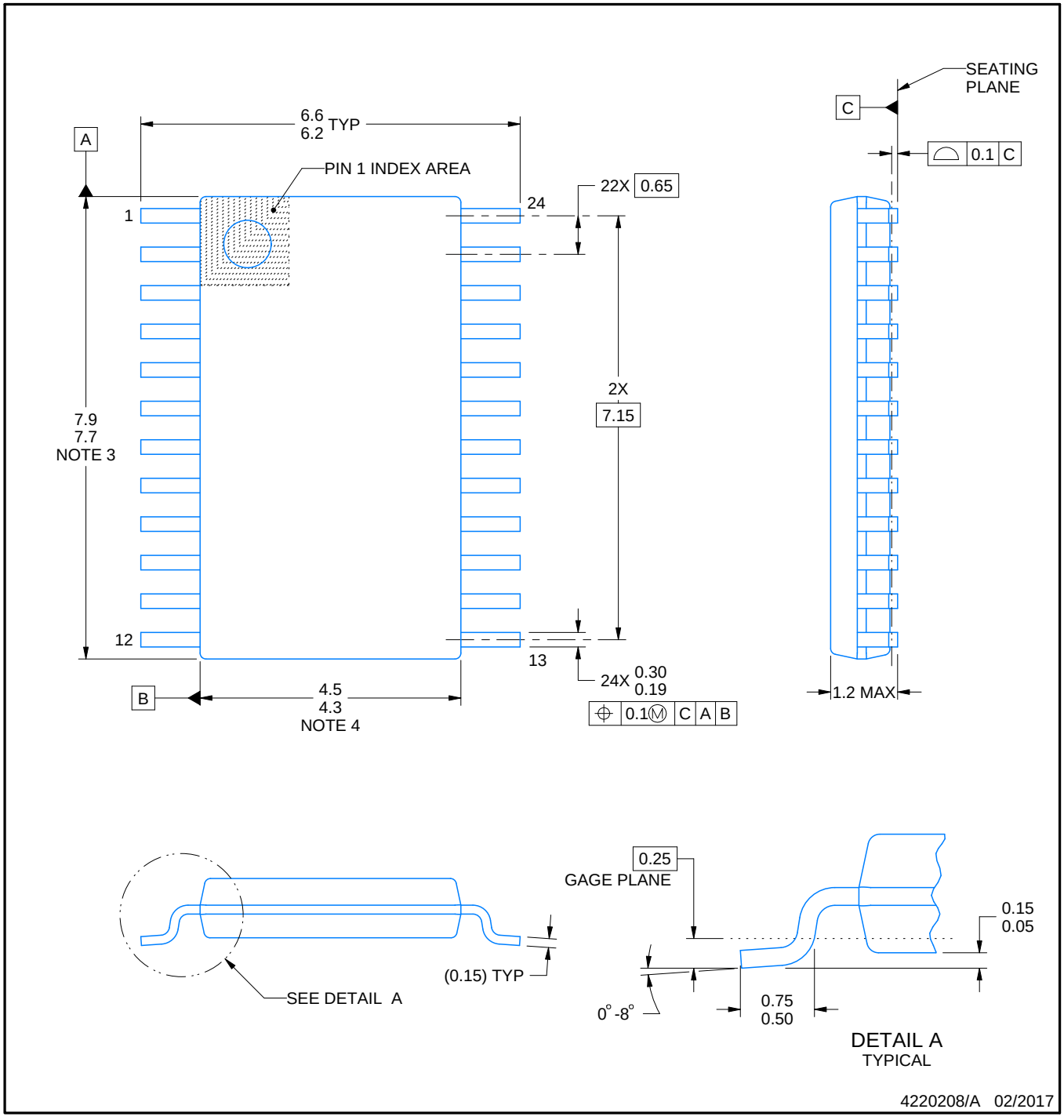
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF2310MPWREP	TSSOP	PW	24	2000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0024A

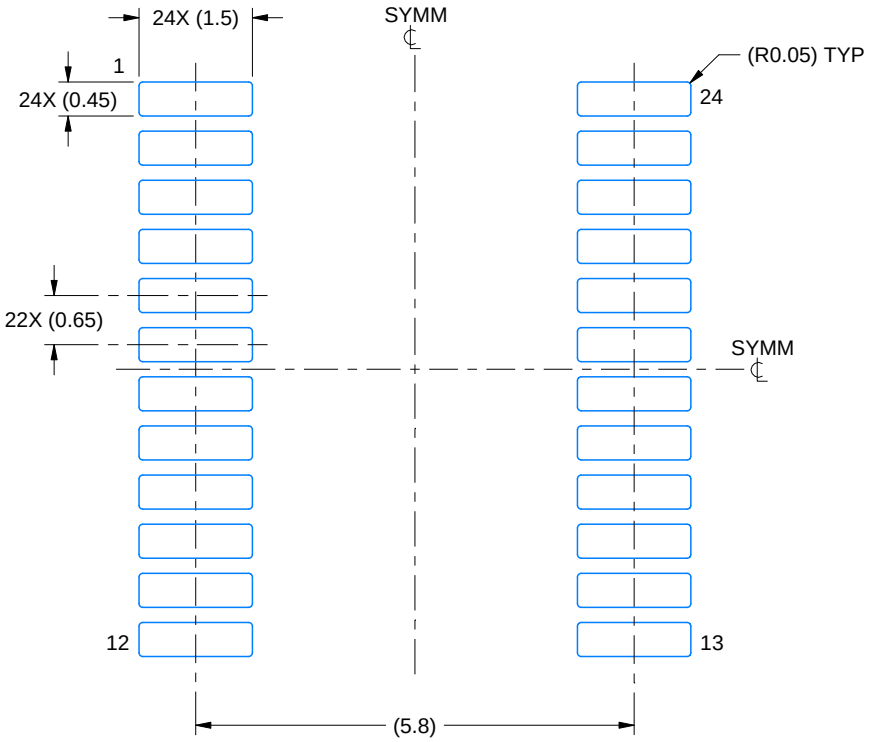
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

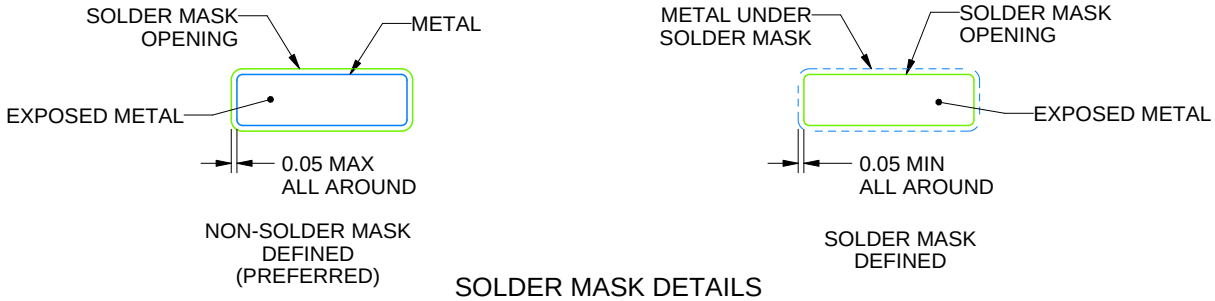


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

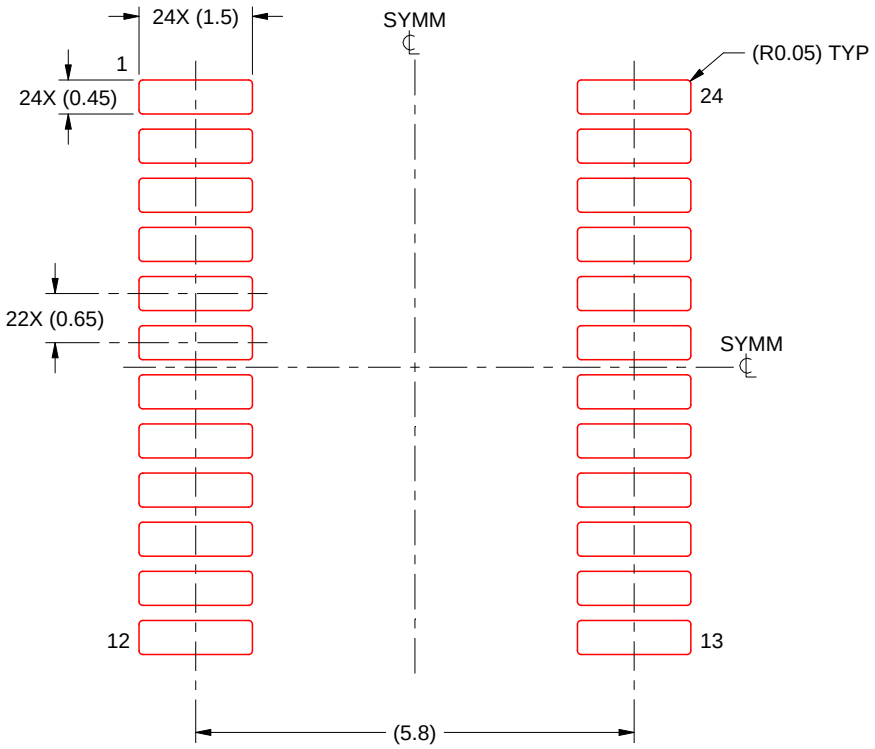


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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