CSD88539ND Dual 60 V N-Channel NexFET™ Power MOSFETs

1 Features

- Ultra-Low Q_g and Q_{gd}
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free

2 Applications

- Half Bridge for Motor Control
- Synchronous Buck Converter

3 Description

This dual SO-8, 60 V, 23 mΩ NexFET™ power MOSFET is designed to serve as a half bridge in low-current motor control applications.

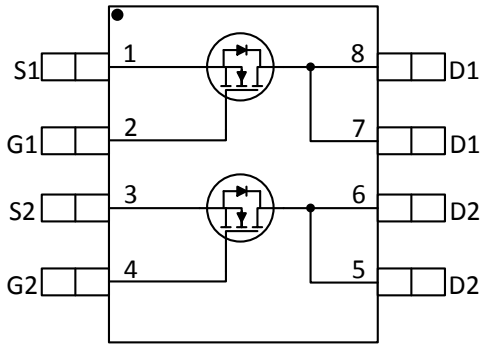


Figure 3-1. Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	60		V
Q_g	Gate Charge Total (10 V)	7.2		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V	27	mΩ
		V_{GS} = 10 V	23	mΩ
$V_{GS(th)}$	Threshold Voltage	3.0		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD88539ND	2500	13-Inch Reel	SO-8 Plastic Package	Tape and Reel
CSD88539NDT	250	7-Inch Reel		

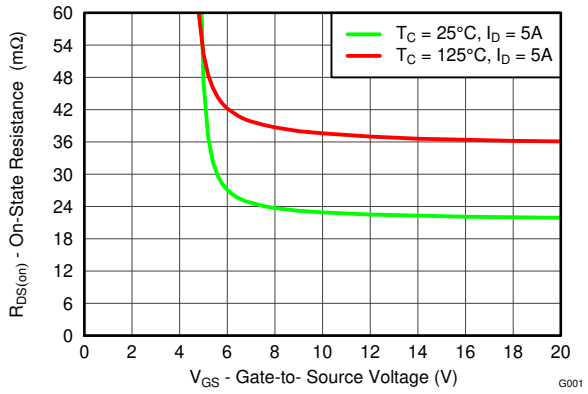
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

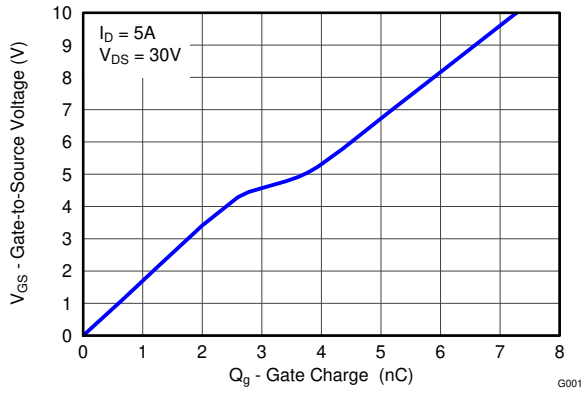
T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	60	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	15	A
	Continuous Drain Current (Silicon limited), T_C = 25°C	11.7	
	Continuous Drain Current(1)	6.3	
I_{DM}	Pulsed Drain Current (2)	46	A
P_D	Power Dissipation(1)	2.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 22 A, L = 0.1 mH, R_G = 25 Ω	24	mJ

(1) Typical $R_{\theta JA}$ = 60°C/W on a 1-inch², 2-oz. Cu pad on a 0.06-inch thick FR4 PCB

(2) Pulse duration ≤300 µs, duty cycle ≤2%



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.6	3.0	3.6	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6 V, I_D = 5 A		27	34	mΩ
		V_{GS} = 10 V, I_D = 5 A		23	28	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 5 A		19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		570	741	pF
C_{oss}	Output Capacitance			70	91	pF
C_{rss}	Reverse Transfer Capacitance			2.0	2.6	pF
R_G	Series Gate Resistance			6.6	13.2	Ω
Q_g	Gate Charge Total (10 V)	V_{DS} = 30 V, I_D = 5 A		7.2	9.4	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.7		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	V_{DS} = 30 V, V_{GS} = 0 V		9.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 5 A, R_G = 0 Ω		5		ns
t_r	Rise Time			9		ns
$t_{d(off)}$	Turn Off Delay Time			14		ns
t_f	Fall Time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	I_{SD} = 5 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DS}= 30 V, I_F = 5A, di/dt = 300A/µs		37		nC
t_{rr}	Reverse Recovery Time			21		ns

4.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JL}$	Junction-to-Lead Thermal Resistance(1)			20	°C/W
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance(1) (2)			75	

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

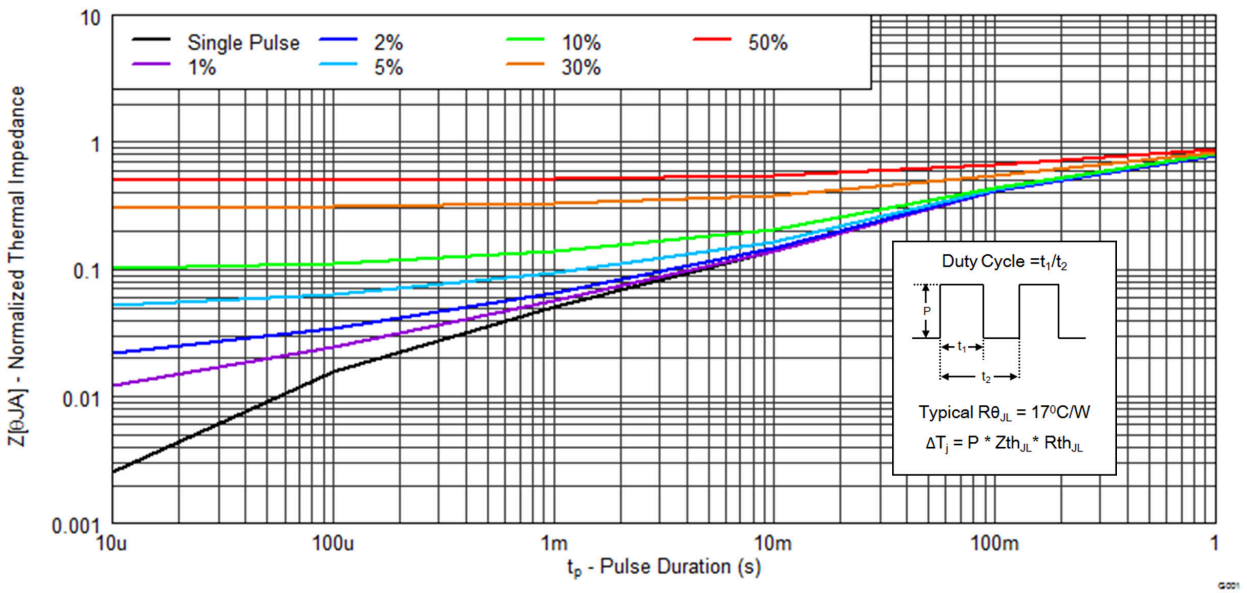


Figure 4-1. Transient Thermal Impedance

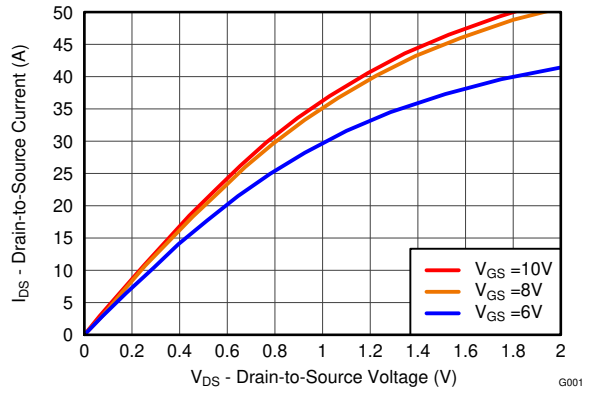


Figure 4-2. Saturation Characteristics

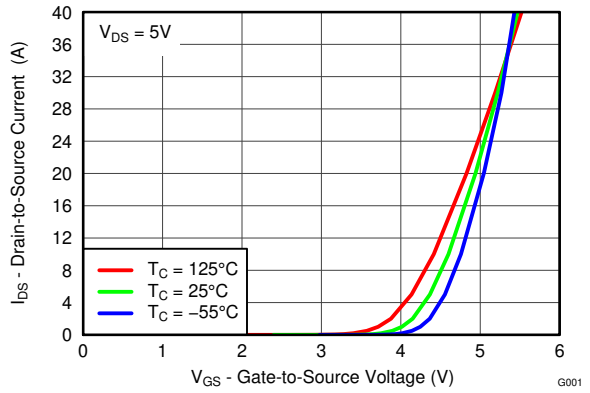


Figure 4-3. Transfer Characteristics

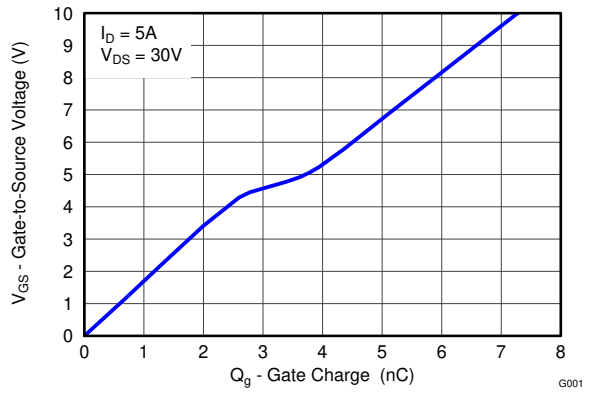


Figure 4-4. Gate Charge

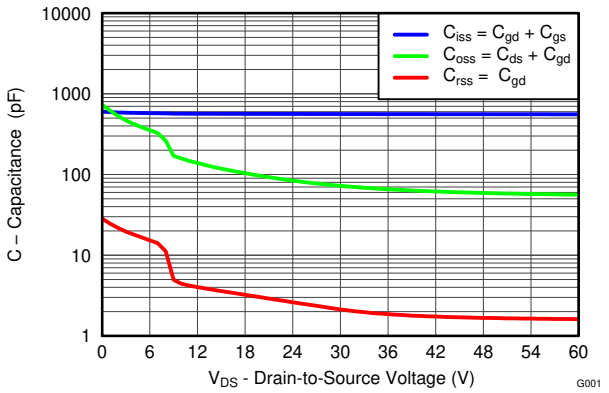


Figure 4-5. Capacitance

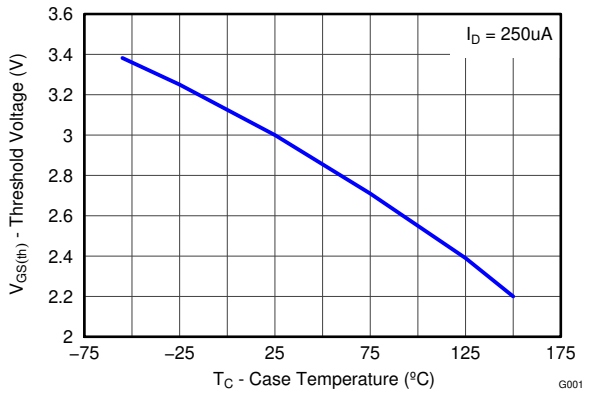


Figure 4-6. Threshold Voltage vs Temperature

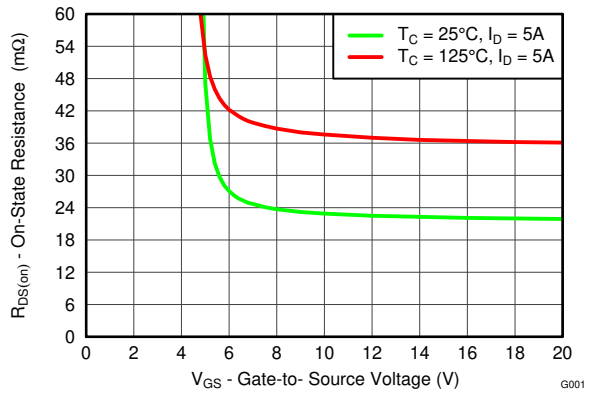


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

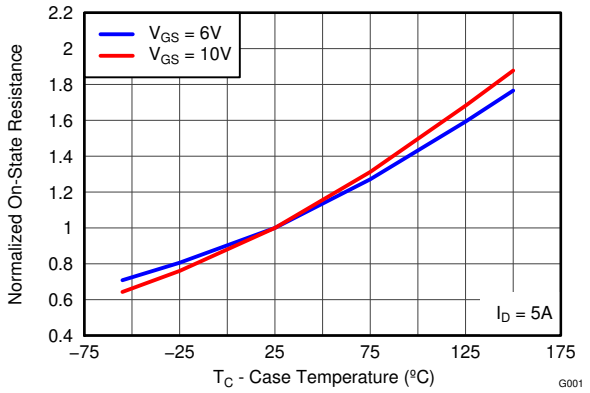


Figure 4-8. Normalized On-State Resistance vs Temperature

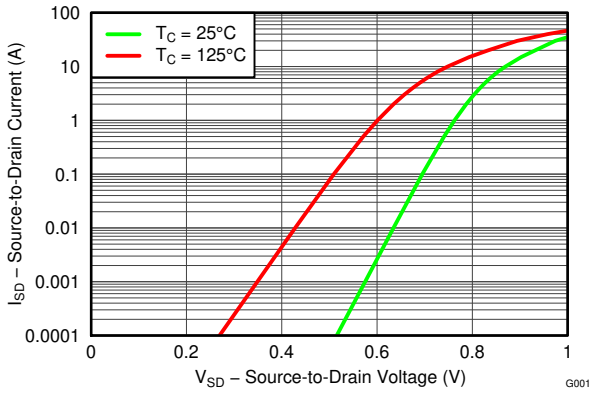


Figure 4-9. Typical Diode Forward Voltage

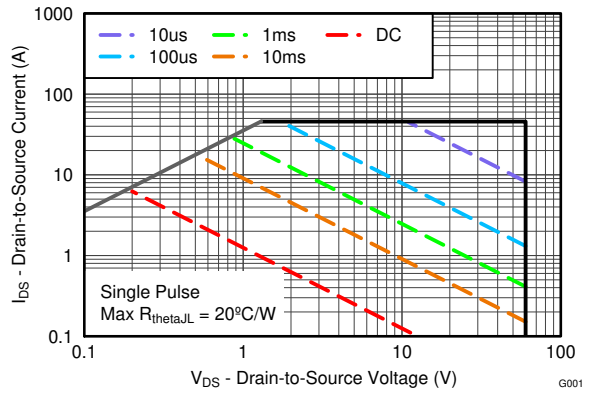


Figure 4-10. Maximum Safe Operating Area

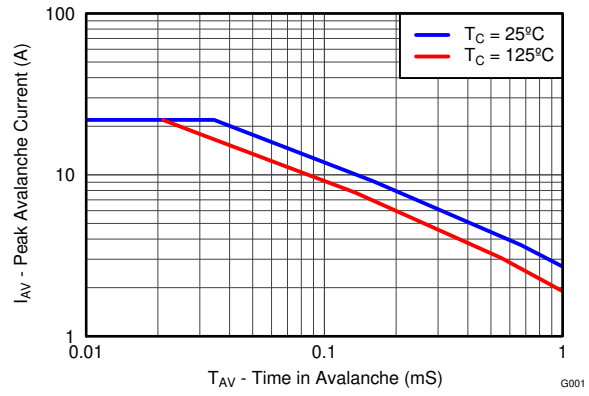


Figure 4-11. Single Pulse Unclamped Inductive Switching

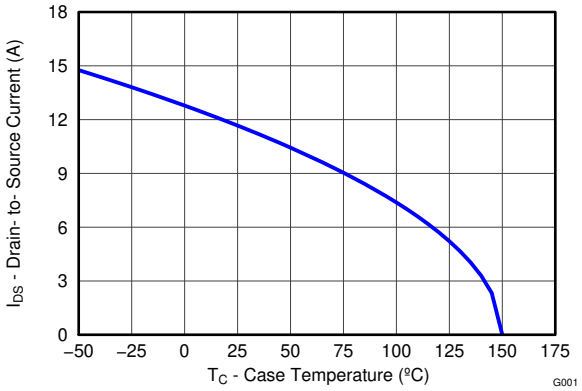


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Trademarks

NexFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5.2 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2014) to Revision A (December 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

7 Mechanical Data

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD88539ND	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N
CSD88539ND.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-55 to 150	
CSD88539NDG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N
CSD88539NDG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N
CSD88539NDT	Active	Production	SOIC (D) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 150	88539N
CSD88539NDT.B	Active	Production	SOIC (D) | 8	250 | SMALL T&R	-	Call TI	Call TI	-55 to 150	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

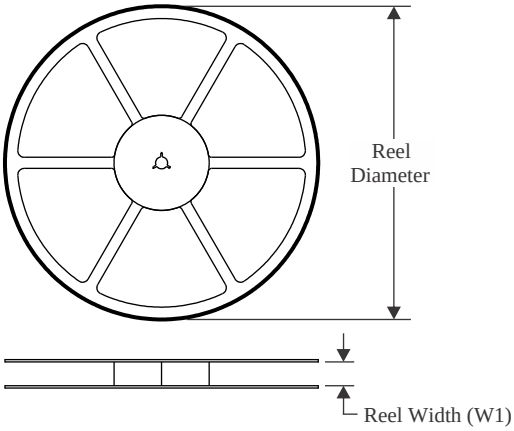
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

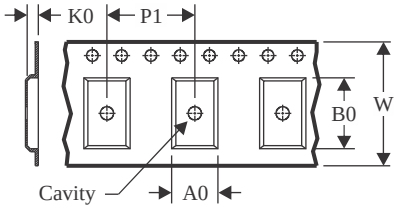
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

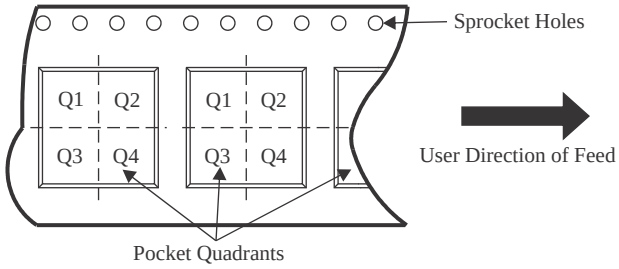


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

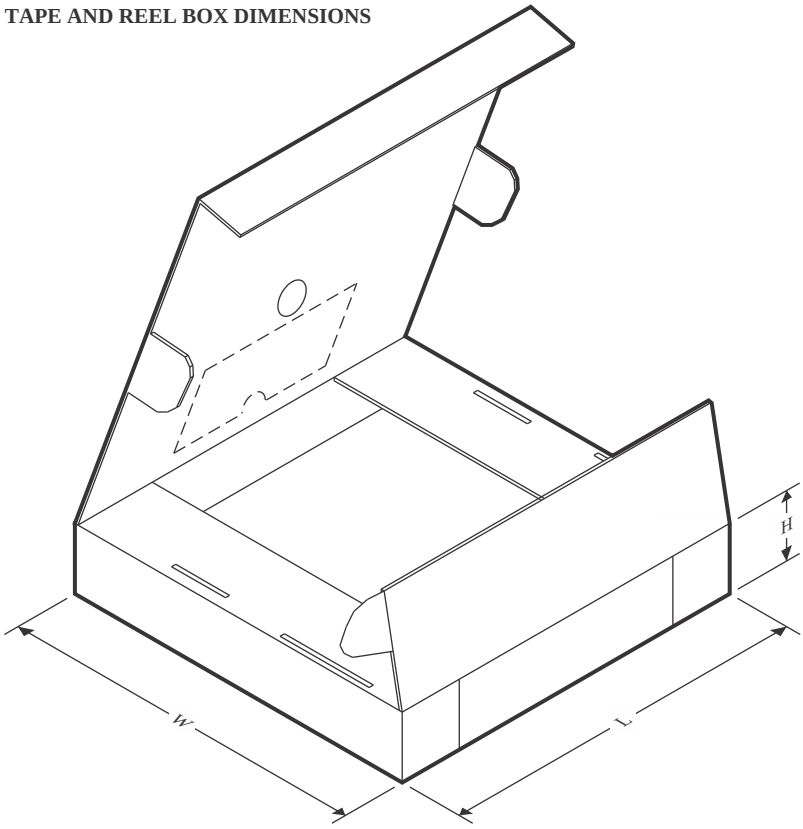
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

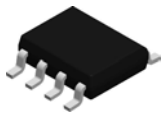
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD88539NDT	SOIC	D	8	250	178.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD88539NDT	SOIC	D	8	250	180.0	180.0	79.0

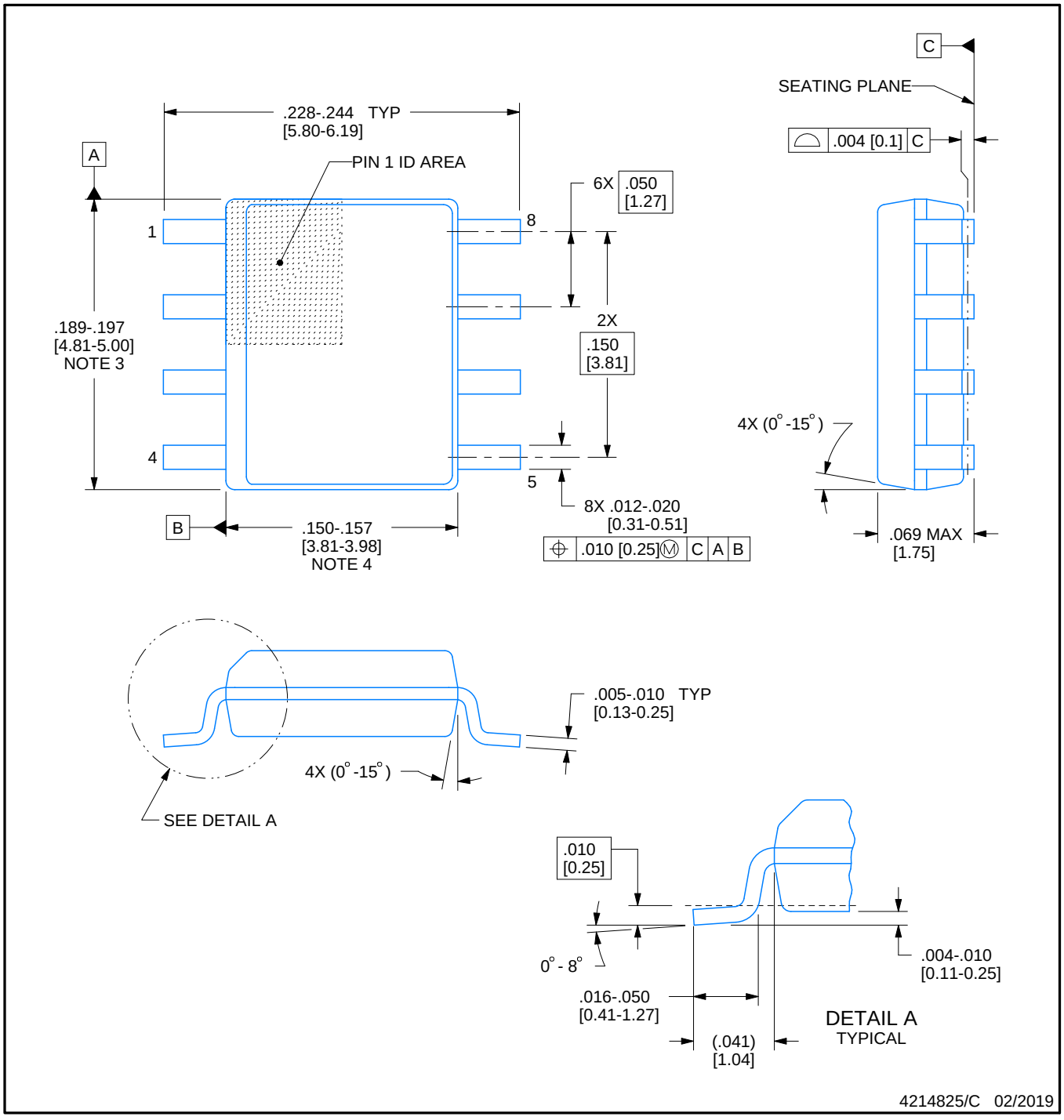


PACKAGE OUTLINE

D0008A

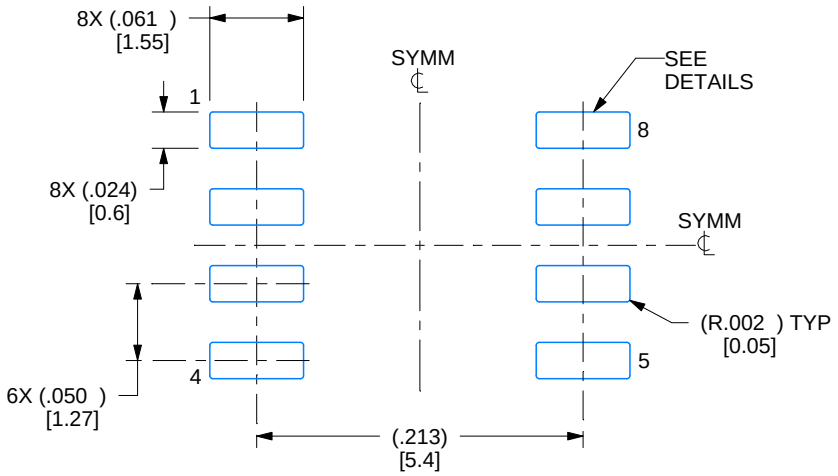
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

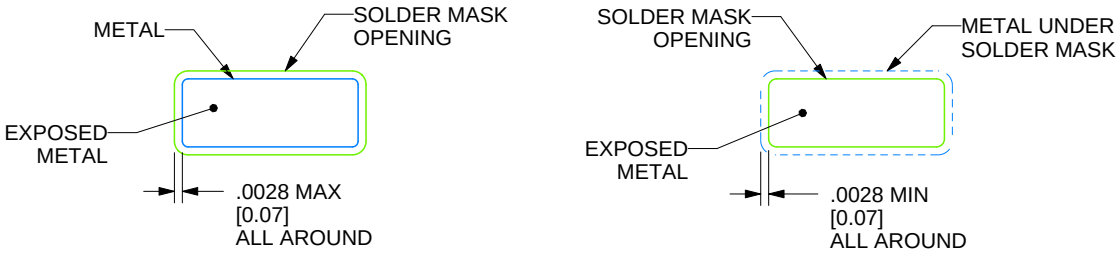


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

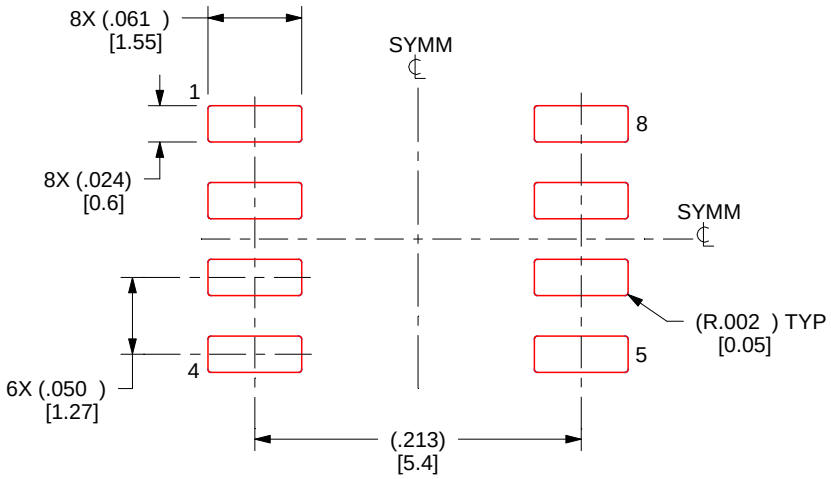
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025