DS80EP100 5 to 12.5 Gbps, Power-Saver Equalizer for Backplanes and Cables

Check for Samples: DS80EP100

FEATURES

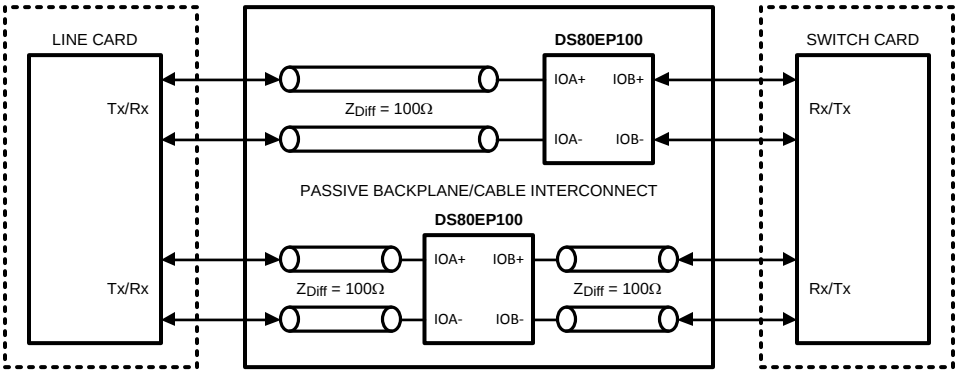
- **5 to 12.5 Gbps Operation**
- **No Power or Ground Required**
- **Equalization Effective Anywhere in Data Path**
- **Equalizes CML, LV-PECL, LVDS Signals**
- **Symmetric I/O Structures Provide Equal Boost for Bi-directional Operation**
- **7 dB Maximum Boost**
- **Code Independent, 8b/10b or Scrambled**
- **Supports Both Bi-level and Multi-level Signaling**
- **Extends Reach Over Backplanes and Cables**
- **Compatible with PCI-Express Gen1 and Gen2**
- **Compatible with XAUI**
- **Will Operate in Series with Existing Active Equalizer**
- **Easy to Handle 6 Pin WSON**

DESCRIPTION

TI's Power-saver equalizer compensates for transmission medium losses and minimizes medium-induced deterministic jitter. Performance is guaranteed over the full range of 5 to 12.5 Gbps. The DS80EP100 requires no power to operate. The equalizer operates anywhere in the data path to minimize media-induced deterministic jitter in both FR4 traces and cable applications. Symmetric I/O structures support full duplex or half duplex applications. Linear compensation is provided independent of line coding or protocol. The device is ideal for both bi-level and multi-level signaling.

The equalizer is available in a 6 pin leadless WSON package with a space saving 2.2 mm X 2.5 mm footprint. This tiny package provides maximum flexibility in placement and routing of the Power-saver equalizer.

Simplified Application Diagram



Note: The DS80EP100 provides the flexibility of passing the data from either side of the device. It can be placed anywhere in the data path.

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O Type(1)	Description
High speed differential I/O			
IOA- IOA+	3 1	I/O	Symmetric differential I/O
IOB- IOB+	4 6	I/O	Symmetric differential I/O
NC Exposed Pad	2, 5 DAP	N/A	Reserved. Do not connect.

(1) I = Input / O = Output

Connection Diagram

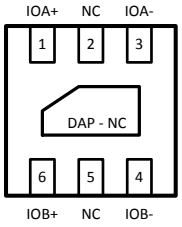


Figure 1. Bottom View
2.2mm x 2.5mm 6-Pin WSON Package
See Package Number NHK0014A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

INPUT/OUTPUT	(IOA+ and IOB+) or (IOA- and IOB-)	+2V
	(IOA+ and IOA-) or (IOB+ and IOB-)	+4V
	(IOA+ and IOB-) or (IOA- and IOB+)	+4V
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature Soldering, 4 sec		+260°C
ESD Rating	HBM, 1.5 kΩ, 100 pF	1.3kV

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Typ	Max	Units
Ambient Temperature	−40	25	+85	°C
Bit Rate	5		12.5	Gbps

Electrical Characteristics (1)

Over recommended operating conditions unless other specified. All parameters are guaranteed by test, statistical analysis or design.

Symbol	Parameter	Conditions	Min	Typ (2)	Max	Units
V_{IN}	Input voltage swing	See (3)		1000	3600	mVp-p
	Equalization	6.25 GHz relative to 100MHz		6		dB
R_{LI}	Differential input return loss	100 MHz – 6.25 GHz, with fixture's effect de-embedded		15		dB
R_{LO}	Differential output return loss	100 MHz – 6.25 GHz, with fixture's effect de-embedded IOA+, or IOB+ = static high.		15		dB
R_{IN}	Input Impedance	Differential across IOA+ and IOA-, or IOB+ and IOB-, ZLOAD = 100Ω		100		Ω
R_O	Output Impedance	Differential across IOA+ and IOA-, or IOB+ and IOB-, ZSOURCE = 100Ω		100		Ω
	Through Response	Relative to ideal load, see Figure 3 for setup	See Figure 4 and Table 1 for limits			
R1	Resistance IOA+ to IOA- and IOB+ to IOB-	No load, high impedance on all ports		150		Ω
R2	Resistance IOA+ to IOB+ and IOA- to IOB-	No load, high impedance on all ports		50		Ω
R3	Resistance IOA+ to IOB- and IOA- to IOB+	No load, high impedance on all ports		150		Ω
	DC Gain (IOA/IOB or IOB/IOA)	ZLOAD = 100Ω		0.4		
DJ1	Residual deterministic jitter	5 Gbps, 20 in of 6mil microstrip FR4 See (4)		0.15		UIp-p
DJ2	Residual deterministic jitter	6.25 Gbps, 20 in of 6mil microstrip FR4 See (4) (5)		0.15	0.20	UIp-p
DJ3	Residual deterministic jitter	8 Gbps, 20 in of 6mil microstrip FR4 See (4) (5)		0.15	0.20	UIp-p
DJ4	Residual deterministic jitter	10 Gbps, 20 in of 6mil microstrip FR4 See (4)		0.15		UIp-p
DJ5	Residual deterministic jitter	12.5 Gbps, 14 in of 6mil microstrip FR4 See (4)		0.15		UIp-p

(1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
(2) Typical values represent most likely parametric norms, TA = +25 degC, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
(3) Differential signal to Equalizer, measured at the input to a transmission line, see point A of Figure 2. The transmission line is Z_0 = 100Ω, 6-mil, microstrip in FR4 material.
(4) Deterministic jitter is measured at the differential outputs (point C of Figure 2), minus the deterministic jitter before the test channel (point A of Figure 2). Test pattern: PRBS- 7 .
(5) Specification is guaranteed by characterization and is not tested in production.

TEST SETUP DIAGRAMS

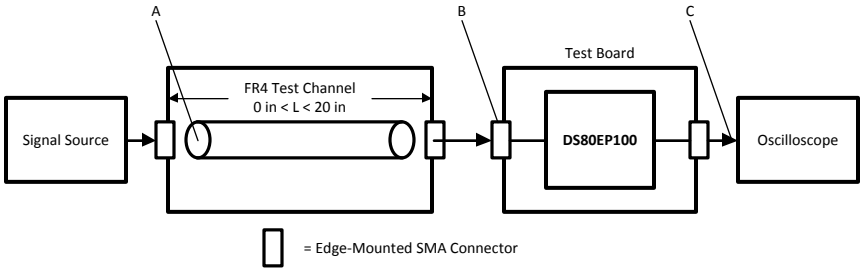


Figure 2. Transient Test Setup Diagram

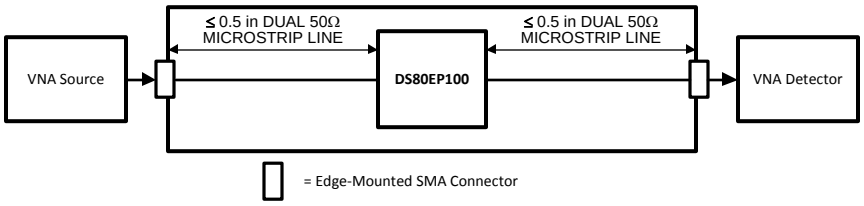


Figure 3. Frequency Response Test Circuit

Typical Equalizer Transfer Function

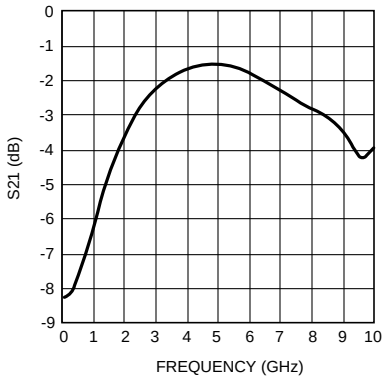


Figure 4. Typical Equalizer Transfer Function

Table 1. Typical Through Response

Frequency (GHz)	DS80EP100 Attenuation Typ (dB)
0.1	-8.25
0.5	-7.64
1	-6.12
1.5	-4.68
2	-3.57
3	-2.22
4	-1.66
5	-1.53
6	-1.77
7	-2.28
8	-2.8
9	-3.47
10	-3.91

Block Diagram

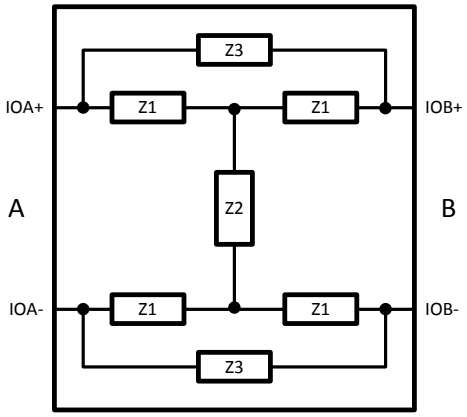


Figure 5. Simplified Block Diagram

APPLICATION INFORMATION

DS80EP100 DEVICE DESCRIPTION

The DS80EP100 Power-Saver equalizer is a passive network circuit composed of resistive, capacitive, and inductive components (See Figure 5). A Differential bridged T-network compensates for the transmission medium losses and minimizes medium-induced deterministic jitter with FR4 and cables. The equalizer attenuates low frequency signals and is a bandpass filter at the resonant frequency. The response is linear and symmetric.

I/O TERMINATIONS

The DS80EP100 I/O impedance is 100Ω differential. The equalizer is designed for 100Ω-balanced differential signals and is not intended for single-ended transmission.

LINEAR COMPENSATION

The unique linear compensation feature of the DS80EP100 combined with the tiny package allows maximum flexibility in placement. The equalizer can be placed anywhere in the data path and will provide the same compensation at the receiving circuit. (See Simplified Application Diagram)

SYMMETRIC I/O STRUCTURES

The symmetry of the passive equalization network allows bi-directional operation. Signals receive equal compensation regardless of the direction of data flow. (See Figure 5).

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS AND NO CONNECT PADS

The differential I/Os must have a controlled differential impedance of 100Ω. It is preferable to route all differential lines exclusively on one layer of the board. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Differential signals should be routed away from other signals and noise sources on the printed circuit board. Pin 2, Pin 5, and the center DAP have to be left as no connect. Therefore, do not connect the landing pads of these pins to the power or ground plane. See AN-1187 for additional information on the WSON package.

Typical Characteristics

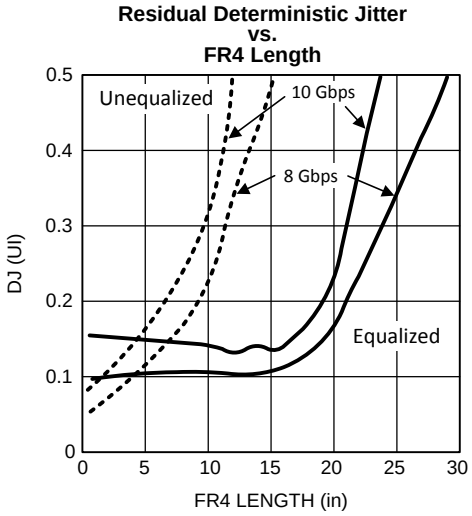


Figure 6.

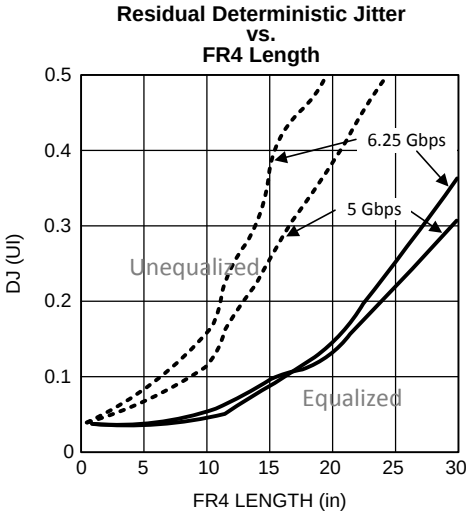


Figure 7.

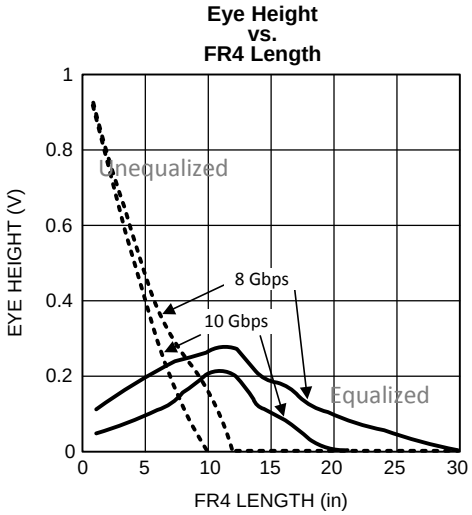


Figure 8.

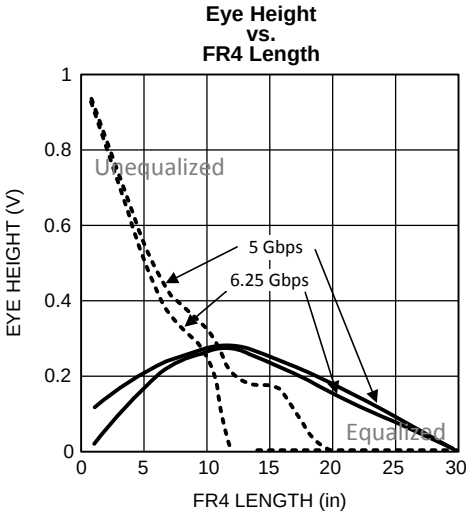


Figure 9.

Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter

Unequalized Signal (20in FR4, 5Gbps, PRBS7)

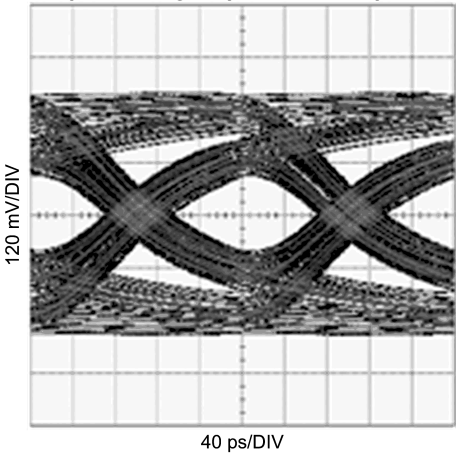


Figure 10.

Equalized Signal (20in FR4, 5Gbps, PRBS7)

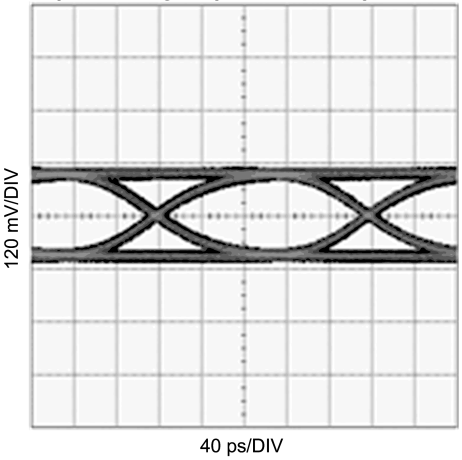


Figure 11.

Equalized Signal (Zoom) (20in FR4, 5Gbps, PRBS7)

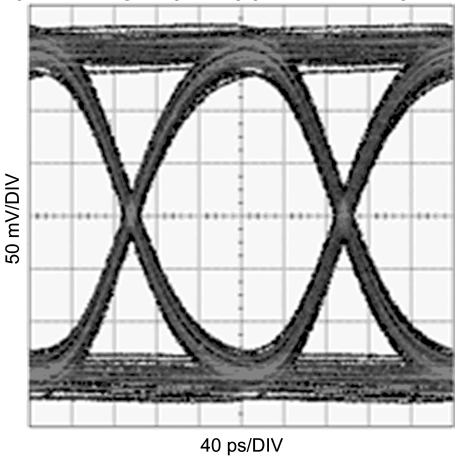


Figure 12.

Unequalized Signal (20in FR4, 6.25Gbps, PRBS7)

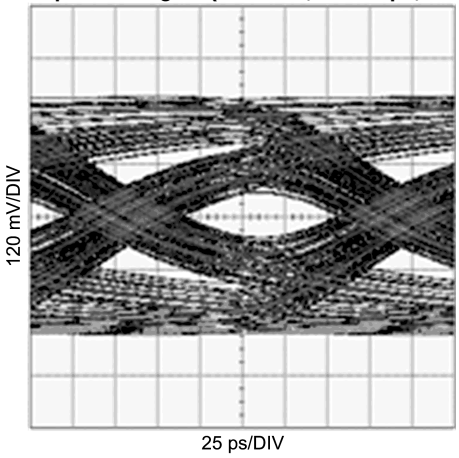


Figure 13.

Equalized Signal (20in FR4, 6.25Gbps, PRBS7)

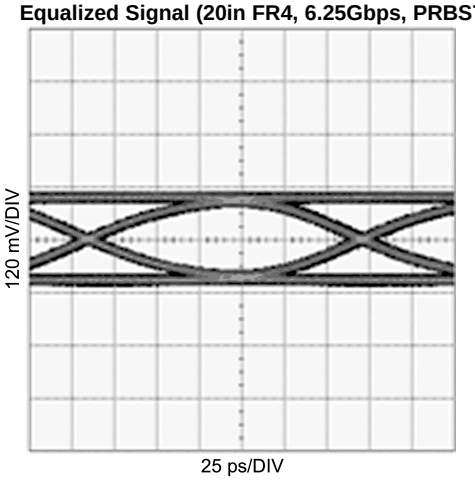


Figure 14.

Equalized Signal (Zoom) (20in FR4, 6.26Gbps, PRBS7)

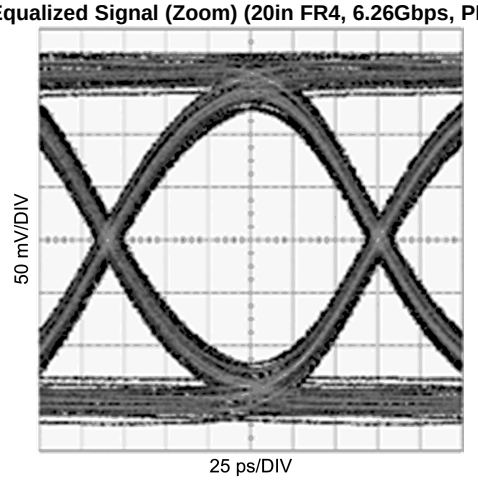


Figure 15.

Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (20in FR4, 8Gbps, PRBS7)

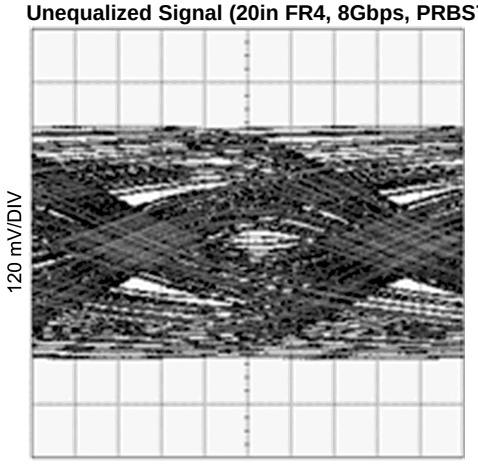


Figure 16.

Equalized Signal (20in FR4, 8Gbps, PRBS7)

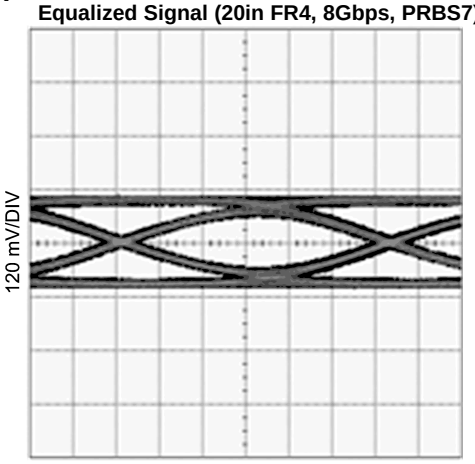


Figure 17.

Equalized Signal (Zoom) (20in FR4, 8Gbps, PRBS7)

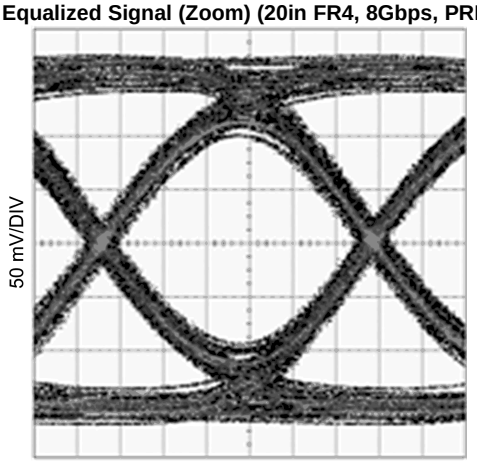


Figure 18.

Unequalized Signal (20in FR4, 10Gbps, PRBS7)

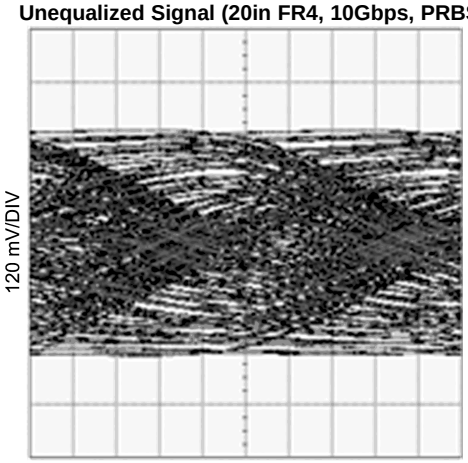


Figure 19.

Equalized Signal (20in FR4, 10Gbps, PRBS7)

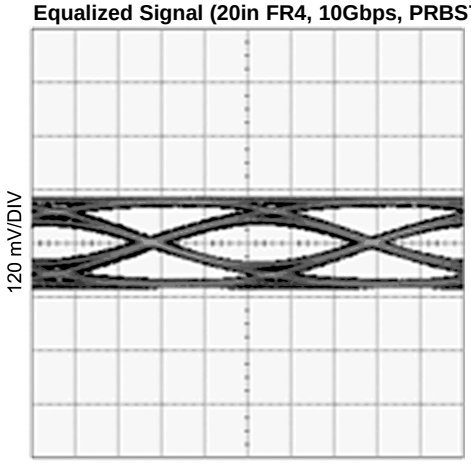


Figure 20.

Equalized Signal (Zoom) (20in FR4, 10Gbps, PRBS7)

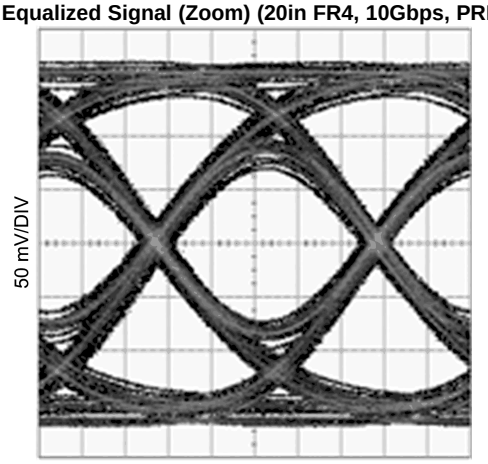


Figure 21.

Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (14in FR4, 12.5Gbps, PRBS7)

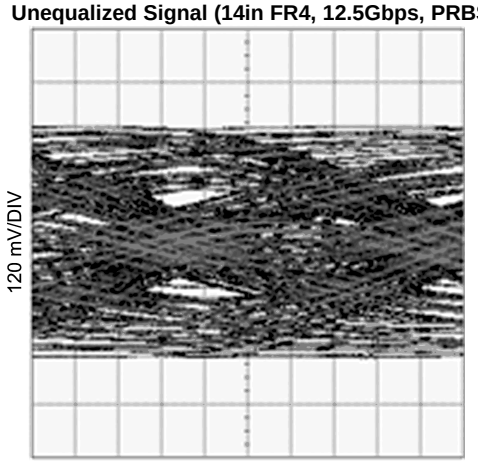


Figure 22.

Equalized Signal (14in FR4, 12.5Gbps, PRBS7)

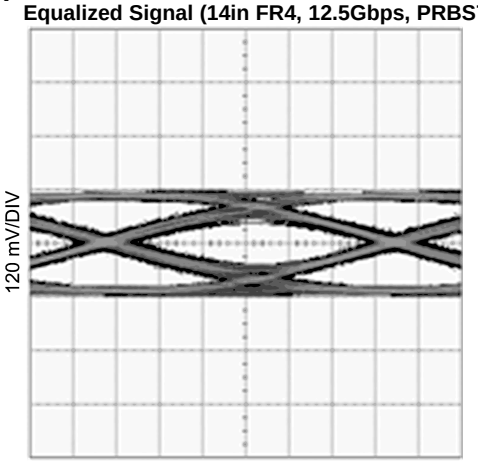


Figure 23.

Equalized Signal (Zoom) (14in FR4, 12.5Gbps, PRBS7)

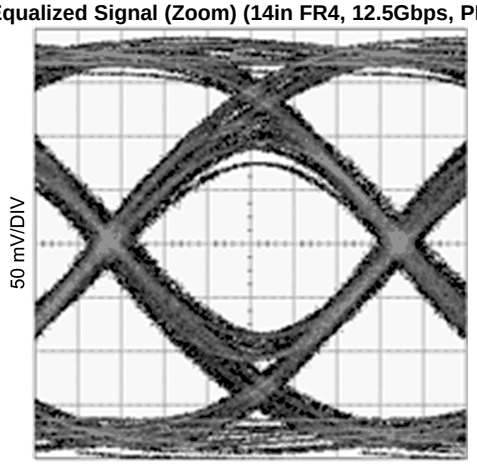


Figure 24.

Unequalized Signal (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)

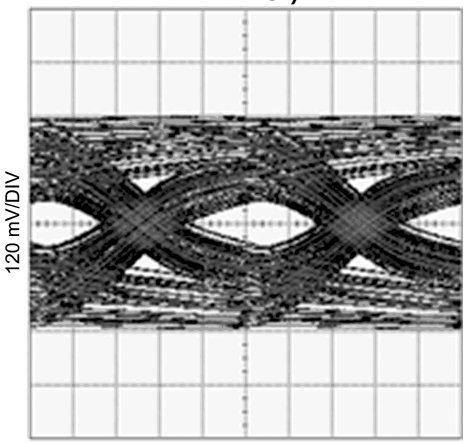


Figure 25.

Equalized Signal (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)

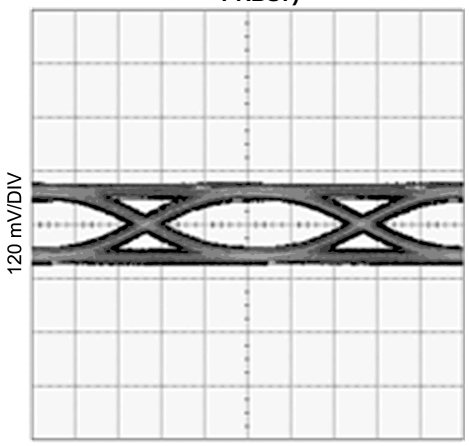


Figure 26.

Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 5Gbps, PRBS7)

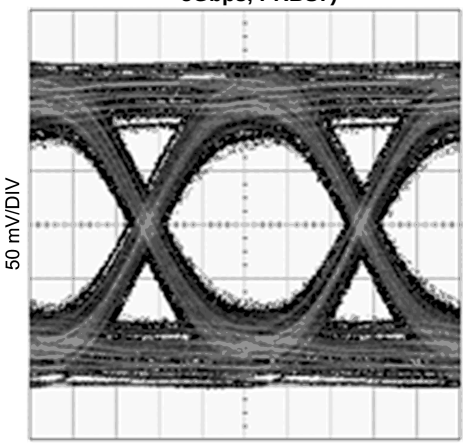


Figure 27.

Typical Eye Diagrams — Includes Transmitter Setup, Interconnect, and Device Total Jitter (continued)

Unequalized Signal (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)

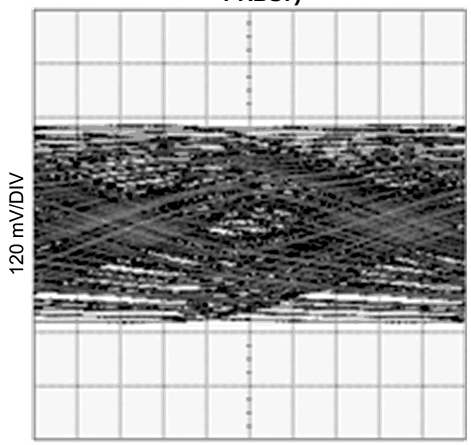


Figure 28.

Equalized Signal (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)

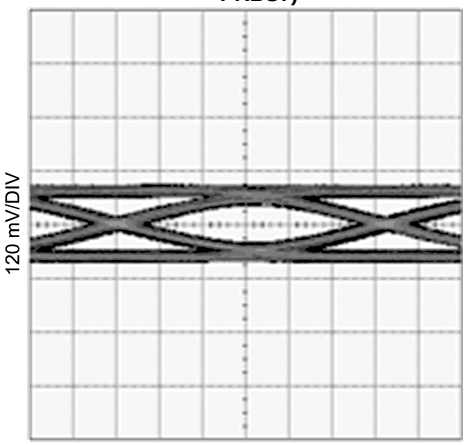


Figure 29.

Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 8Gbps, PRBS7)

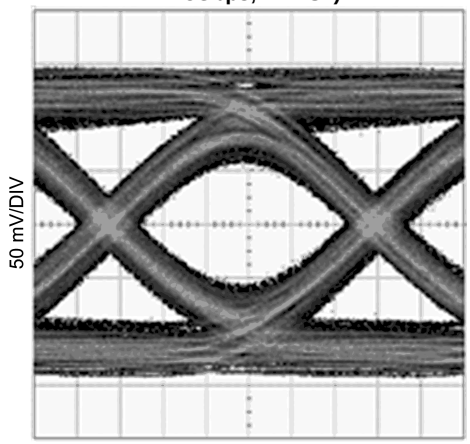


Figure 30.

Unequalized Signal (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)

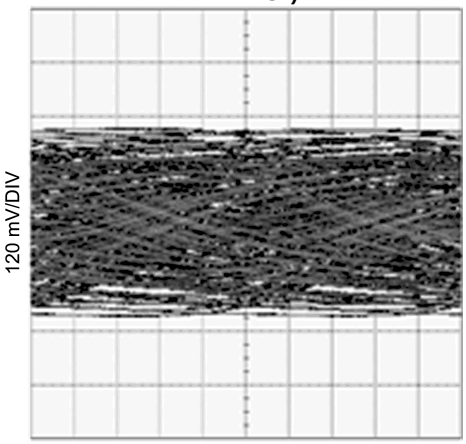


Figure 31.

Equalized Signal (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)

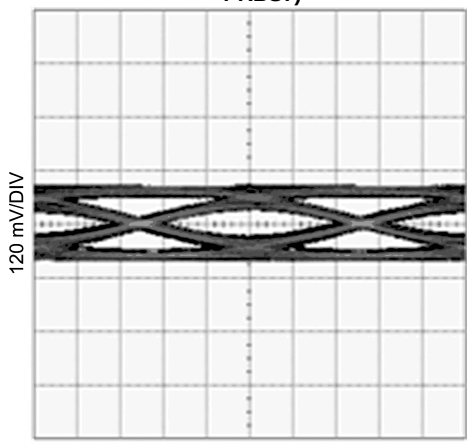


Figure 32.

Equalized Signal (Zoom) (5m 26AWG Twin-AX Cable, 10Gbps, PRBS7)

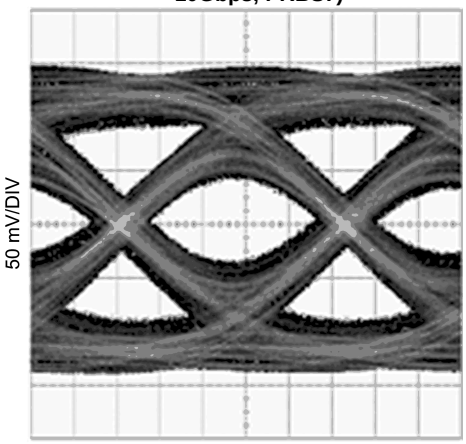


Figure 33.

REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS80EP100SD/NOPB	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	80S
DS80EP100SD/NOPB.A	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	80S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

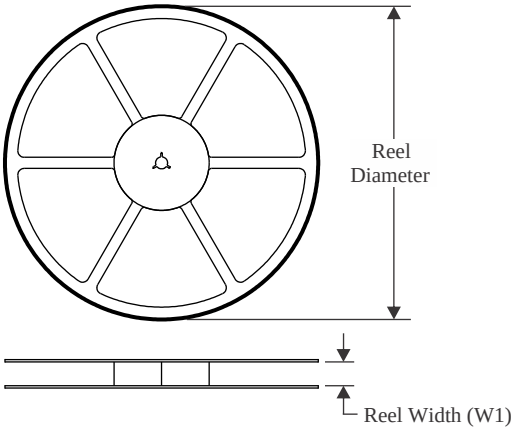
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

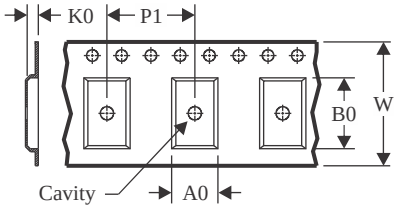
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

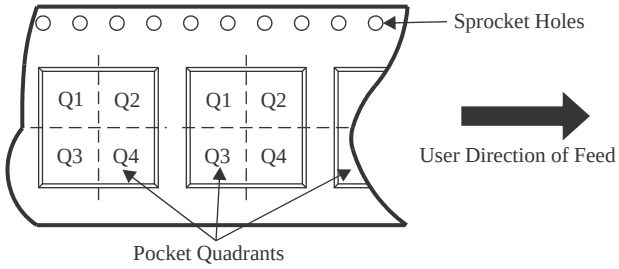


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

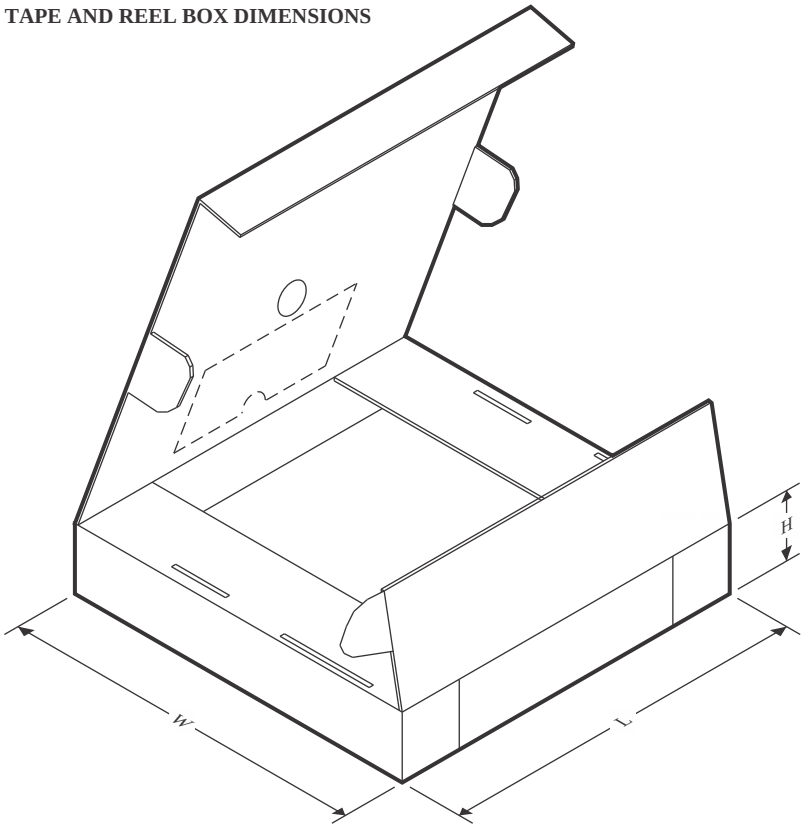
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS80EP100SD/NOPB	WSON	NGF	6	1000	177.8	12.4	2.8	2.5	1.0	8.0	12.0	Q1

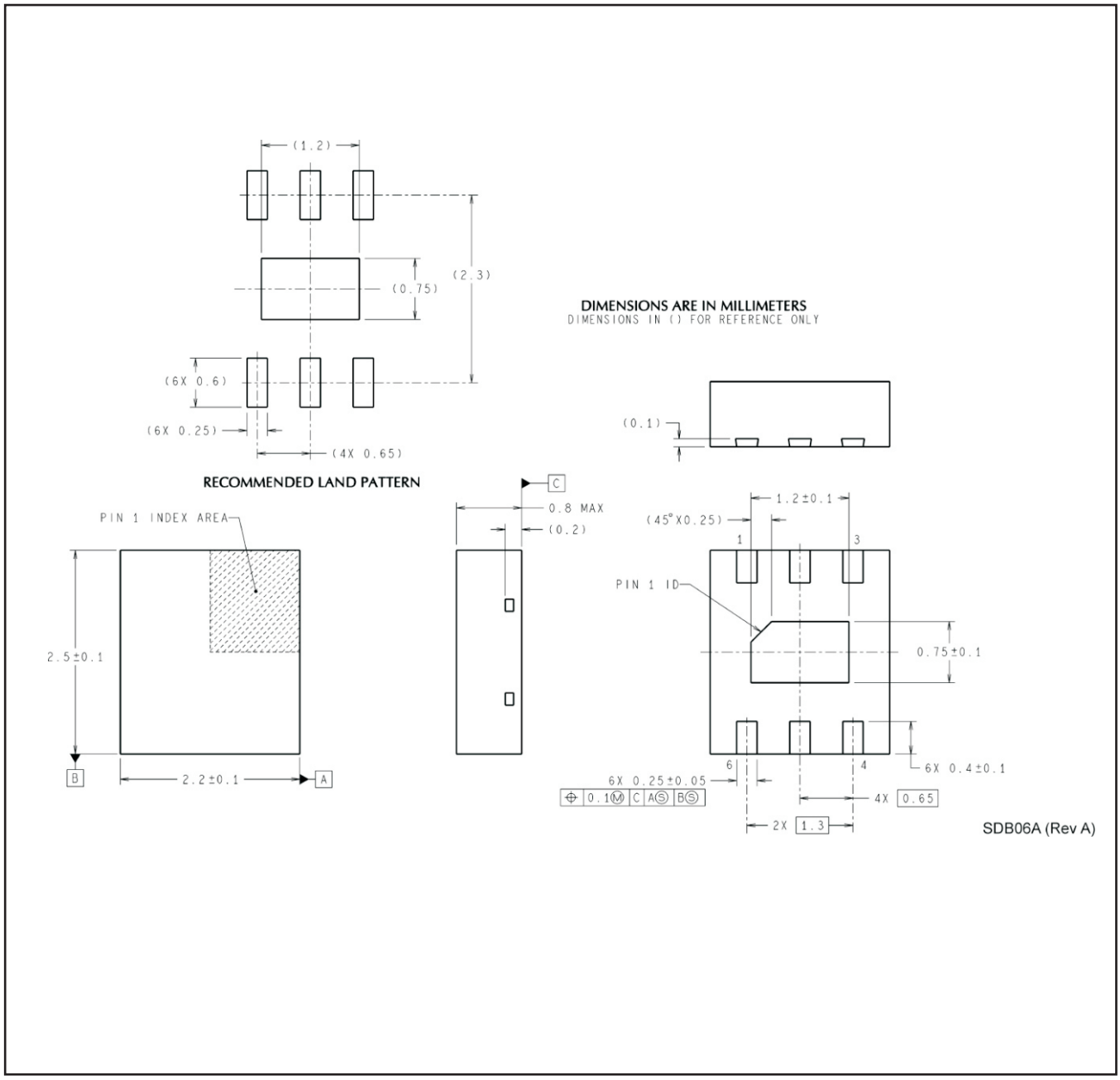
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS80EP100SD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0

NGF0006A


(1.2)
(2.3)
(0.75)
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
2.5±0.1
2.2±0.1
B
A
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
6X 0.4±0.1
6X 0.25±0.05
0.10 M C A S B S
4X 0.65
2X 1.3
SDB06A (Rev A)

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