DS90CR286A/-Q1 (or DS90CR216A) 3.3-V Rising Edge Data Strobe LVDS Receiver 28-Bit (or 21-Bit) Channel Link-66 MHz

1 Features

- 20 to 66 MHz Shift Clock Support
- 50% Duty Cycle on Receiver Output Clock
- Best–in–Class Set and Hold Times on Rx Outputs
- Rx Power Consumption < 270 mW (Typ) at 66 MHz Worst Case
- Rx Power-Down Mode < 200 μW (Max)
- ESD Rating > 7 kV (HBM), > 700 V (EIAJ)
- PLL Requires No External Components
- Compatible with TIA/EIA-644 LVDS Standard
- Low Profile 56-Pin or 48-Pin DGG (TSSOP) Package
- Operating Temperature: −40°C to 85°C
- Automotive Q Grade Available - AEC-Q100 Grade 3 Qualified

2 Applications

- Video Displays
- Automotive Infotainment
- Industrial Printers and Imaging
- Digital Video Transport
- Machine Vision

3 Description

The DS90CR286A receiver converts the four LVDS data streams back into parallel 28 bits of LVCMOS data. Also available is the DS90CR216A receiver that converts the three LVDS data streams back into parallel 21 bits of LVCMOS data. The outputs of both receivers strobe on the rising edge.

The receiver LVDS clock operates at rates from 20 to 66 MHz. The device phase-locks to the input clock, samples the serial bit streams at the LVDS data lines, and converts them into parallel output data. At an incoming clock rate of 66 MHz, each LVDS input line is running at a bit rate of 462 Mbps, resulting in a maximum throughput of 1.848 Gbps for the DS90CR286A and 1.386 Gbps for the DS90CR216A.

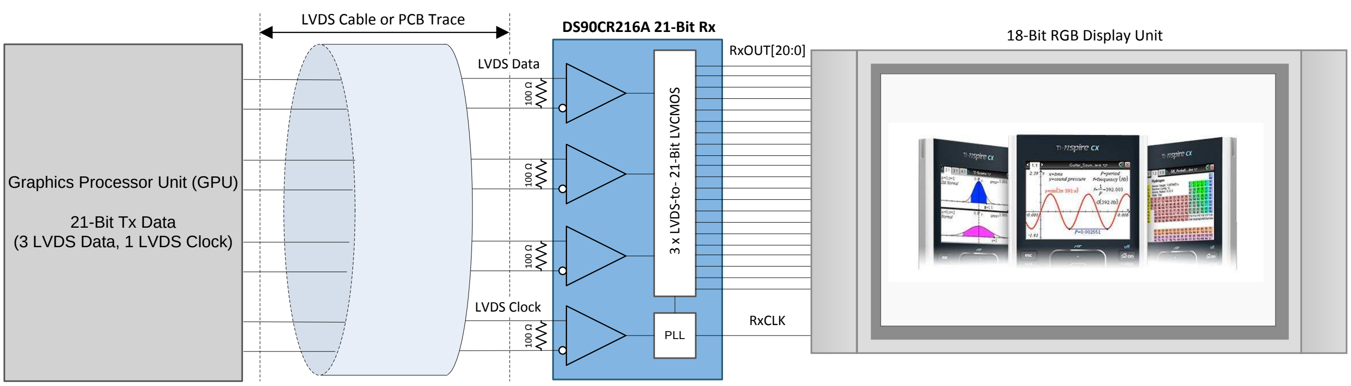
The DS90CR286A and DS90CR216A devices are enhanced over prior generation receivers and provide a wider data valid time on the receiver output. The use of these serial link devices is ideal for solving EMI and cable size problems associated with transmitting data over wide, high speed parallel LVCMOS interfaces. Both devices are offered in TSSOP packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90CR286AMTD	TSSOP (56)	14.00 mm x 6.10 mm
DS90CR286AQMT	TSSOP (56)	14.00 mm x 6.10 mm
DS90CR216AMTD	TSSOP (48)	12.50 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram (DS90CR216A)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (August 2015) to Revision H **Page**

- Changed Figure 6 and Figure 7 to clarify that TxIN on Tx is the same as RxOUT on Rx 9
- Changed "limit output amplitude" to "reduce reflections from long board traces" for clarification 18
- Deleted 0.01-µF and 0.001-µF caps from required DC power supply coupling capacitors 18
- Deleted "Setup and Hold Time" label from the Rx strobe window diagram to clarify RSKM concept 21
- Changed direction of Rx strobe position shift for correct left and right RSKM margin shift behavior 21
- Added new Application Note reference for RSKM improvement 21
- Added improved layout guidelines 23
- Changed Figure 28 graphic to clarify the use of series resistors on LVCMOS output 24

Changes from Revision F (February 2013) to Revision G **Page**

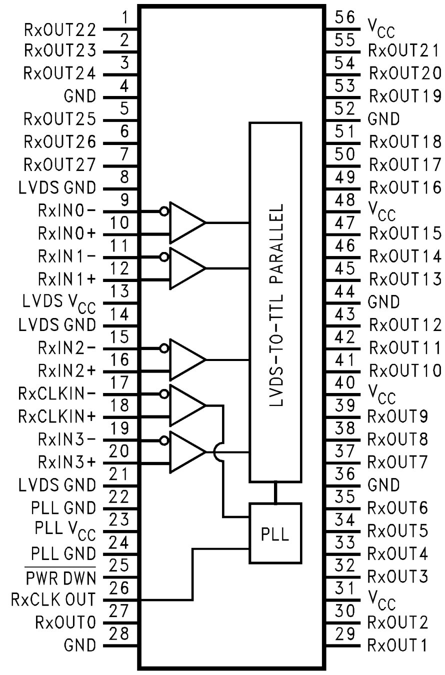
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Changed specification title to clarify 3.3 V LVCMOS and not standard 5 V CMOS 6
- Changed title and graphic of figure to clarify 3.3 V LVCMOS and not standard 5 V CMOS 8
- Changed title of DS90CR286A mapping to clarify the make-up of the LVDS lines 9
- Changed title of DS90CR216A mapping to clarify the make-up of the LVDS lines 9
- Added cycle-to-cycle jitter value of 250 ps instead of TBD ps 12

Changes from Revision E (February 2013) to Revision F **Page**

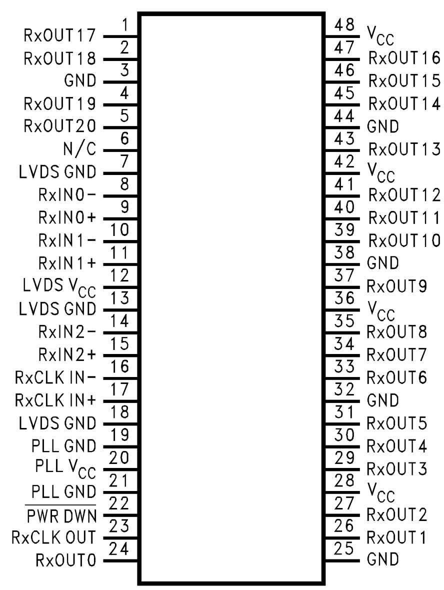
- Changed layout of National Data Sheet to TI format 3

5 Pin Configuration and Functions

DGG Package
56-Pin TSSOP
DS90CR286A Top View



DGG Package
48-Pin TSSOP
DS90CR216A Top View



DS90CR286A Pin Functions — DGG0056A Package — 28-Bit Channel Link Receiver

PIN NAME	PIN NO.	I/O , TYPE	PIN DESCRIPTION
RxIN0+, RxIN0-, RxIN1+, RxIN1-, RxIN2+, RxIN2-, RxIN3+, RxIN3-	10, 9, 12, 11, 16, 15, 20, 19	I, LVDS	Positive and negative LVDS differential data inputs. 100-Ω termination resistors should be placed between RxIN+ and RxIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxCLKIN+, RxCLKIN-	18, 17	I, LVDS	Positive and negative LVDS differential clock input. 100-Ω termination resistor should be placed between RxCLKIN+ and RxCLKIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxOUT[27:0]	7, 6, 5, 3, 2, 1, 55, 54, 53, 51, 50, 49, 47, 46, 45, 43, 42, 41, 39, 38, 37, 35, 34, 33, 32, 30, 29, 27	O, LVCMOS	LVCMOS level data outputs.
RxCLK OUT	26	O, LVCMOS	LVCMOS level clock output. The rising edge acts as the data strobe.
$\overline{\text{PWR DWN}}$	25	I, LVCMOS	LVCMOS level input. When asserted low, the receiver outputs are low.
V_{CC}	56, 48, 40, 31	Power	Power supply pins for LVCMOS outputs.
GND	52, 44, 36, 28, 4	Power	Ground pins for LVCMOS outputs.
PLL V_{CC}	23	Power	Power supply for PLL.
PLL GND	24, 22	Power	Ground pin for PLL.
LVDS V_{CC}	13	Power	Power supply pin for LVDS inputs.
LVDS GND	21, 14, 8	Power	Ground pins for LVDS inputs.

DS90CR216A Pin Functions — DGG0048A Package — 21-Bit Channel Link Receiver

PIN NAME	PIN NO.	I/O , TYPE	PIN DESCRIPTION
RxIN0+, RxIN0-, RxIN1+, RxIN1-, RxIN2+, RxIN2-	9, 8, 11, 10, 15, 14	I, LVDS	Positive and negative LVDS differential data inputs. 100-Ω termination resistors should be placed between RxIN+ and RxIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxCLKIN+, RxCLKIN-	17, 16	I, LVDS	Positive and negative LVDS differential clock input. 100-Ω termination resistor should be placed between RxCLKIN+ and RxCLKIN- receiver inputs as close as possible to the receiver pins for proper signaling.
RxOUT[20:0]	5, 4, 2, 1, 47, 46, 45, 43, 41, 40, 39, 37, 35, 34, 33, 31, 30, 29, 27, 26, 24	O, LVCMOS	LVCMOS level data outputs.
RxCLK OUT	23	O, LVCMOS	LVCMOS level clock output. The rising edge acts as the data strobe.
$\overline{\text{PWR DWN}}$	22	I, LVCMOS	LVCMOS level input. When asserted low, the receiver outputs are low.
V_{CC}	48, 42, 36, 28	Power	Power supply pins for LVCMOS outputs.
GND	44, 38, 32, 25, 3	Power	Ground pins for LVCMOS outputs.
PLL V_{CC}	20	Power	Power supply for PLL.
PLL GND	21, 19	Power	Ground pin for PLL.
LVDS V_{CC}	12	Power	Power supply pin for LVDS inputs.
LVDS GND	18, 13, 7	Power	Ground pins for LVDS inputs.

6 Specifications

6.1 Absolute Maximum Ratings

see [1][2]

	MIN	MAX	UNIT
Supply voltage (V_{CC})	–0.3	4	V
LVCMOS output voltage	–0.3	(V_{CC} + 0.3 V)	V
LVDS receiver input voltage	–0.3	(V_{CC} + 0.3 V)	V
Junction temperature		150	°C
Lead temperature (soldering, 4 sec)		260	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±7000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage (V_{CC})	3.0	3.3	3.6	V
Operating free air temperature (T_A)	–40	25	85	°C
Receiver input range	0		2.4	V
Supply noise voltage (V_{NOISE})			100	mV_{PP}

6.4 Thermal Information

THERMAL METRIC[1]		DS90CR286A/-Q1	DS90CR216A	UNIT
		DGG (TSSOP)	DGG (TSSOP)	
		56 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.6	67.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.6	22.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.3	34.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.0	34.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS DC SPECIFICATIONS (For $\overline{\text{PWR DWN}}$ Pin)							
V_{IH}	High Level Input Voltage			2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			–0.79	–1.5	V
I_{IN}	Input Current	V_{IN} = 0.4 V, 2.5 V or V_{CC}			1.8	10	μA
		V_{IN} = GND		–10	0		μA
LVCMOS DC SPECIFICATIONS							
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.06	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V			–60	–120	mA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				100	mV
V_{TL}	Differential Input Low Threshold			–100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	μA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	μA
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR286A (Figure 1 Figure 2), T_A=−10°C to +70°C	f = 33 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 66 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR286A (Figure 1 Figure 2), T_A=−40°C to +85°C	f = 40 MHz		53	70	mA
			f = 66 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR216A (Figure 1 Figure 2), T_A=−10°C to +70°C	f = 33 MHz		49	55	mA
			f = 37.5 MHz		53	60	mA
			f = 66 MHz		78	90	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR216A (Figure 1 Figure 2), T_A=−40°C to +85°C	f = 40 MHz		53	60	mA
			f = 66 MHz		78	90	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Receiver Outputs Stay Low during Power Down Mode			10	55	μA

(1) Typical values are given for V_{CC} = 3.3 V and T_A = 25ºC.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

6.6 Switching Characteristics: Receiver

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			MIN	TYP	MAX	UNIT
CLHT	LVCMOS Low-to-High Transition Time (Figure 2)			2	5	ns
CHLT	LVCMOS High-to-Low Transition Time (Figure 2)			1.8	5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 9, Figure 10)	f = 40 MHz	1	1.4	2.15	ns
RSPos1	Receiver Input Strobe Position for Bit 1	f = 40 MHz	4.5	5	5.8	ns
RSPos2	Receiver Input Strobe Position for Bit 2	f = 40 MHz	8.1	8.5	9.15	ns
RSPos3	Receiver Input Strobe Position for Bit 3	f = 40 MHz	11.6	11.9	12.6	ns
RSPos4	Receiver Input Strobe Position for Bit 4	f = 40 MHz	15.1	15.6	16.3	ns
RSPos5	Receiver Input Strobe Position for Bit 5	f = 40 MHz	18.8	19.2	19.9	ns
RSPos6	Receiver Input Strobe Position for Bit 6	f = 40 MHz	22.5	22.9	23.6	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 9, Figure 10)	f = 66 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1	f = 66 MHz	2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2	f = 66 MHz	5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3	f = 66 MHz	7.3	7.7	8	ns
RSPos4	Receiver Input Strobe Position for Bit 4	f = 66 MHz	9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5	f = 66 MHz	11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6	f = 66 MHz	13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin(2) (Figure 11)	f = 40 MHz	490			ps
		f = 66 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 3)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 3)	f = 40 MHz	10	12.2		ns
RCOL	RxCLK OUT Low Time (Figure 3)	f = 40 MHz	10	11		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 3)	f = 40 MHz	6.5	11.6		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 3)	f = 40 MHz	6	11.6		ns
RCOH	RxCLK OUT High Time (Figure 3)	f = 66 MHz	5	7.6		ns
RCOL	RxCLK OUT Low Time (Figure 3)	f = 66 MHz	5	6.3		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 3)	f = 66 MHz	4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 3)	f = 66 MHz	4	6.3		ns
RCCD	RxCLK IN to RxCLK OUT Delay at 25°C, V_{CC} = 3.3 V(3) (Figure 4)		3.5	5	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 5)				10	ms
RPDD	Receiver Power Down Delay (Figure 8)				1	µs

(1) Typical Values are given for V_{CC} = 3.3 V and T_A = 25ºC
(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).
(3) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the DS90CR215/DS90CR285 transmitter and DS90CR216A/DS90CR286A receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period.

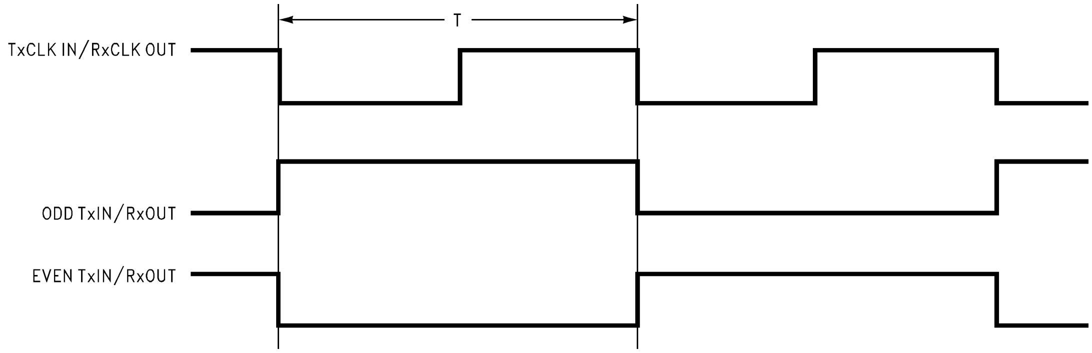


Figure 1. "Worst Case" Test Pattern

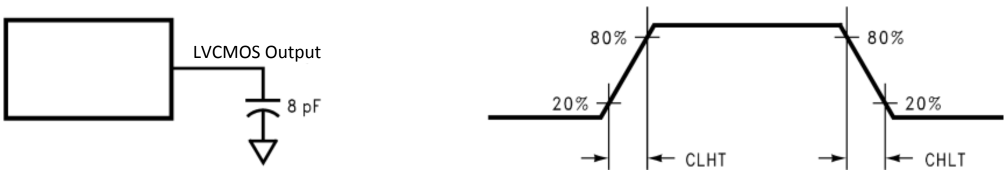


Figure 2. LVCMOS Output Load and Transition Times

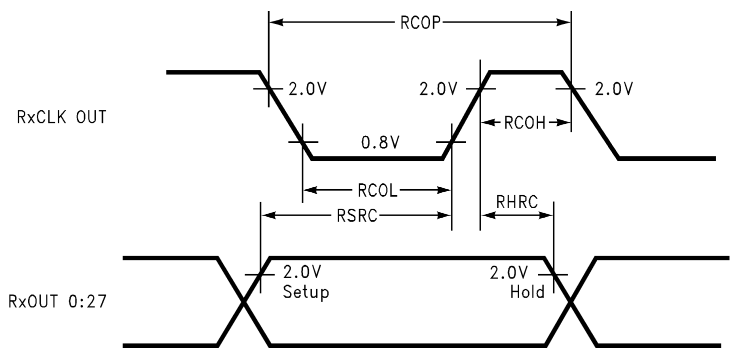


Figure 3. Setup/Hold and High/Low Times

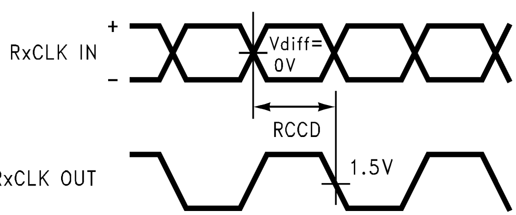


Figure 4. Clock In to Clock Out Delay

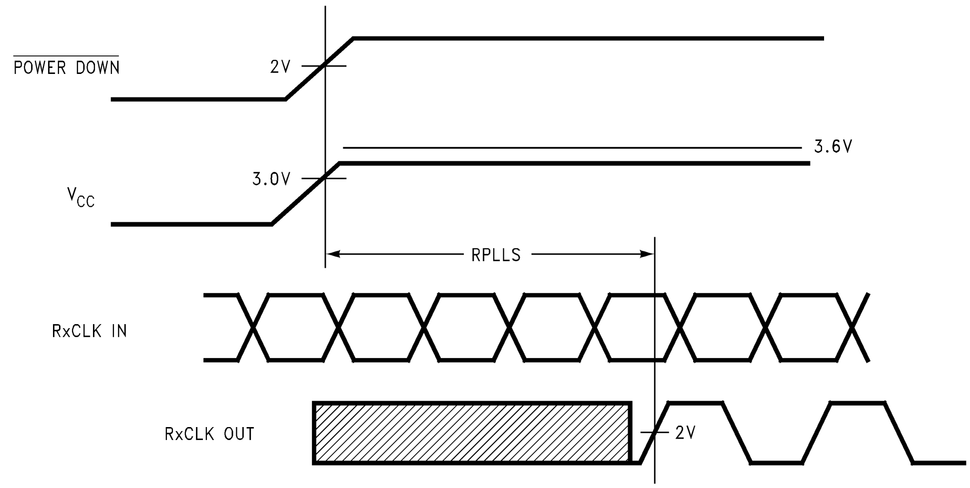


Figure 5. Phase Lock Loop Set Time

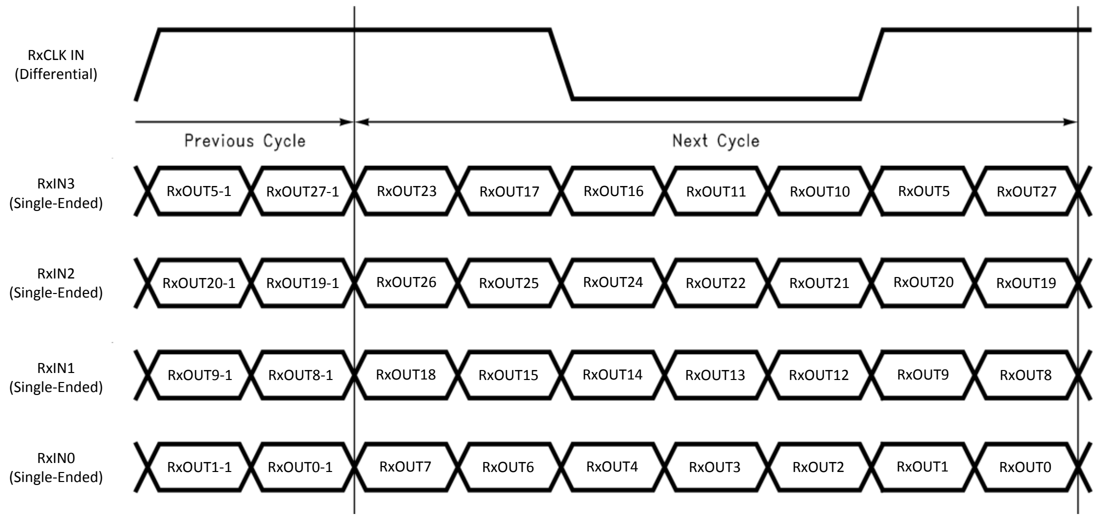


Figure 6. DS90CR286A Mapping of 28 LVCMOS Parallel Data to 4D + C LVDS Serialized Data

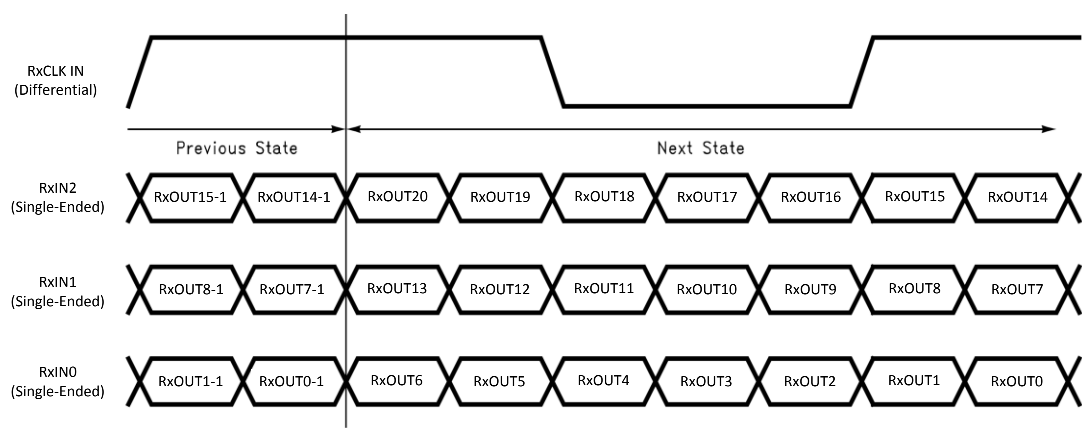


Figure 7. DS90CR216A Mapping of 21 LVCMOS Parallel Data to 3D + C LVDS Serialized Data

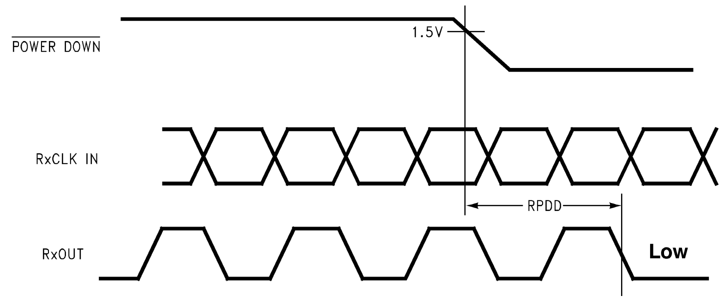


Figure 8. Power Down Delay

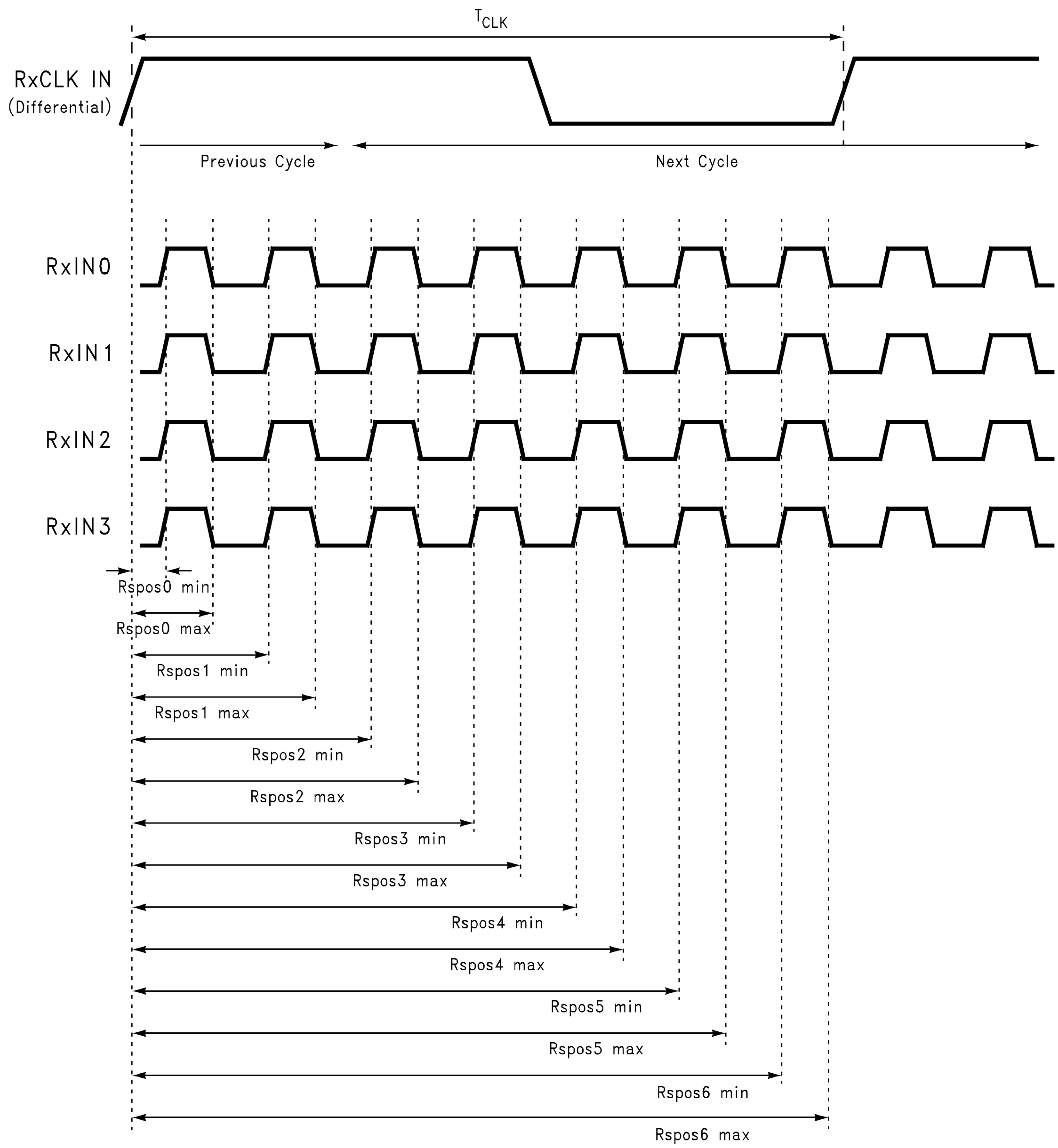


Figure 9. DS90CR286A LVDS Input Strobe Position

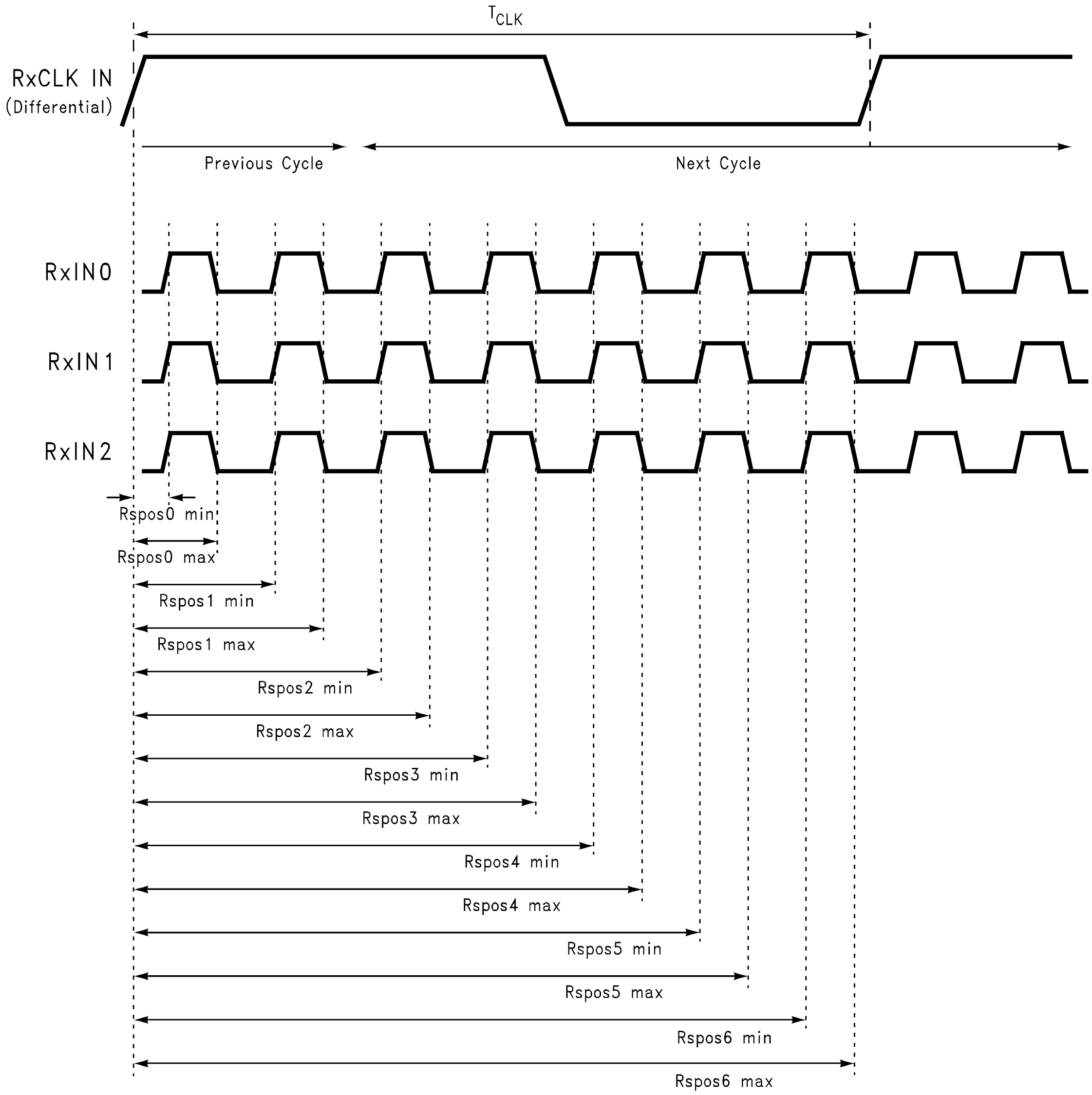
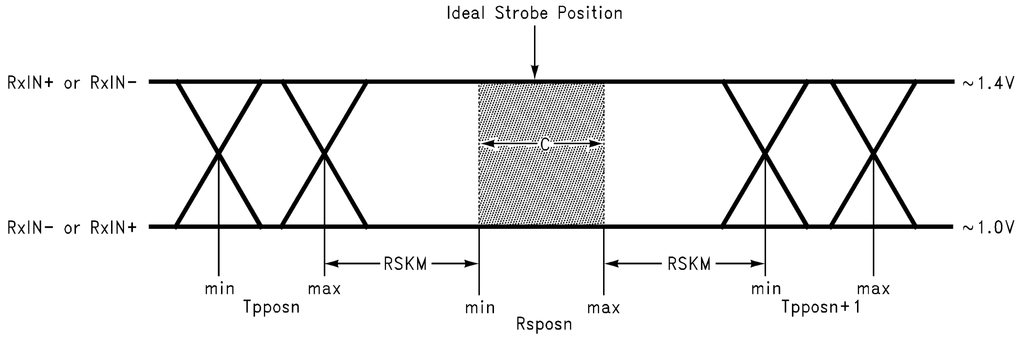


Figure 10. DS90CR216A LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos—Transmitter output pulse position (min and max)
Cable Skew—typically 10 ps–40 ps per foot, media dependent
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)(1) + ISI (Inter-symbol interference)(2)

(1) Cycle-to-cycle jitter depends on the Tx source. if a Channel Link I Source Transmitter is used, clock jitter is maintained to less than 250 ps at 66 MHz.

(2) ISI is dependent on interconnect length; may be zero.

Figure 11. Receiver LVDS Input Skew Margin

6.7 Typical Characteristics

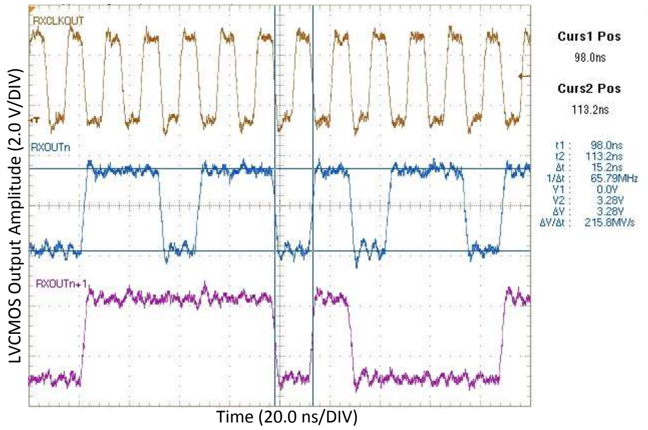


Figure 12. Parallel PRBS-7 on LVCMOS Outputs at 66 MHz

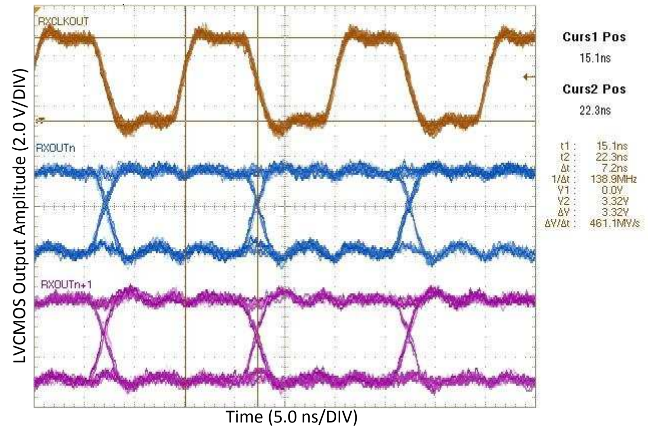


Figure 13. Typical RxOUT Strobe Position at 66 MHz

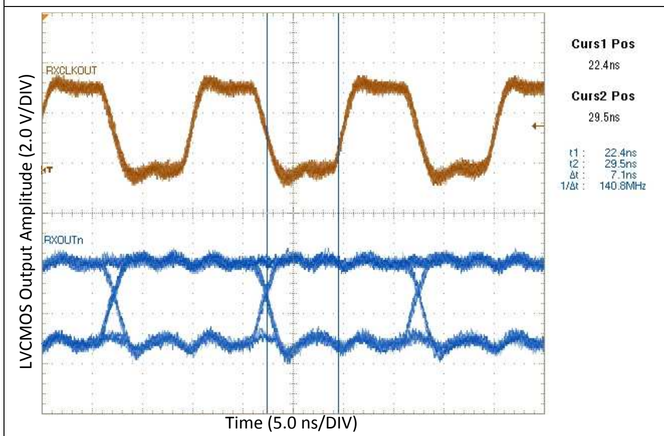


Figure 14. Typical RxOUT Setup Time at 66 MHz (RSRC = 7.1 ns)

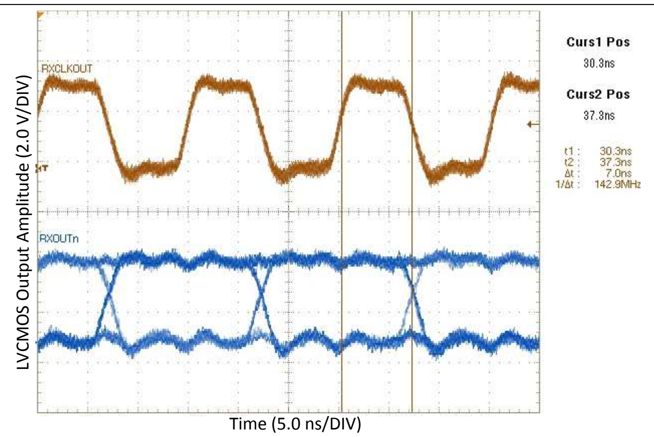


Figure 15. Typical RxOUT Hold Time at 66 MHz (RHRC = 7.0 ns)

7 Detailed Description

7.1 Overview

The DS90CR286A and DS90CR286A-Q1 are receivers that convert four LVDS (Low Voltage Differential Signaling) data streams into parallel 28 bits of LVCMOS data (24 bits of RGB and 4 bits of HSYNC, VSYNC, DE, and CNTL). The DS90CR216A is a receiver that converts three LVDS data streams back into parallel 21 bits of LVCMOS data (18 bits of RGB and 3 bits of HSYNC, VSYNC, and DE). An internal PLL locks to the incoming LVDS clock ranging from 20 to 66 MHz. The locked PLL ensures a stable clock to sample the output LVCMOS data on the Receiver Clock Out rising edge. These devices feature a $\overline{\text{PWR DWN}}$ pin to put the device into low power mode when there is no active input data.

7.2 Functional Block Diagrams

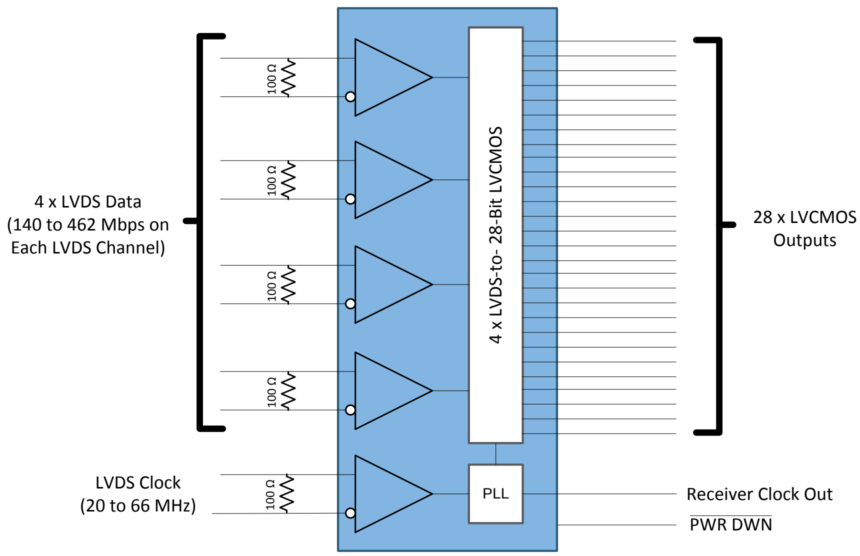


Figure 16. DS90CR286A Block Diagram

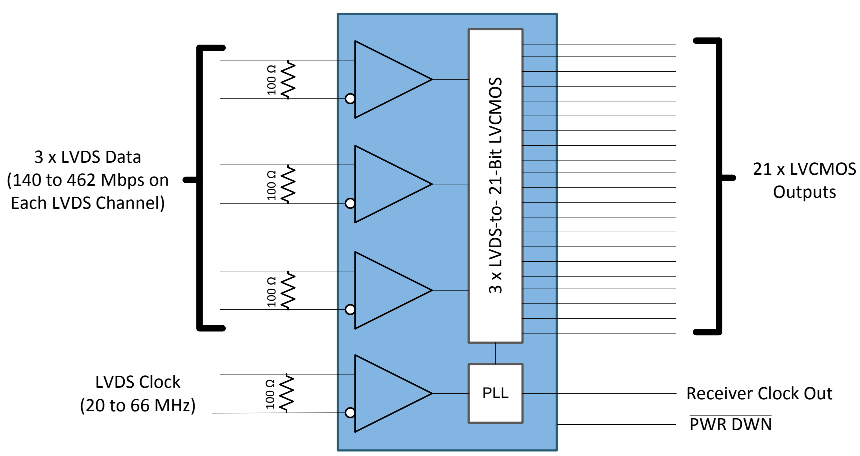


Figure 17. DS90CR216A Block Diagram

7.3 Feature Description

The DS90CR286A and DS90CR216A consist of several key blocks:

- LVDS Receivers
- Phase Locked Loop (PLL)
- Serial LVDS-to-Parallel LVCMOS Converter
- LVCMOS Drivers

7.3.1 LVDS Receivers

There are five differential LVDS inputs to the DS90CR286A and four differential LVDS inputs to the DS90CR216A. Four of the LVDS inputs contain serialized data originating from a 28-bit source transmitter. For the DS90CR216A, three of the LVDS inputs contain serialized data originating from a 21-bit source transmitter. The remaining LVDS input contains the LVDS clock associated with the data pairs.

7.3.1.1 LVDS Input Termination

The DS90CR286A and DS90CR216A require a single 100-Ω terminating resistor across the true and complement lines on each differential pair of the receiver input. To prevent reflections due to stubs, this resistor should be placed as close to the device input pins as possible. Figure 18 shows an example.

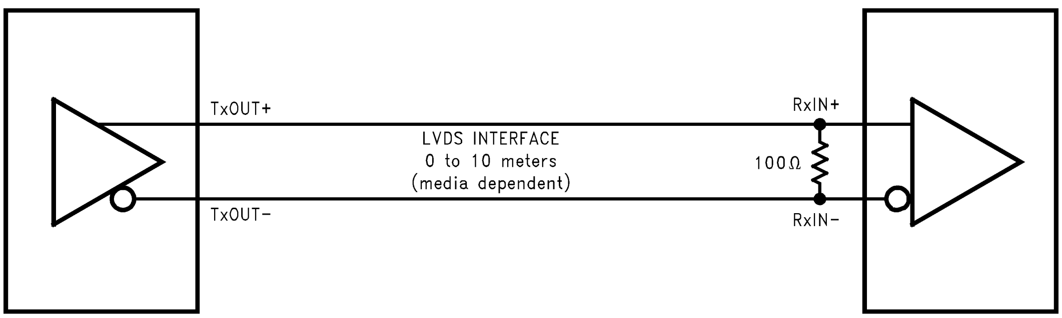


Figure 18. LVDS Serialized Link Termination

7.3.2 Phase Locked Loop (PLL)

The Channel Link I devices use an internal PLL to recover the clock transmitted across the LVDS interface. The recovered clock is then used as a reference to determine the sampling position of the seven serial bits received per clock cycle. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock to improve the overall jitter budget.

7.3.3 Serial LVDS-to-Parallel LVCMOS Converter

After the PLL locks to the incoming LVDS clock, the receiver deserializes each LVDS differential data pair into seven parallel LVCMOS data outputs per clock cycle. For the DS90CR286A, the LVDS data inputs map to LVCMOS outputs according to Figure 6. For the DS90CR216A, the LVDS data inputs map to LVCMOS outputs according to Figure 7.

7.3.4 LVCMOS Drivers

The LVCMOS outputs from the DS90CR286A and DS90CR216A are the deserialized parallel single-ended data from the serialized LVDS differential data pairs. Each LVCMOS output is clocked by the PLL and strobes on the RxCLKOUT rising edge. All unused DS90CR286A and DS90CR216A RxOUT outputs can be left floating.

7.4 Device Functional Modes

7.4.1 Power Down Mode

The DS90CR286A and DS90CR216A may be placed into a power down mode at any time by asserting the $\overline{\text{PWR DWN}}$ pin (active low). The DS90CR286A and DS90CR216A are also designed to protect themselves from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited to 5 mA per input, thus avoiding the potential for latch-up when powering the device.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90CR286A and DS90CR216A are designed for a wide variety of data transmission applications. The use of serialized LVDS data lines in these applications allows for efficient signal transmission over a narrow bus width, thereby reducing cost, power, and space.

8.2 Typical Applications

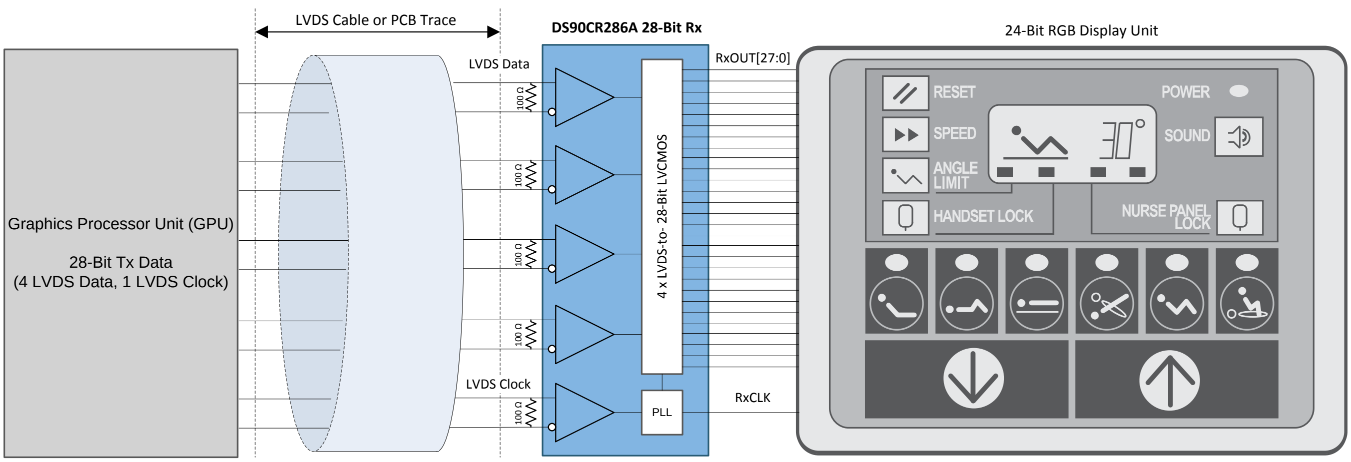


Figure 19. Typical DS90CR286A Application Block Diagram

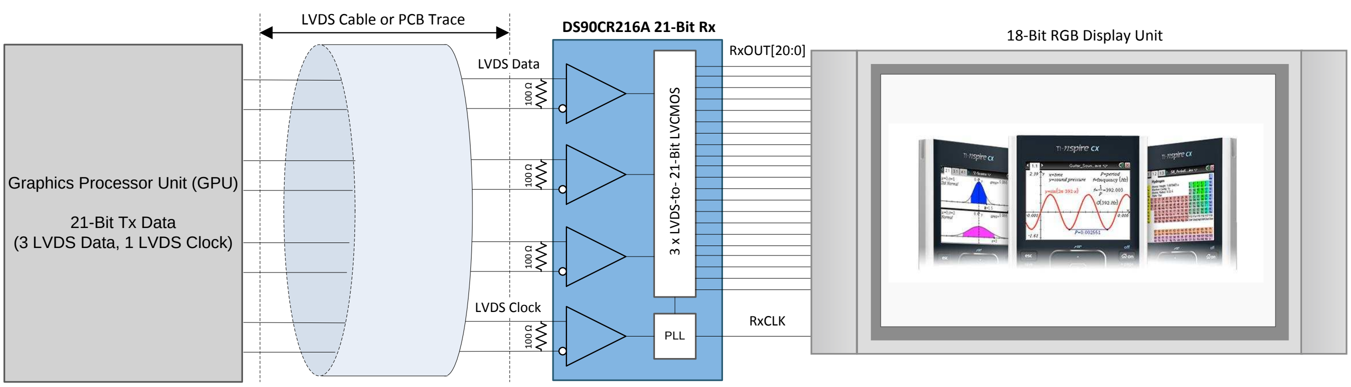


Figure 20. Typical DS90CR216A Application Block Diagram

Typical Applications (continued)

8.2.1 Design Requirements

For this design example, ensure that the following requirements are observed.

Table 1. Design Parameters

DESIGN PARAMETER	DESIGN REQUIREMENTS
Operating Frequency	LVDS clock must be within 20-66 MHz.
Bit Resolution	DS90CR286A: No higher than 24 bpp. The maximum supported resolution is 8-bit RGB. DS90CR216A: No higher than 18 bpp. The maximum supported resolution is 6-bit RGB.
Bit Data Mapping	Determine the appropriate mapping required by the panel display following the DS90CR286A or DS90CR216A outputs.
RSKM (Receiver Skew Margin)	Ensure that there is acceptable margin between Tx pulse position and Rx strobe position.
Input Termination for RxIN±	100 Ω ± 10% resistor across each LVDS differential pair. Place as close as possible to IC input pins.
RxIN± Board Trace Impedance	Design differential trace impedance with 100 Ω ± 5%
LVCMOS Outputs	If unused, leave pins floating. Series resistance on each LVCMOS output optional to reduce reflections from long board traces. If used, 33-Ω series resistance is typical.
DC Power Supply Coupling Capacitors	Use a 0.1-µF capacitor to minimize power supply noise. Place as close as possible to V_{CC} pins.

8.2.2 Detailed Design Procedure

To design with the DS90CR286A or DS90CR216A, determine the following:

- Cable Interface
- Bit Resolution and Operating Frequency
- Bit Mapping from Receiver to Endpoint Panel Display
- RSKM Interoperability with Transmitter Pulse Position Margin

8.2.2.1 Cables

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The DS90CR216A requires four pairs of signal wires and the DS90CR286A requires five pairs of signal wires. The ideal cable interface has a constant 100-Ω differential impedance throughout the path. It is also recommended that cable skew remain below 150 ps (assuming 66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

Depending upon the application and data rate, the interconnecting media between Tx and Rx may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed or long distance applications, the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). For example, twin-coax cables have been demonstrated at distances as long as five meters and with the maximum data transfer of 1.386 Gbps (DS90CR216A) and 1.848 Gbps (DS90CR286A).

8.2.2.2 Bit Resolution and Operating Frequency Compatibility

The bit resolution of the endpoint panel display reveals whether there are enough bits available in the DS90CR286A or DS90CR216A to output the required data per pixel. The DS90CR286A has 28 parallel LVCMOS outputs and can therefore provide a bit resolution up to 24 bpp (bits per pixel). In each clock cycle, the remaining bits are the three control signals (HSync, VSync, DE) and one spare bit. The DS90CR216A has 21 parallel LVCMOS outputs and can therefore provide a bit resolution up to 18 bpp (bits per pixel). In each clock cycle, the remaining bits are the three control signals (HSync, VSync, DE).

The number of pixels per frame and the refresh rate of the endpoint panel display indicate the required operating frequency of the deserializer clock. To determine the required clock frequency, refer to the following formula:

$$f\_Clk = [H\_Active + H\_Blank] \times [V\_Active + V\_Blank] \times f\_Vertical$$

where

- H_Active = Active Display Horizontal Lines

- H_Blank = Blanking Period Horizontal Lines
- V_Active = Active Display Vertical Lines
- V_Blank = Blanking Period Vertical Lines
- f_Vertical = Refresh Rate (in Hz)
- f_Clk = Operating Frequency of LVDS clock (1)

In each frame, there is a blanking period associated with horizontal rows and vertical columns that are not actively displayed on the panel. These blanking period pixels must be included to determine the required clock frequency. Consider the following example to determine the required LVDS clock frequency:

- H_Active = 640
- H_Blank = 40
- V_Active = 480
- V_Blank = 41
- f_Vertical = 59.95 Hz

Thus, the required operating frequency is determined below:

$$[640 + 40] \times [480 + 41] \times 59.95 = 21239086 \text{ Hz} \approx 21.24 \text{ MHz} \quad (2)$$

Since the operating frequency for the PLL in the DS90CR286A and DS90CR216A ranges from 20-66 MHz, the DS90CR286A and DS90CR216A can support a panel display with the aforementioned requirements.

If the specific blanking interval is unknown, the number of pixels in the blanking interval can be approximated to 20% of the active pixels. The following formula can be used as a conservative approximation for the operating LVDS clock frequency:

$$f\_Clk \approx H\_Active \times V\_Active \times f\_Vertical \times 1.2 \quad (3)$$

Using this approximation, the operating frequency for the example in this section is estimated below:

$$640 \times 480 \times 59.95 \times 1.2 = 22099968 \text{ Hz} \approx 22.10 \text{ MHz} \quad (4)$$

8.2.2.3 Data Mapping between Receiver and Endpoint Panel Display

Ensure that the LVCMOS outputs are mapped to align with the endpoint display RGB mapping requirements following the deserializer. Two popular mapping topologies for 8-bit RGB data are shown below:

1. LSBs are mapped to RxIN3±.
2. MSBs are mapped to RxIN3±.

The following tables depict how these two popular topologies can be mapped to the DS90CR286A outputs.

Table 2. 8-Bit Color Mapping with LSBs on RxIN3±

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN0	TxIN0	RxOUT0	R2	
	TxIN1	RxOUT1	R3	
	TxIN2	RxOUT2	R4	
	TxIN3	RxOUT3	R5	
	TxIN4	RxOUT4	R6	
	TxIN6	RxOUT6	R7	MSB
RxIN1	TxIN7	RxOUT7	G2	
	TxIN8	RxOUT8	G3	
	TxIN9	RxOUT9	G4	
	TxIN12	RxOUT12	G5	
	TxIN13	RxOUT13	G6	
	TxIN14	RxOUT14	G7	MSB
	TxIN15	RxOUT15	B2	
	TxIN18	RxOUT18	B3	

Table 2. 8-Bit Color Mapping with LSBs on RxIN3± (continued)

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN2	TxIN19	RxOUT19	B4	
	TxIN20	RxOUT20	B5	
	TxIN21	RxOUT21	B6	
	TxIN22	RxOUT22	B7	MSB
	TxIN24	RxOUT24	HSYNC	Horizontal Sync
	TxIN25	RxOUT25	VSYNC	Vertical Sync
	TxIN26	RxOUT26	DE	Data Enable
RxIN3	TxIN27	RxOUT27	R0	LSB
	TxIN5	RxOUT5	R1	
	TxIN10	RxOUT10	G0	LSB
	TxIN11	RxOUT11	G1	
	TxIN16	RxOUT16	B0	LSB
	TxIN17	RxOUT17	B1	
	TxIN23	RxOUT23	GP	General Purpose

Table 3. 8-Bit Color Mapping with MSBs on RxIN3±

LVDS INPUT CHANNEL	LVDS BIT STREAM POSITION	LVCMOS OUTPUT CHANNEL	COLOR MAPPING	COMMENTS
RxIN0	TxIN0	RxOUT0	R0	LSB
	TxIN1	RxOUT1	R1	
	TxIN2	RxOUT2	R2	
	TxIN3	RxOUT3	R3	
	TxIN4	RxOUT4	R4	
	TxIN6	RxOUT6	R5	
RxIN1	TxIN7	RxOUT7	G0	LSB
	TxIN8	RxOUT8	G1	
	TxIN9	RxOUT9	G2	
	TxIN12	RxOUT12	G3	
	TxIN13	RxOUT13	G4	
	TxIN14	RxOUT14	G5	
	TxIN15	RxOUT15	B0	LSB
	TxIN18	RxOUT18	B1	
RxIN2	TxIN19	RxOUT19	B2	
	TxIN20	RxOUT20	B3	
	TxIN21	RxOUT21	B4	
	TxIN22	RxOUT22	B5	
	TxIN24	RxOUT24	HSYNC	Horizontal Sync
	TxIN25	RxOUT25	VSYNC	Vertical Sync
	TxIN26	RxOUT26	DE	Data Enable
RxIN3	TxIN27	RxOUT27	R6	
	TxIN5	RxOUT5	R7	MSB
	TxIN10	RxOUT10	G6	
	TxIN11	RxOUT11	G7	MSB
	TxIN16	RxOUT16	B6	
	TxIN17	RxOUT17	B7	MSB
	TxIN23	RxOUT23	GP	General Purpose

In either the case where the DS90CR216A is used or the DS90CR286A must support 18 bpp, Table 2 is commonly used. With this mapping, MSBs of RGB data are retained on RXIN0±, RXIN1±, and RXIN2± while the two LSBs for the original 8-bit RGB resolution are ignored from RxIN3±.

8.2.2.4 RSKM Interoperability

One of the most important factors when designing the receiver into a system application is assessing how much RSKM (Receiver Skew Margin) is available. In each LVDS clock cycle, the LVDS data stream carries seven serialized data bits. Ideally, the Transmit Pulse Position for each bit will occur every (n x T)/7 seconds, where n = Bit Position and T = LVDS Clock Period. Likewise, ideally the Receive Strobe Position for each bit will occur every ((n + 0.5) x T)/7 seconds. However, due to the effects of cable skew, clock jitter, and ISI, both LVDS transmitter and receiver in real systems will have a minimum and maximum pulse and strobe position, respectively, for each bit position. This concept is illustrated in Figure 21:

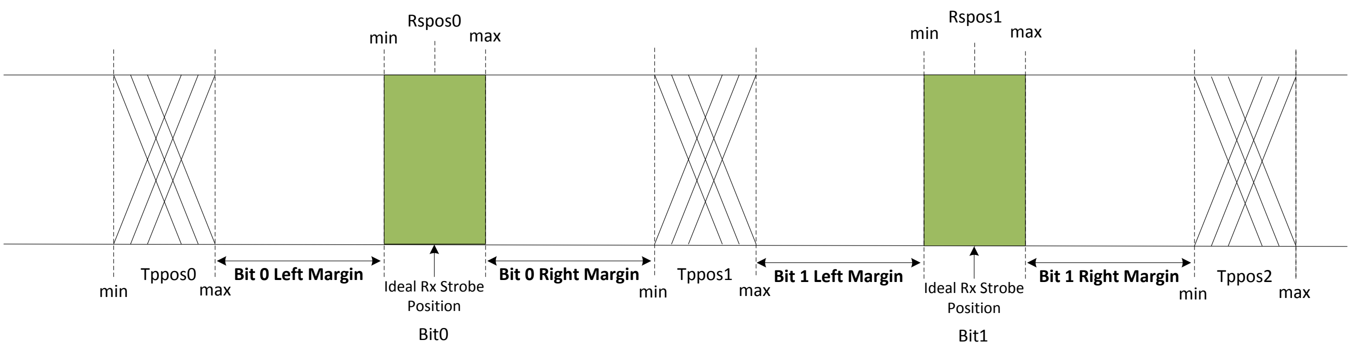


Figure 21. RSKM Measurement Example

All left and right margins for Bits 0-6 must be considered in order to determine the absolute minimum for the whole LVDS bit stream. This absolute minimum corresponds to the RSKM.

To improve RSKM performance between LVDS transmitter and receiver, designers often either advance or delay the LVDS clock compared to the LVDS data. Moving the LVDS clock compared to the LVDS data can improve the location of the setup and hold time for the transmitter compared to the setup and hold time for the receiver.

If there is less left bit margin than right bit margin, the LVDS clock can be delayed so that the Rx strobe position for incoming data appears to be delayed. If there is less right bit margin than left bit margin, all the LVDS data pairs can be delayed uniformly so that the LVDS clock and Rx strobe position for incoming data appear to advance. To delay an LVDS data or clock pair, designers either add more PCB trace length or install a capacitor between the LVDS transmitter and receiver. It is important to note that when using these techniques, all serialized bit positions are shifted right or left uniformly.

When designing the DS90CR286A or DS90CR216A receiver with a third-party OpenLDI transmitter, users must calculate the skew margin budget (RSKM) based on the Tx pulse position and the Rx strobe position to ensure error-free transmission. For more information about calculating RSKM, refer to Application Note SNLA249.

8.2.3 Application Curves

The following application curves are examples taken with a DS90C385 serializer interfacing to a DS90CR286A deserializer in nominal temperature (25ºC) at an operating frequency of 66 MHz.

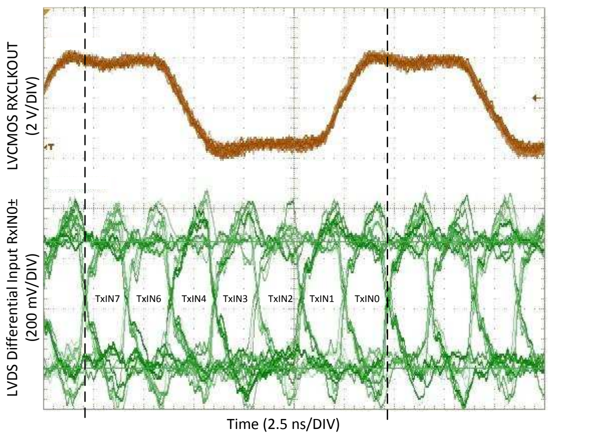


Figure 22. LVDS RxIN0± aligned with LVCMOS RxCLKOUT

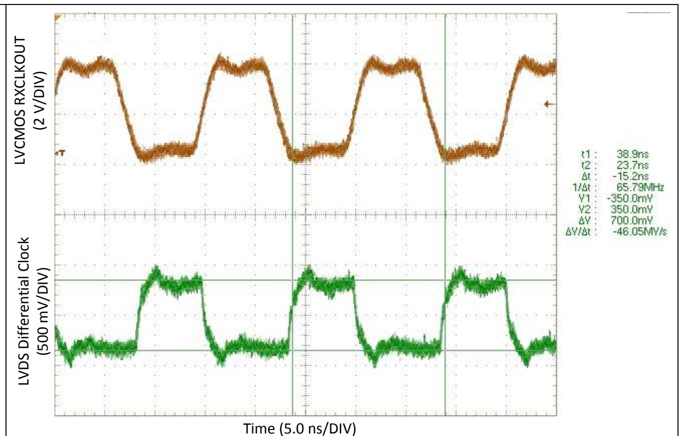


Figure 23. LVDS CLKIN aligned with LVCMOS RxCLKOUT

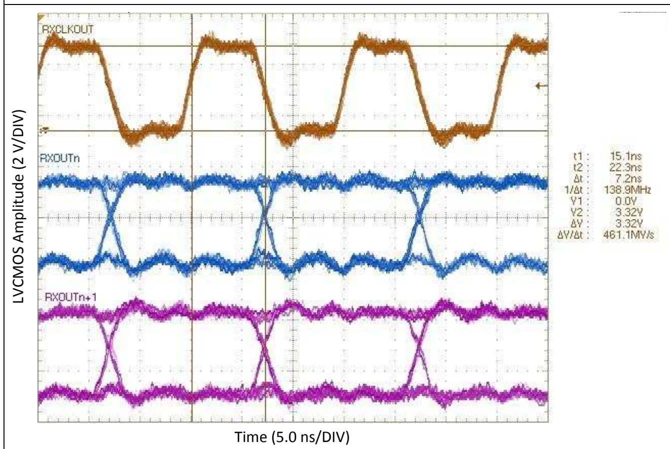


Figure 24. RxOUT Strobe on Rising Edge of RxCLKOUT

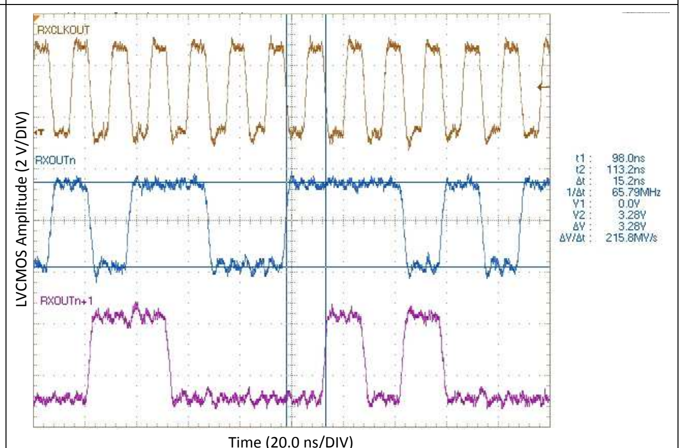


Figure 25. PRBS-7 Output on RxOUT Channels

9 Power Supply Recommendations

Proper power supply decoupling is important to ensure a stable power supply with minimal power supply noise. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01 µF and 0.001 µF. The preferred capacitor size is 0402. An example is shown in Figure 26. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

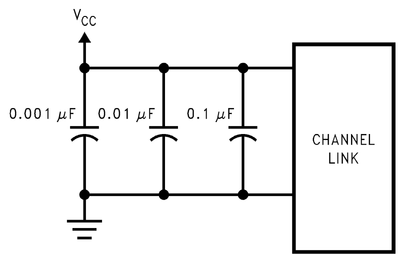


Figure 26. Recommended Bypass Capacitor Decoupling Configuration

10 Layout

10.1 Layout Guidelines

As with any high speed design, board designers must maximize signal integrity by limiting reflections and crosstalk that can adversely affect high frequency and EMI performance. The following practices are recommended layout guidelines to optimize device performance.

- Ensure that differential pair traces are always closely coupled to eliminate noise interference from other signals and take full advantage of the common mode noise canceling effect of the differential signals.
- Maintain equal length on signal traces for a given differential pair.
- Limit impedance discontinuities by reducing the number of vias on signal traces.
- Eliminate any 90º angles on traces and use 45º bends instead.
- If a via must exist on one signal polarity, mirror the via implementation on the other polarity of the differential pair.
- Match the differential impedance of the selected physical media. This impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input.
- When possible, use short traces for LVDS inputs.

10.2 Layout Examples

The following images show an example layout of the DS90CR286A.Traces in blue correspond to the top layer and the traces in green correspond to the bottom layer. Note that differential pair inputs to the DS90CR286A are tightly coupled and close to the connector pins. In addition, observe that the power supply decoupling capacitors are placed as close as possible to the power supply pins with through vias in order to minimize inductance. The principles illustrated in this layout can also be applied to the 48-pin DS90CR216A.

Layout Examples (continued)

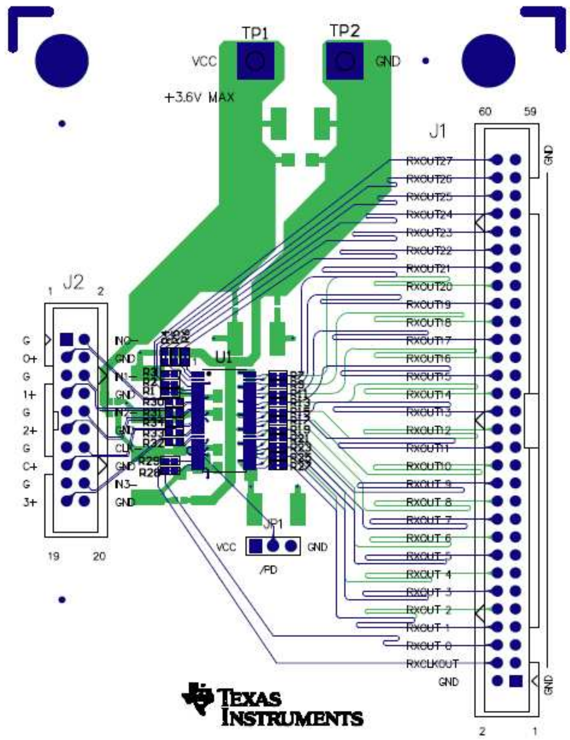


Figure 27. Example Layout With DS90CR286A (U1)

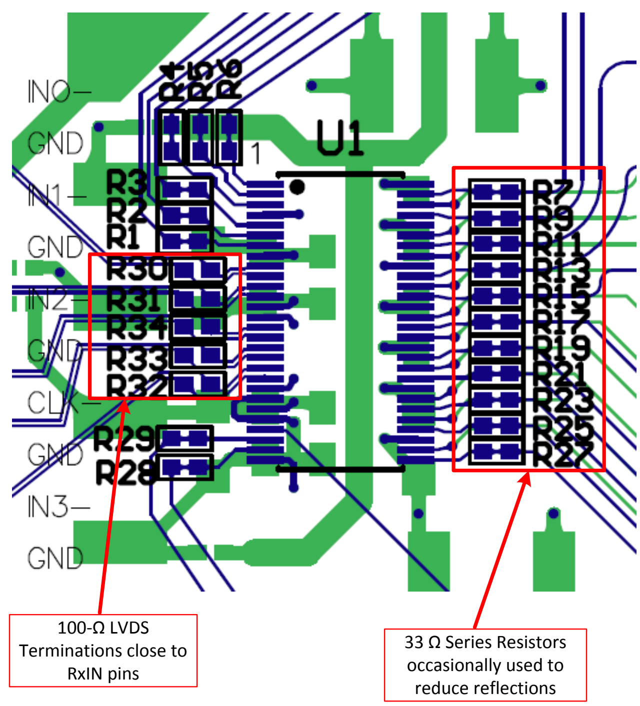


Figure 28. Example Layout Close-up

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DS90CR216A	Click here	Click here	Click here	Click here	Click here
DS90CR286A	Click here	Click here	Click here	Click here	Click here
DS90CR286A-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90CR216AMTD/NOPB	Active	Production	TSSOP (DGG) | 48	38 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR216AMTD >B
DS90CR216AMTD/NOPB.B	Active	Production	TSSOP (DGG) | 48	38 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR216AMTD >B
DS90CR216AMTDX/NOPB	Active	Production	TSSOP (DGG) | 48	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR216AMTD >B
DS90CR286AMTD/NOPB	Active	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AMTD >B
DS90CR286AMTD/NOPB.B	Active	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AMTD >B
DS90CR286AMTDX/NOPB	Active	Production	TSSOP (DGG) | 56	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AMTD >B
DS90CR286AQMT/NOPB	Active	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AQ MT
DS90CR286AQMT/NOPB.B	Active	Production	TSSOP (DGG) | 56	34 | TUBE	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AQ MT
DS90CR286AQMTX/NOPB	Active	Production	TSSOP (DGG) | 56	1000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AQ MT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DS90CR286A, DS90CR286A-Q1 :

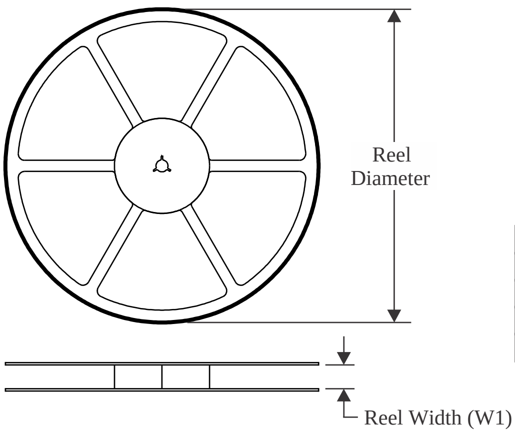
- Catalog : DS90CR286A
- Automotive : DS90CR286A-Q1

NOTE: Qualified Version Definitions:

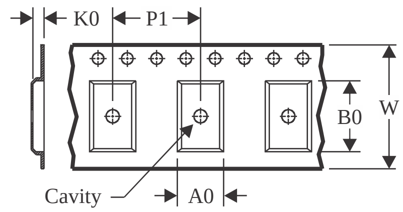
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

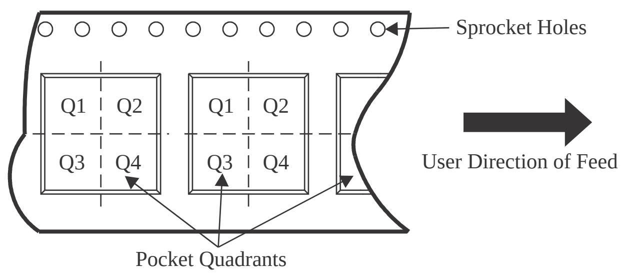


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

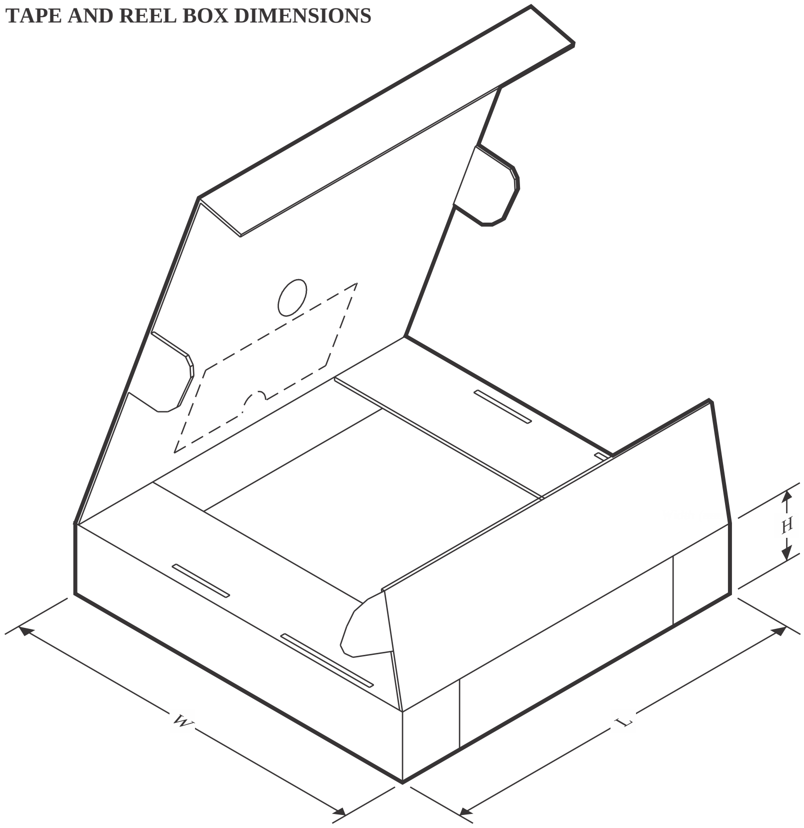
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR216AMTDX/ NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CR286AMTDX/ NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
DS90CR286AQMTX/ NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

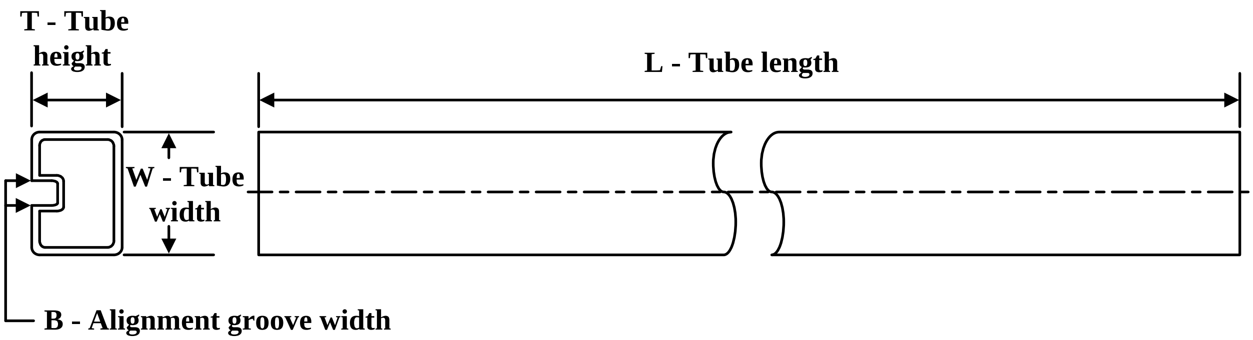
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

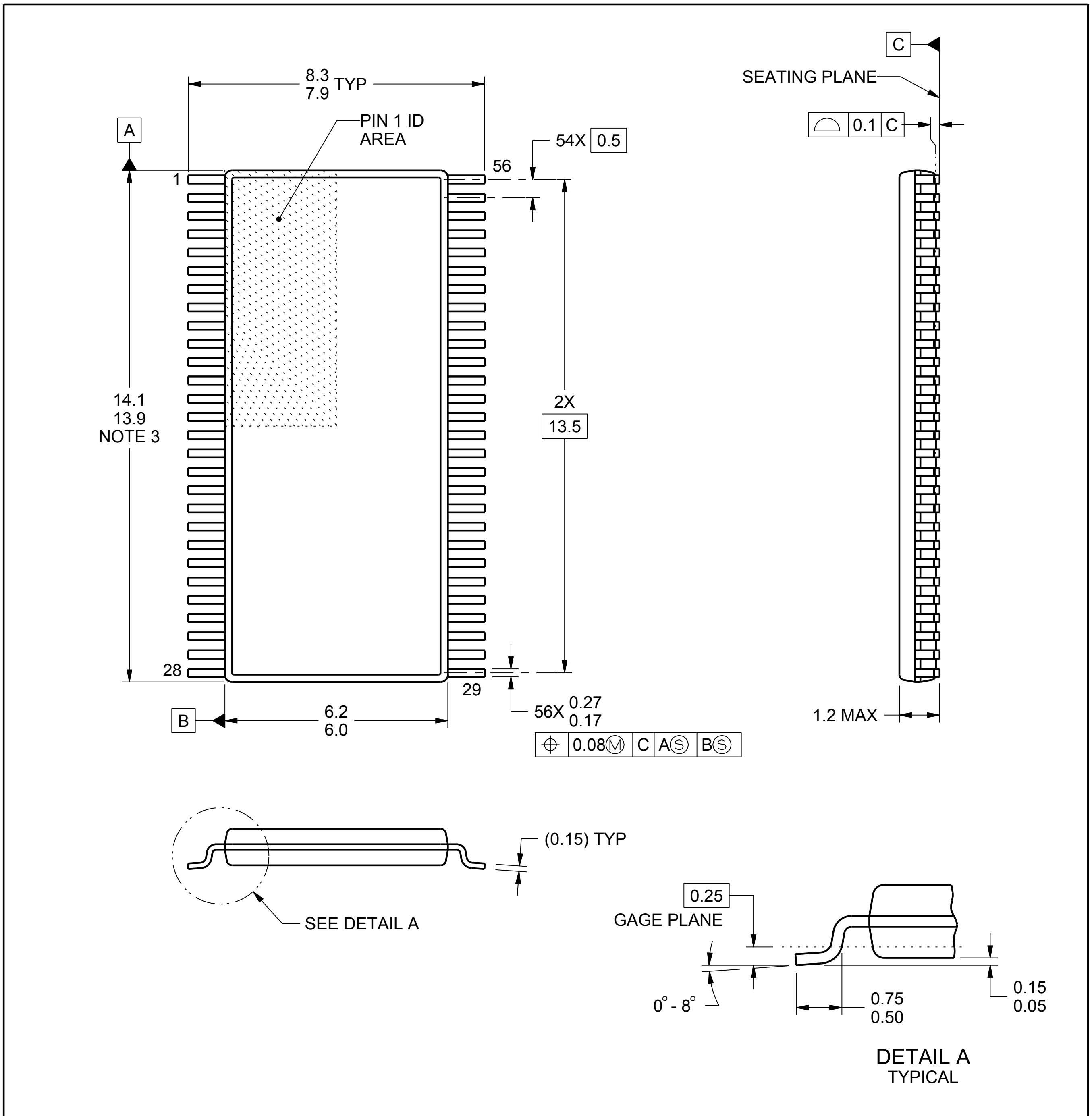
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR216AMTDX/NOPB	TSSOP	DGG	48	1000	356.0	356.0	45.0
DS90CR286AMTDX/NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0
DS90CR286AQMTX/ NOPB	TSSOP	DGG	56	1000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

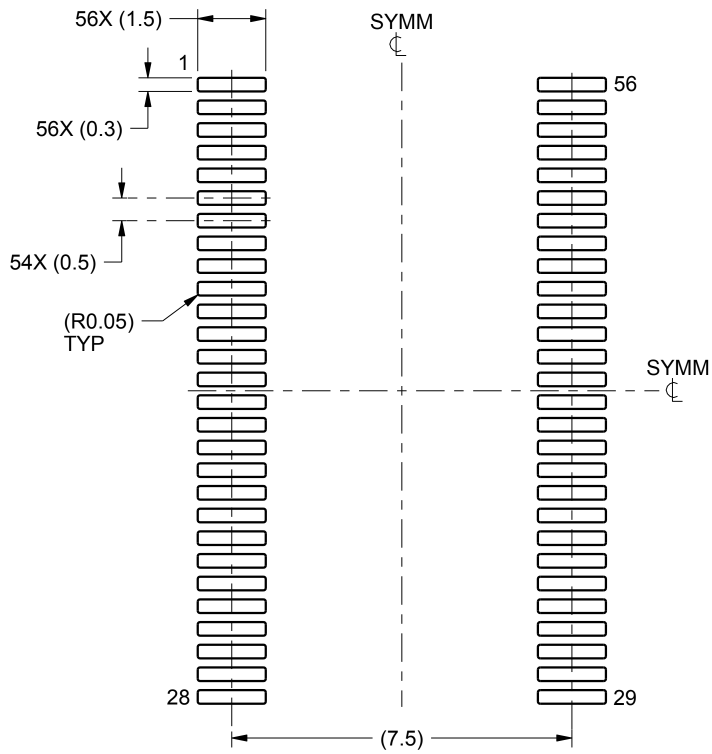
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90CR216AMTD/NOPB	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR216AMTD/NOPB.B	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR286AMTD/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR286AMTD/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR286AQMT/NOPB	DGG	TSSOP	56	34	495	10	2540	5.79
DS90CR286AQMT/NOPB.B	DGG	TSSOP	56	34	495	10	2540	5.79



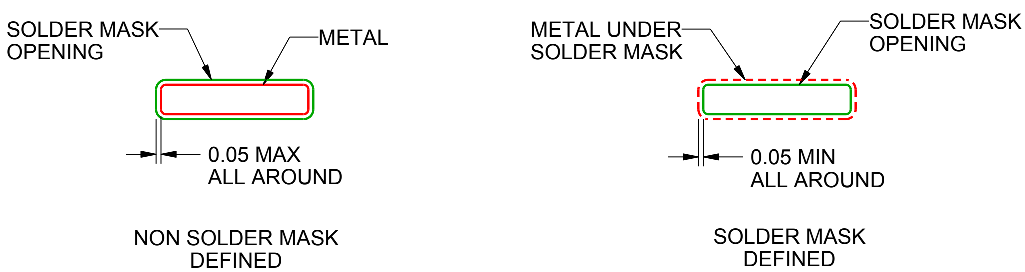
4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

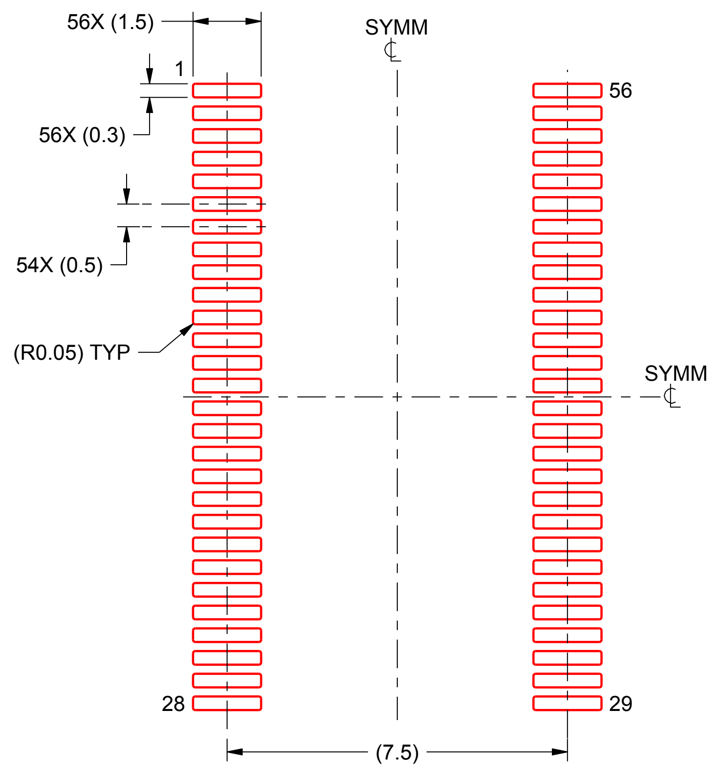


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

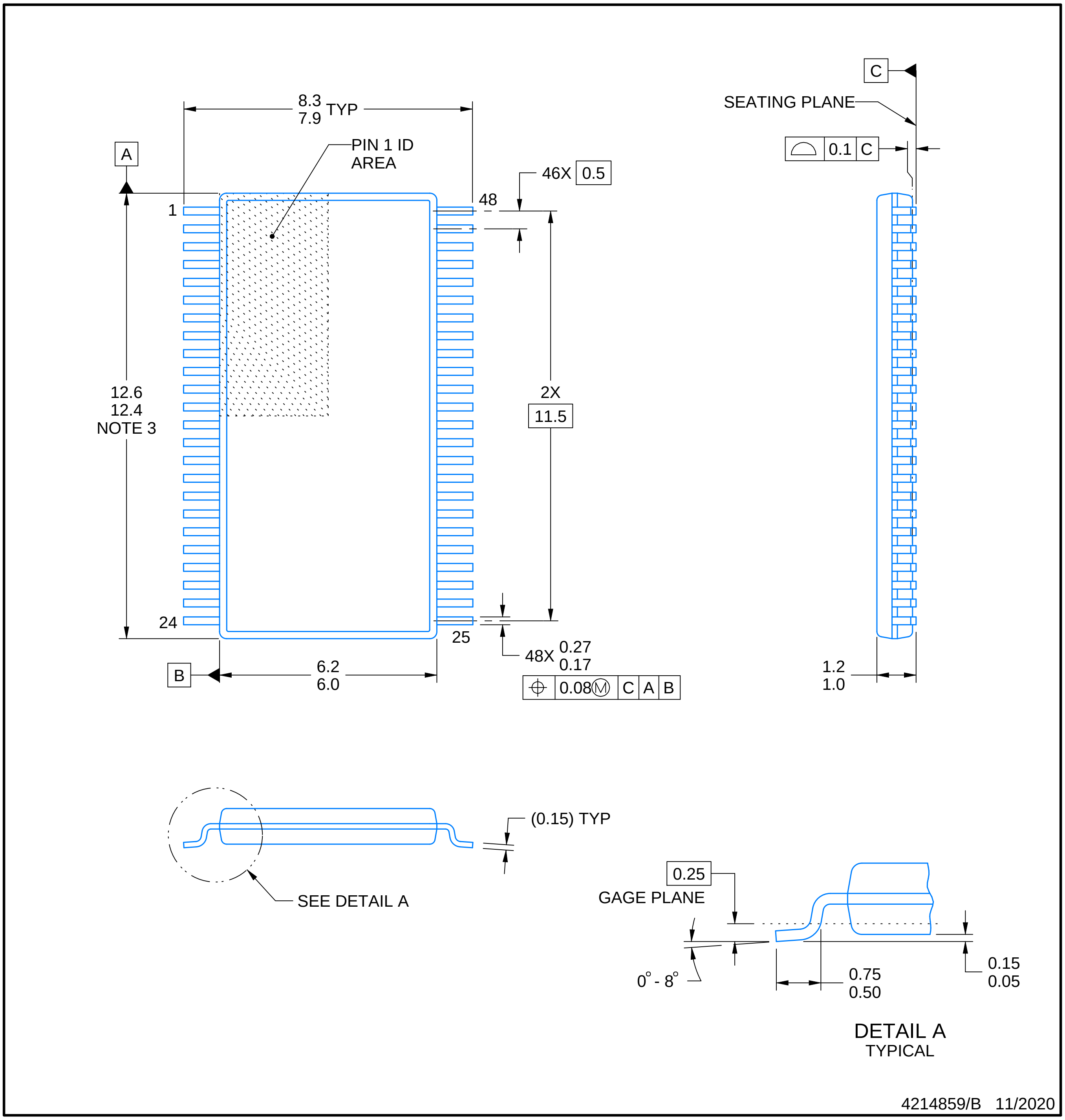


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

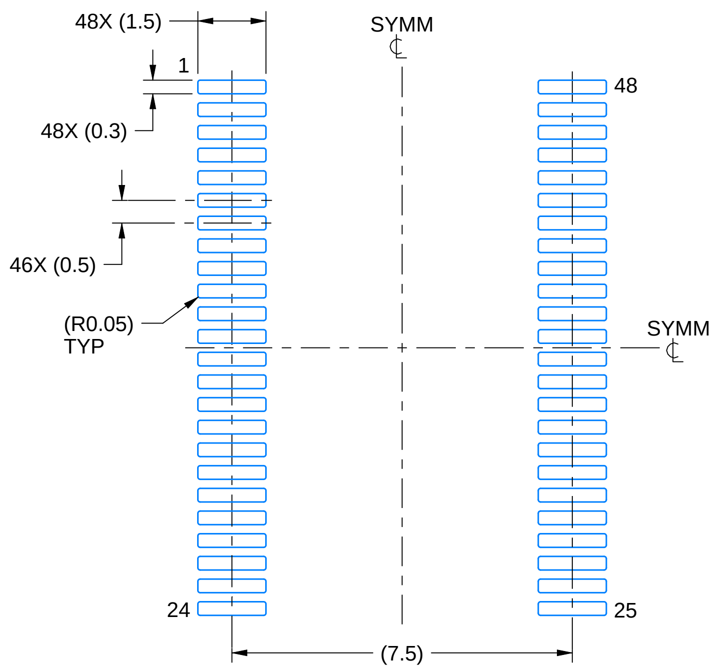
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

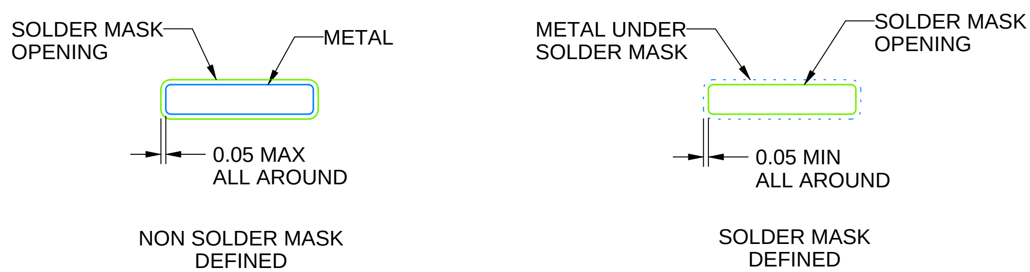


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

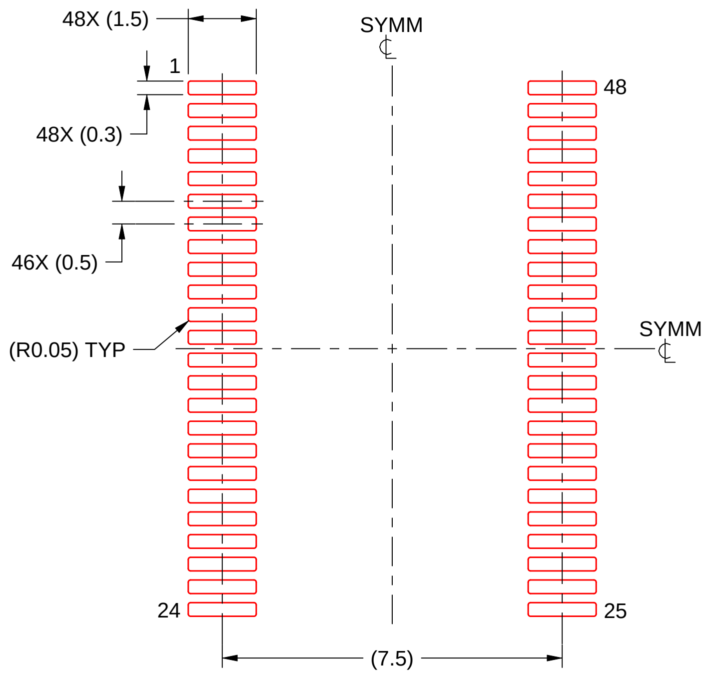


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

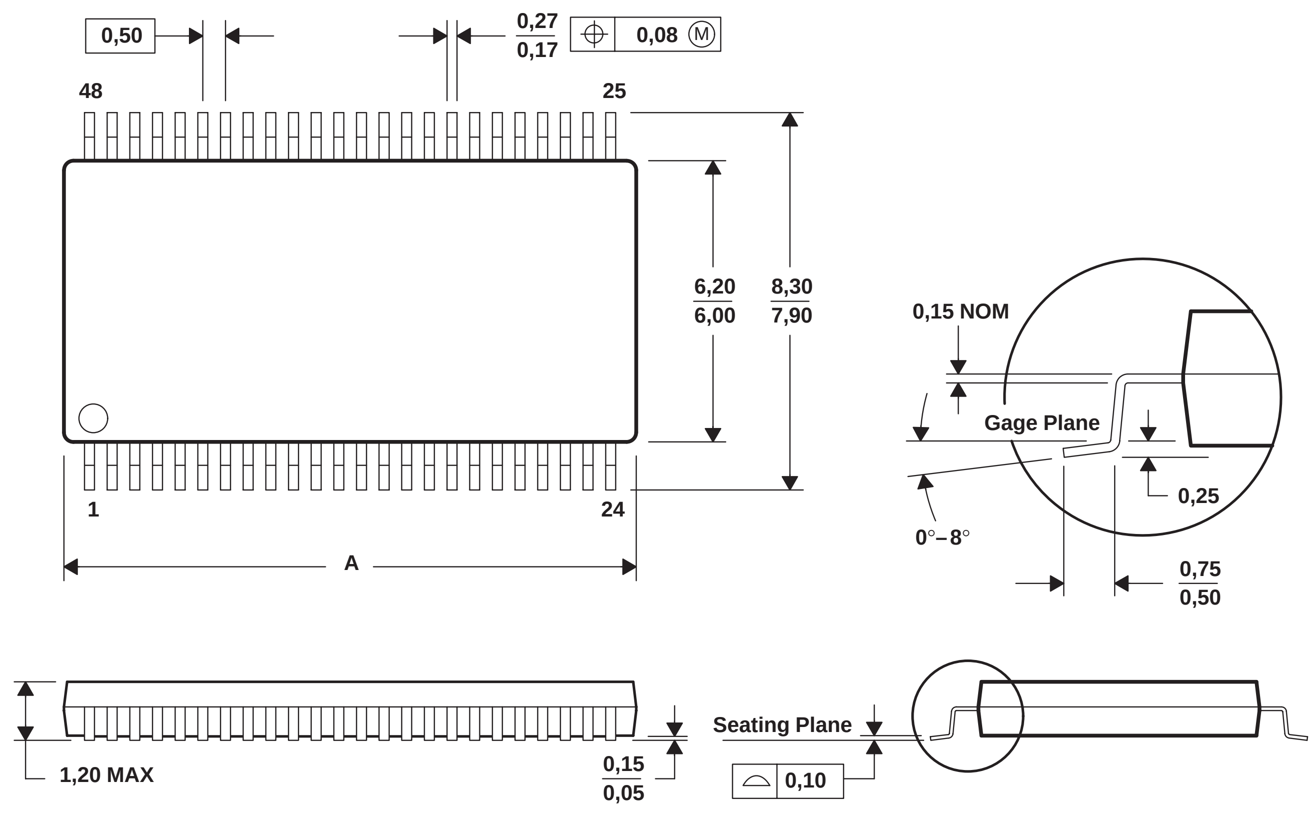
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153