

INA132 Low Power, Single-Supply Difference Amplifier

1 Features

- Wide supply range:
 - Single supply: 2.7V to 36V
 - Dual supplies: $\pm 1.35\text{V}$ to $\pm 18\text{V}$
- DC precision performance:
 - Low gain error: $\pm 0.075\%$ (maximum)
 - Low nonlinearity: 0.001% (maximum)
 - High common-mode rejection: 90dB (typical)
- Low quiescent current: 175 μA

2 Applications

- [Optical modules](#)
- [Building security gateways](#)
- [AC analog input module](#)
- [Mass spectrometer](#)
- [CPU \(PLC Controller\)](#)
- [Lab and field instrumentation](#)

3 Description

The INA132 is a low-power, unity-gain differential amplifier consisting of a precision op amp with a precision resistor network. The on-chip resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent TCR tracking of the resistors maintains gain accuracy and common-mode rejection over temperature. The internal op amp common-mode range extends to the negative supply—an excellent choice for single-supply applications. The INA132 operates on single (2.7V to 36V) or dual ($\pm 1.35\text{V}$ to $\pm 18\text{V}$) supplies.

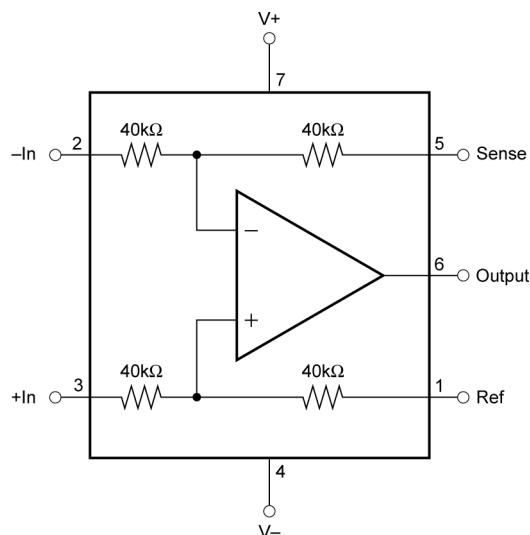
The differential amplifier is the foundation of many commonly used circuits. The INA132 provides this circuit function without using an expensive precision resistor network. The INA132 is available in an SO-8 surface-mount package and operates over the industrial temperature range of -40°C to $+85^{\circ}\text{C}$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
INA132	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see [Section 9](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Diagram



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4 Pin Configuration and Functions

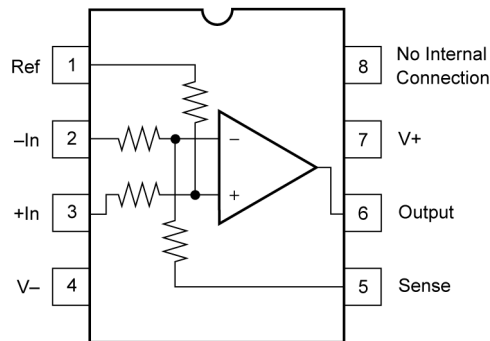


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
-In	2	Input	Negative (inverting) input
+In	3	Input	Positive (noninverting) input
No Internal Connection	8	—	No internal connection. Leave unconnected.
Output	6	Output	Output
Ref	1	—	Reference input. Drive this pin with a low impedance source. Interchanging pin 1 and 3 degrade CMR.
Sense	5	—	Sense input. Drive this pin with a low impedance source. Interchanging pin 2 and 5 degrade CMR.
V-	4	Input	Negative supply
V+	7	Input	Positive supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage	Dual supply, V _S = (V+) – (V–)		±18	V
		Single supply, V _S = (V+) – 0V		36	
	Input voltage range			±80	V
	Output short-circuit to (V _S / 2)		Continuous		
T _A	Operating temperature		–55	125	°C
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		–55	125	°C
	Lead temperature (soldering, 10s)			300	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±750	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _S	Supply voltage	Single-supply	2.7	36	V
		Dual-supply	±1.35	±18	
T _A	Specified temperature		–40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		INA132	UNIT
		D (SOIC)	
		8 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	150	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics: $V_S = \pm 15V$

at $T_A = 25^\circ C$, $V_S = \pm 15V$, $R_L = 10k\Omega$, $V_{REF} = 0V$, $V_{CM} = V_S/2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage ⁽¹⁾	RTO	INA132		± 75	± 250	μV
			INA132A		± 75	± 500	
	Offset voltage drift ⁽¹⁾	RTO, $T_A = -40^\circ C$ to $+85^\circ C$	INA132		± 1	± 5	$\mu V/^\circ C$
			INA132A		± 1	$\pm 10^{(4)}$	
	Long-term stability ⁽¹⁾				± 0.3		$\mu V/mo$
PSRR	Power-supply rejection ratio ⁽¹⁾	RTO, $V_S = \pm 1.35V$ to $\pm 18V$			± 5	± 30	$\mu V/V$
V_{CM}	Common-mode voltage	$V_O = 0V$		(V-)		$2(V+) - 2$	V
CMRR	Common-mode rejection	$V_{CM} = -15V$ to $+28V$, $R_S = 0\Omega$	INA132	76	90		dB
			INA132A	70	90		dB
	Differential input impedance ⁽²⁾				80		k Ω
	Common-mode input impedance ⁽²⁾				80		k Ω
NOISE							
e_N	Voltage noise ⁽³⁾	RTO, $f_B = 0.1Hz$ to $10Hz$			1.6		μV_{PP}
		RTO, $f = 1kHz$			75		nV/ \sqrt{Hz}
GAIN							
	Gain				1		V/V
GE	Gain error	$V_O = -14V$ to $+13.5V$		INA132	± 0.01	± 0.075	%
				INA132A	± 0.01	± 0.1	
	Gain error drift ⁽⁴⁾	$T_A = -40^\circ C$ to $+85^\circ C$			± 1	± 10	ppm/ $^\circ C$
	Gain nonlinearity	$V_O = -14V$ to $+13.5V$		INA132	± 0.0001	± 0.001	% of FSR
				INA132A	± 0.0001	± 0.002	
OUTPUT							
	Positive output voltage swing	$R_L = 100k\Omega$		(V+) - 1	(V+) - 0.8		V
		$R_L = 10k\Omega$		(V+) - 1.5	(V+) - 0.8		
	Negative output voltage swing	$R_L = 100k\Omega$		(V-) + 0.5	(V-) + 0.15		V
		$R_L = 10k\Omega$		(V-) + 1	(V-) + 0.25		
C_L	Load capacitance	Stable operation			10000		pF
I_{SC}	Short-circuit current	Continuous to $V_S / 2$			+6/-15		mA
FREQUENCY RESPONSE							
BW	Small signal bandwidth, -3dB				300		kHz
SR	Slew rate				0.1		V/ μs
t_s	Settling time	$V_O = 10V$ step	0.1%		85		μs
			0.01%		88		
	Overload recovery time	50% input overdrive			7		μs
POWER SUPPLY							
I_Q	Quiescent current	$V_{IN} = 0V$			± 175	± 230	μA

(1) Includes effects of amplifier input bias and offset currents.

(2) 40k Ω resistors are ratio matched but have $\pm 20\%$ absolute value.

(3) Includes effects of amplifier input current noise and thermal noise contribution of resistor network.

(4) Specified by wafer test to 95% confidence level.

5.6 Electrical Characteristics: $V_S = 5V$

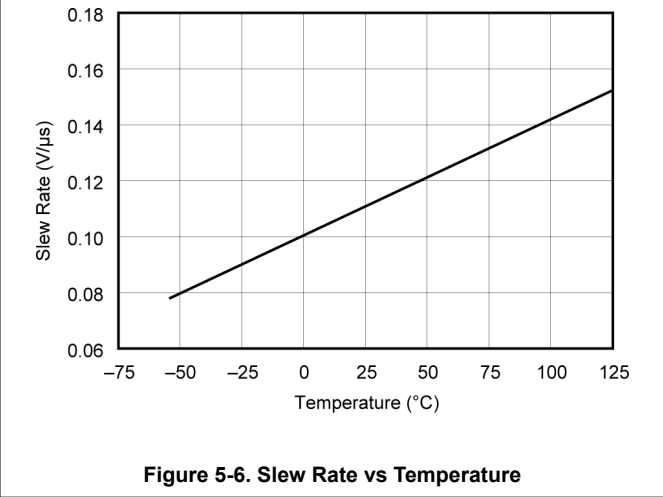
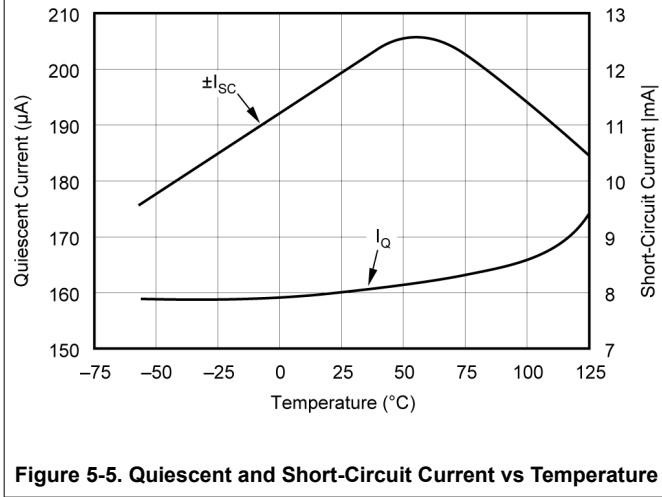
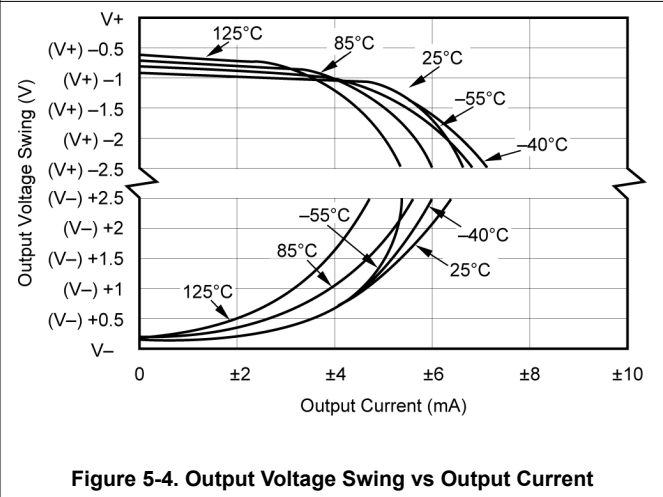
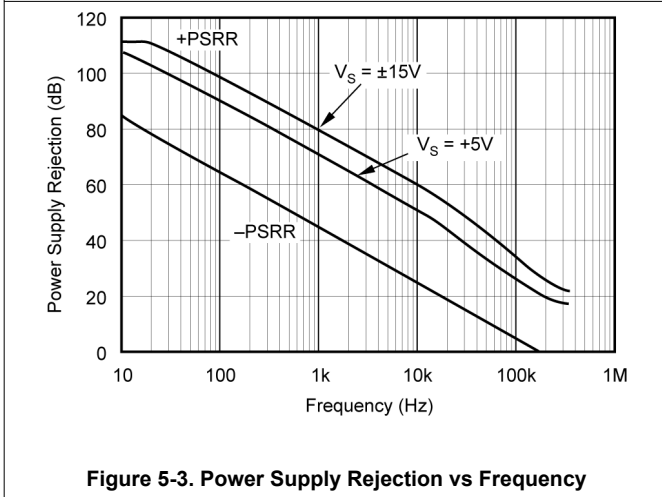
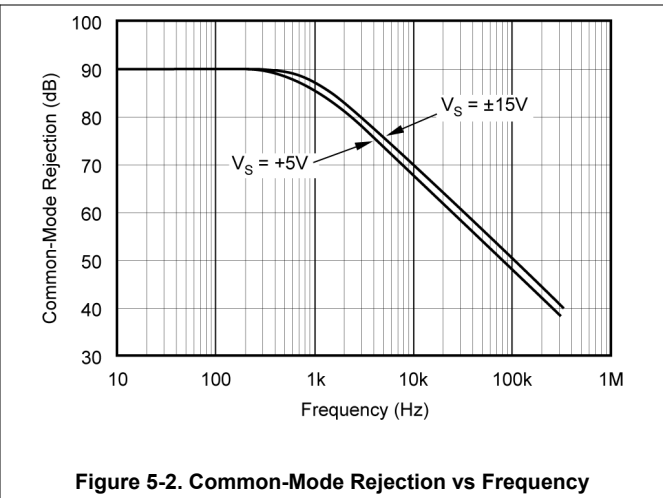
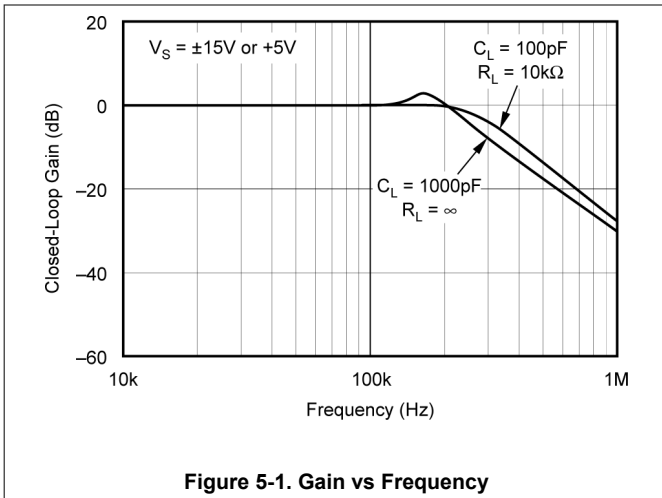
at $T_A = 25^\circ C$, $V_S = +5V$, $R_L = 10k\Omega$ connected to $V_S/2$, $V_{REF} = V_S/2$, $V_{CM} = V_S/2$, and $G = 1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage ⁽¹⁾	RTO	INA132		± 150	± 500	μV
			INA132A		± 150	± 750	
	Offset voltage drift ⁽¹⁾	RTO, $T_A = -40^\circ C$ to $+85^\circ C$			± 2		$\mu V/^\circ C$
V_{CM}	Common-mode voltage	$V_O = 0V$		(V-)		$2(V+) - 2$	V
CMRR	Common-mode rejection	$V_{CM} = 0V$ to $8V$, $R_S = 0\Omega$	INA132	76	90		dB
			INA132A	70	90		
OUTPUT							
	Positive output voltage swing	$R_L = 100k\Omega$		$(V+) - 1$	$(V+) - 0.75$		V
		$R_L = 10k\Omega$		$(V+) - 1$	$(V+) - 0.8$		
	Negative output voltage swing	$R_L = 100k\Omega$		$(V-) + 0.25$	$(V-) + 0.06$		V
		$R_L = 10k\Omega$		$(V-) + 0.25$	$(V-) + 0.12$		
POWER SUPPLY							
I_Q	Quiescent current	$V_{IN} = 0V$			± 175	± 230	μA

(1) Includes effects of amplifier input bias and offset currents.

5.7 Typical Characteristics

at $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$ (unless otherwise noted)



5.7 Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$ (unless otherwise noted)

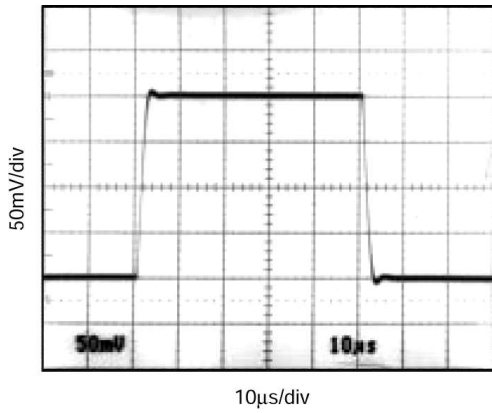


Figure 5-7. Small-Signal Step Response

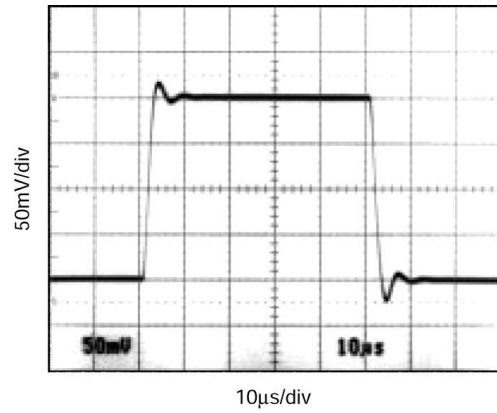


Figure 5-8. Small-Signal Step Response

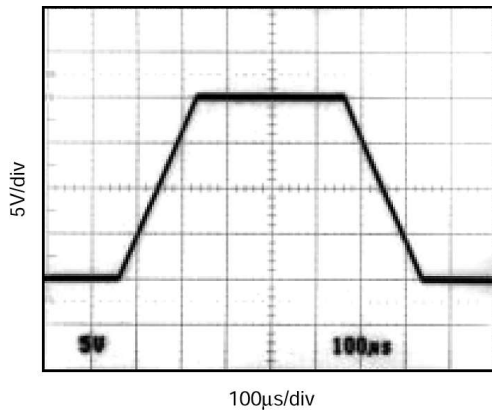


Figure 5-9. Large-Signal Step Response

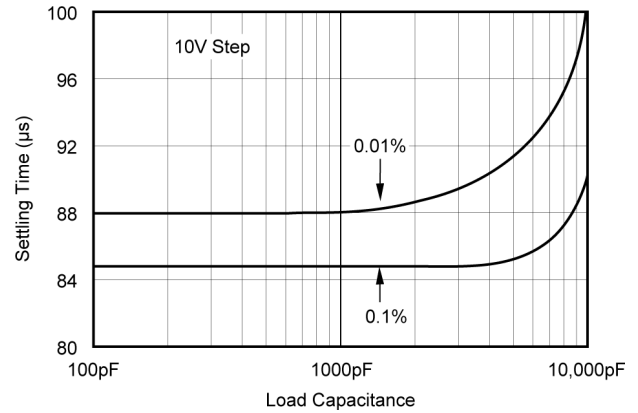


Figure 5-10. Settling Time vs Load Capacitance

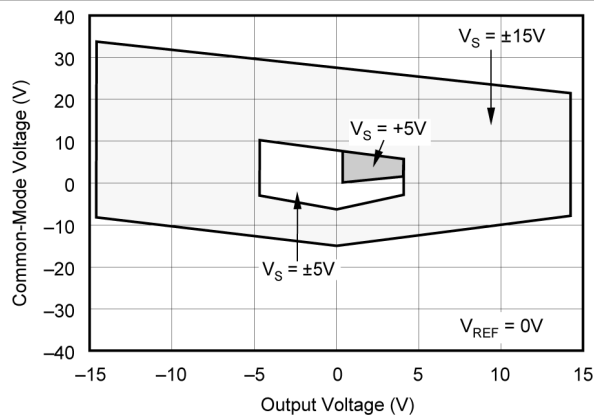


Figure 5-11. Input Common-mode Voltage Range vs Output Voltage

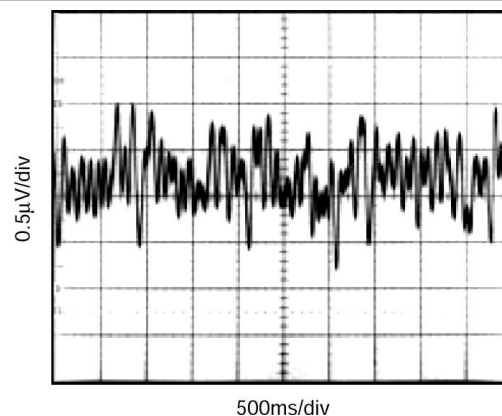


Figure 5-12. 0.1-Hz to 10-Hz Peak-to-Peak Voltage Noise

5.7 Typical Characteristics (continued)

at $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$ (unless otherwise noted)

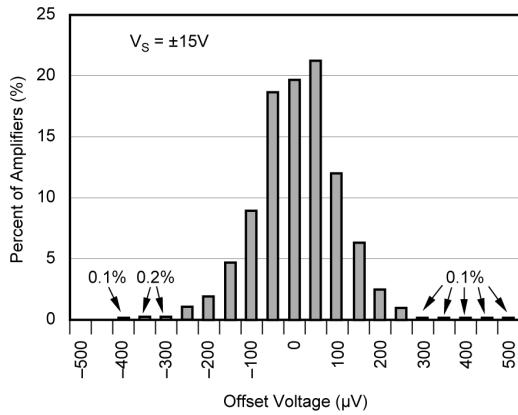


Figure 5-13. Offset Voltage Production Distribution

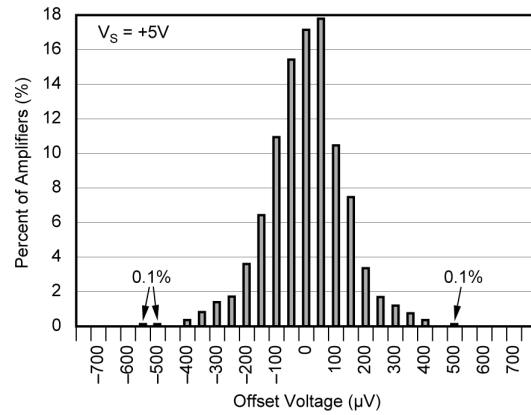


Figure 5-14. Offset Voltage Production Distribution

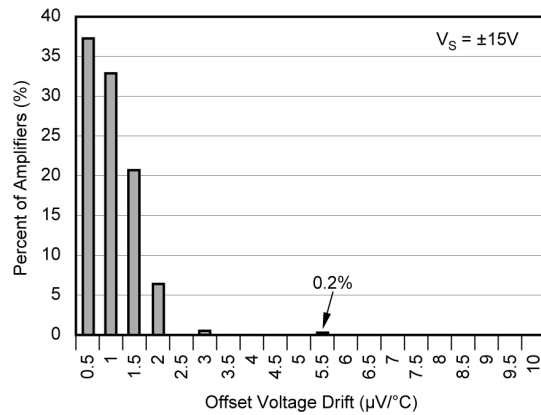


Figure 5-15. Offset Voltage Drift Production Distribution

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Applications Information

Figure 6-1 shows the basic connections required for operation of the INA132. Connect power-supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3 as shown. Ensure that the source impedances connected to the inputs are nearly equal to maintain good common-mode rejection. An 8Ω mismatch in source impedance degrades the common-mode rejection of a typical device to approximately 80dB. Gain accuracy is also slightly affected. If the source has a known impedance mismatch, use an additional resistor in series with one input to preserve good common-mode rejection.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR. Interchanging these pins does not provide specified performance. Sense measurements at the load, as in Figure 6-1.

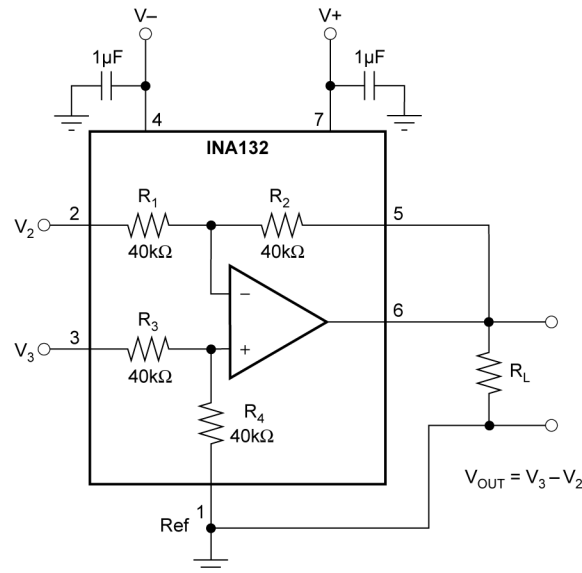


Figure 6-1. Basic Power Supply and Signal Connections

6.1.1 Operating Voltage

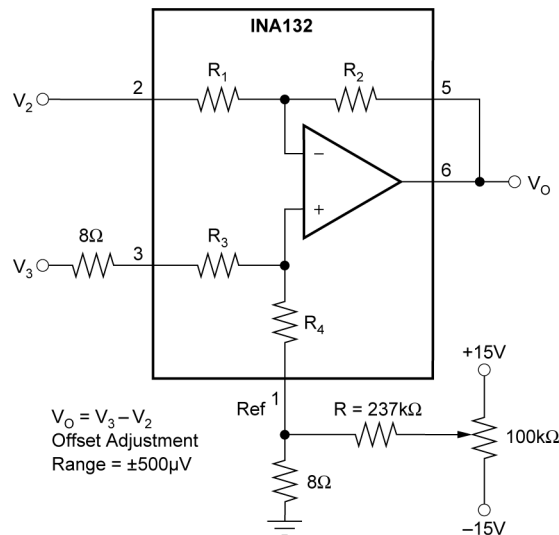
The INA132 operates from single (2.7V to 36V) or dual ($\pm 1.35V$ to $\pm 18V$) supplies with excellent performance. Specifications are production tested with +5V and $\pm 15V$ supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics*.

The internal op amp in the INA132 is a single-supply design. This design allows linear operation with the op-amp common-mode voltage equal to, or slightly below $V-$ (or single supply ground). Although input voltages on pins 2 and 3 that are less than the negative supply voltage do not damage the device, operation in this region is not recommended. Transient conditions at the inverting input terminal less than the negative supply can cause a positive feedback condition that can lock the INA132 output to the negative rail.

The INA132 can accurately measure differential signals that are greater than the positive power supply. The linear common-mode range extends to nearly twice the positive power supply voltage—see typical characteristics curve, *Common-Mode Range vs Output Voltage*.

6.1.2 Offset Voltage Trim

The INA132 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 6-2 shows an optional circuit for trimming the output offset voltage. The output is referred to the output reference terminal (pin 1), which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal, and can be used to null offset voltage. Ensure that the source impedance of a signal applied to the Ref terminal is less than 8Ω to maintain good common-mode rejection. To maintain low impedance at the Ref terminal, the trim voltage can be buffered with an op amp, such as the [OPA177](#).



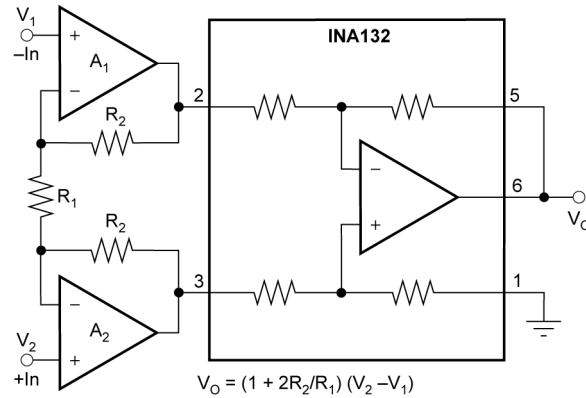
NOTE: For $\pm 750\mu\text{V}$ range, $R = 158\text{k}\Omega$.

Figure 6-2. Offset Adjustment.

6.1.3 Capacitive Load Drive Capability

The INA132 drives large capacitive loads, even at low supplies. The device is stable with a 10,000-pF load. See the *Small-Signal Step Response* and *Settling Time vs Load Capacitance* typical characteristics.

6.2 Typical Applications



The INA132 can be combined with op amps to form a complete instrumentation amplifier with specialized performance characteristics. Burr-Brown offers many complete high performance IAs. Products with related performances are shown at the right.

A ₁ , A ₂	FEATURE	SIMILAR COMPLETE BURR-BROWN IA
OPA27	Low Noise	INA103
OPA129	Ultra Low Bias Current (fA)	INA116
OPA177	Low Offset Drift, Low Noise	INA114, INA128
OPA2130	Low Power, FET-Input (pA)	INA111
OPA2234	Single Supply, Precision, Low Power	INA122 ⁽¹⁾ , INA118
OPA2237	Single Supply, Low Power, MSOP-8	INA122 ⁽¹⁾ , INA126 ⁽¹⁾

NOTE: (1) Available 1Q'97.

Figure 6-3. Precision Instrumentation Amplifier

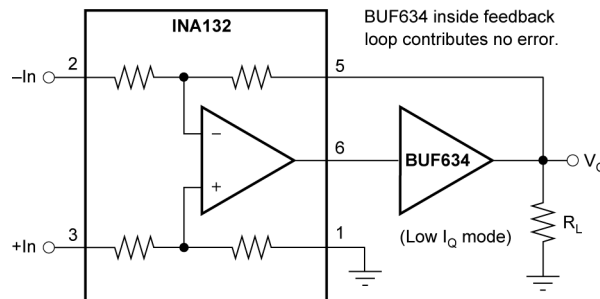


Figure 6-4. Low Power, High Output Current Precision Difference Amplifier

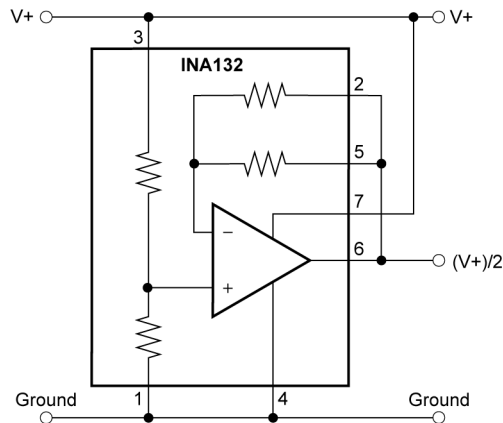


Figure 6-5. Pseudoground Generator

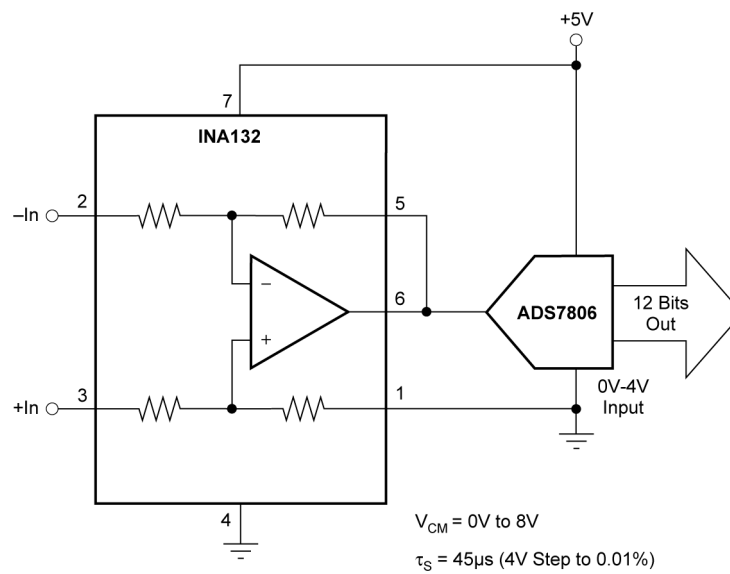


Figure 6-6. Differential Input Data Acquisition

Set $R_1 = R_2$

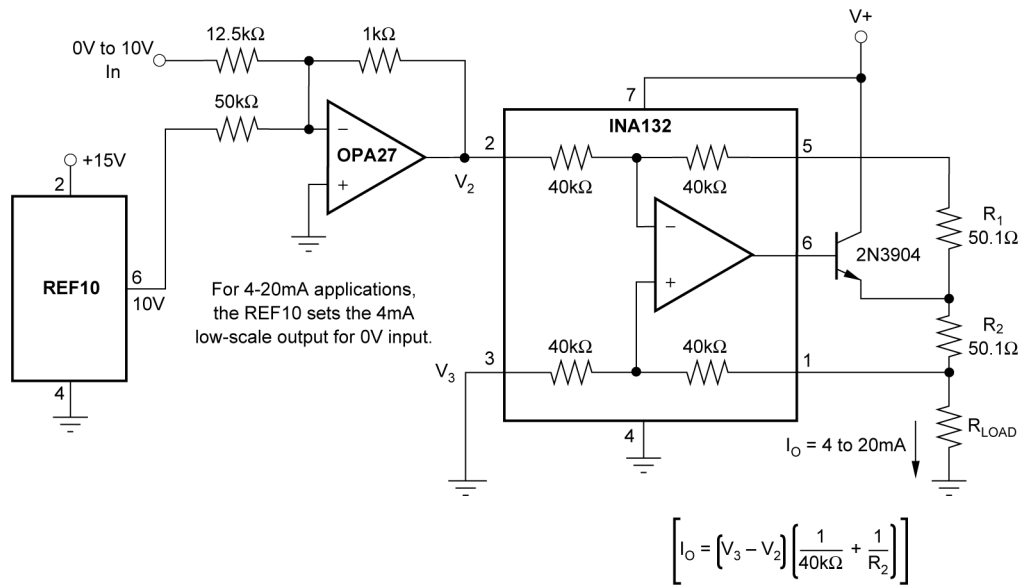


Figure 6-7. Precision Voltage-to-Current Conversion

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. See the [INA105](#) data sheet for additional applications ideas, including:

- Current receiver with compliance to rails
- Precision unity-gain inverting amplifier
- ± 10 -V precision voltage reference
- ± 5 -V precision voltage reference
- Precision unity-gain buffer
- Precision average value amplifier
- Precision $G = 2$ amplifier
- Precision summing amplifier
- Precision $G = 1/2$ amplifier
- Precision bipolar offsetting
- Precision summing amplifier with gain
- Instrumentation amplifier guard drive generator
- Precision summing instrumentation amplifier
- Precision absolute value buffer
- Precision voltage-to-current converter with differential inputs
- Differential input voltage-to-current converter for low I_{OUT}
- Isolating current source
- Differential output difference amplifier
- Isolating current source with buffering amplifier for greater accuracy
- Window comparator with window span and window center inputs
- Precision voltage-controlled current source with buffered differential inputs and gain
- Digitally controlled gain of ± 1 amplifier

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 1996) to Revision A (February 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>ESD Ratings, Recommended Operating Conditions, Thermal Information, Application and Implementation, Typical Applications, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections.....	1
• Deleted DIP package and associated content from data sheet.....	1
• Updated <i>Features</i> bullets.....	1
• Updated <i>Applications</i> bullets.....	1
• Added <i>Pin Functions</i> table.....	2
• Added dual supply specification to <i>Absolute Maximum Ratings</i>	3
• Changed output short-circuit from "ground" to " $V_S / 2$ " in <i>Absolute Maximum Ratings</i>	3
• Added $V_{REF} = 0V$, $V_{CM} = V_S / 2$, and $G = 1$ to test conditions in <i>Electrical Characteristics and Typical Characteristics</i> for clarity.....	4
• Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added $T_A = -40^\circ C$ to $+85^\circ C$ test condition for clarity.....	4
• Changed "Offset Voltage vs Time" to "Long-term stability" for clarity.....	4
• Changed "Offset Voltage vs Power Supply" to Power-supply rejection ratio for clarity.....	4
• Changed voltage noise typical value at 1kHz from $65nV/\sqrt{Hz}$ to $75nV/\sqrt{Hz}$	4
• Changed "Gain Error vs Temperature" to "Gain error drift" and added $T_A = -40^\circ C$ to $+85^\circ C$ test condition for clarity.....	4

- Changed "Voltage, Positive" to "Positive output voltage swing" and from "Voltage, Negative" to "Negative output voltage swing".....4
- Added test condition of "Continuous to $V_S / 2$ " to short-circuit current for clarity.....4
- Changed short-circuit current typical value from $\pm 12\text{mA}$ to $+6\text{mA}/-15\text{mA}$4
- Deleted power supply voltage range typical value of $\pm 15\text{V}$4
- Moved voltage range, operating temperature range, and thermal resistance from *Electrical Characteristics* to *Recommended Operating Conditions* and *Thermal Information*4
- Changed quiescent current typical value from $\pm 160\mu\text{A}$ to $\pm 175\mu\text{A}$ and maximum value from $\pm 185\mu\text{A}$ to $\pm 230\mu\text{A}$4
- Added $V_{\text{REF}} = V_S / 2$, $V_{\text{CM}} = V_S / 2$, and $G = 1$ to test conditions in *Electrical Characteristics: $V_S = 5\text{V}$* for clarity.....5
- Changed "Offset Voltage vs Temperature" to "Offset voltage drift" and added $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ test condition for clarity.....5
- Added (V-) to negative output voltage swing minimum and typical values.....5
- Deleted power supply voltage range typical value of $+5\text{V}$5
- Moved voltage range from *Electrical Characteristics: $V_S = 5\text{V}$* to *Recommended Operating Conditions*5
- Changed quiescent current typical value from $\pm 155\mu\text{A}$ to $\pm 175\mu\text{A}$ and maximum value from $\pm 185\mu\text{A}$ to $\pm 230\mu\text{A}$5

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA132U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI		INA 132U	
INA132U/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI NIPDAU	Level-3-260C-168 HR		INA 132U	Samples
INA132UA	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	INA 132U A	
INA132UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	INA 132U A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA132U/2K5	SOIC	D	8	2500	356.0	356.0	35.0
INA132UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA132U	D	SOIC	8	75	506.6	8	3940	4.32
INA132UA	D	SOIC	8	75	506.6	8	3940	4.32



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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