LM109QML 5-Volt Regulator

Check for Samples: LM109QML

FEATURES

- **Specified to be Compatible, Worst Case, with TTL and DTL**
- **Output Current in Excess of 1A**
- **Internal Thermal Overload Protection**
- **No External Components Required**

DESCRIPTION

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar PFM header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Connection Diagrams

Metal Can Packages

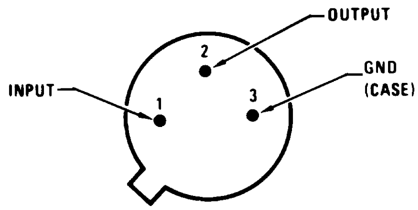


**Figure 1. 3-Pin PFM
Bottom View
See NDT003A Package**

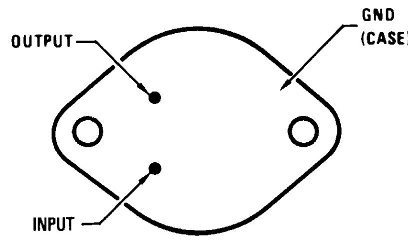
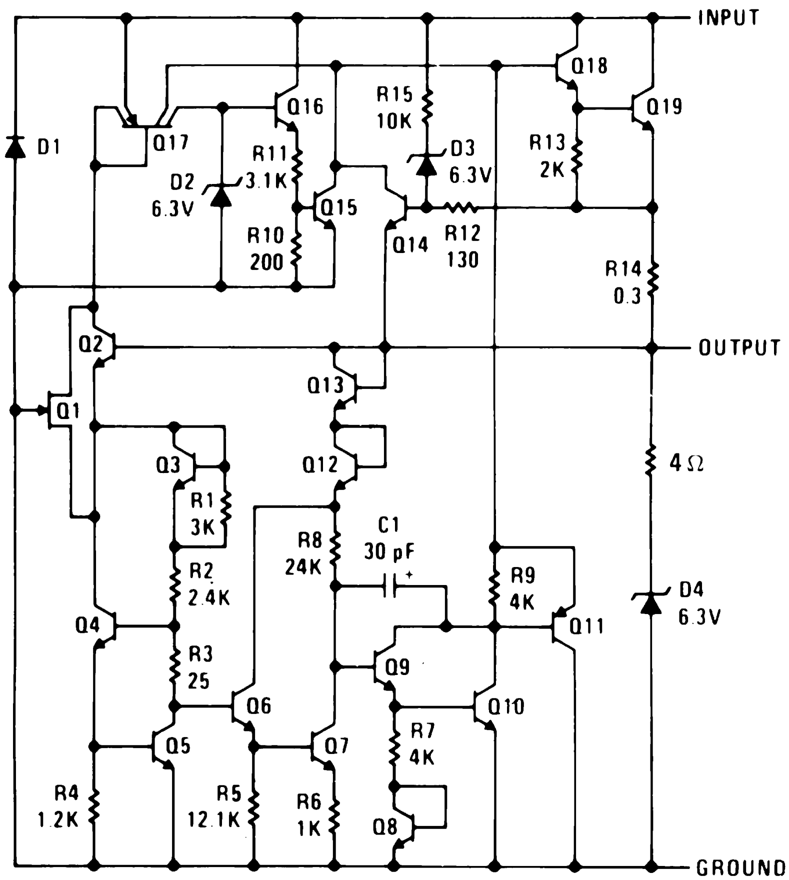


**Figure 2. 2-Pin TO
Bottom View
See K Package**

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1]

Input Voltage			35V
Power Dissipation			Internally Limited
Operating Ambient Temperature Range			$-55°C \le T_A \le +150°C$
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Maximum Junction Temperature			150°C
Thermal Resistance	θ_{JA}	PFM-Pkg (Still Air)	190°C/W
		PFM-Pkg (500LF/Min Air flow)	69°C/W
		TO-Pkg (Still Air)	39°C/W
		TO-Pkg (500LF/Min Air flow)	TBD
	θ_{JC}	PFM-Pkg	25°C/W
		TO-Pkg	3°C/W
Lead Temperature (Soldering, 10 sec.)			300°C
ESD Tolerance[2]			4000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Human body model, 1.5kΩ in series with 100pF.

Table 1. QUALITY CONFORMANCE INSPECTION

Mil-Std-883, Method 5005 - Group A		
Subgroup	**Description**	**Temp °C**
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM109H ELECTRICAL CHARACTERISTICS DC/AC PARAMETERS

The following conditions apply to all the following parameters, unless otherwise specified.
AC / DC: I_L = 5mA

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Start}	Start Up Input Voltage	$V_O \geq$ 4.706V, R_L = 25Ω	(1)		9.0	V	1
I_Q	Quiescent Current	V_I = 7V		-10		mA	1, 2, 3
		V_I = 7.2V, I_L = 500mA	(2)	-10		mA	1, 2, 3
		V_I = 25V		-10		mA	1, 2, 3
		V_I = 25V, I_L = 500mA	(2)	-10		mA	1, 2, 3
		V_I = 35V		-10		mA	1
Δ_{IQ}	Quiescent Current Change	7V ≤ V_I ≤ 25 V		-0.5	0.5	mA	1, 2, 3
		V_I = 7.2V, 5mA ≤ I_L ≤ 500mA	(2)	-0.8	0.8	mA	1, 2, 3
V_{RLine}	Line Regulation	7V ≤ V_I ≤ 25V		-50	50	mV	1
				-100	100	mV	2, 3
V_{RLoad}	Load Regulation	V_I = 7.2V, 5mA ≤ I_L ≤ 500mA		-50	50	mV	1
			(2)	-100	100	mV	2, 3
		V_I = 10V, 5mA ≤ I_L ≤ 500mA		-50	50	mV	1
			(2)	-100	100	mV	2, 3
		V_I = 25V, 20mA ≤ I_L ≤ 500mA		-150	150	mV	1
		V_I = 25V, t_{PW} ≤ 10ms, 500mA ≥ I_L ≥ 20mA,	(2)	-50	50	mV	1
V_O	Output Voltage	V_I = 7V, P_1 ≤ 2W		4.6	5.4	V	1, 2, 3
		V_I = 7.2V, I_L = 500mA, P ≤ 2W	(2)	4.6	5.4	V	1, 2, 3
		V_I = 10V, I_L = 100mA, P ≤ 2W		4.7	5.3	V	1
		V_I = 25V, I_L = 20mA, P ≤ 2W		4.6	5.4	V	1
		V_I = 25V, I_L = 500mA, P ≤ 2W, t_{PW} ≤ 10mS	(2)	4.6	5.4	V	1, 2, 3
		V_I = 25V, P ≤ 2W		4.6	5.4	V	1, 2, 3
I_{OS}	Short Circuit Current	V_I = 35V			2.0	A	1
RR	Ripple Rejection *ƒ*	*ƒ* ≤ 120Hz, e_I = 1V_{RMS}, I_L = 125mA		50		dB	4

(1) This test is performed by shifting the input voltage in 50mV increments until output reaches 4.706V.
(2) At −55°C & 125°C, I_L = 200mA rather than 500mA.

LM109K ELECTRICAL CHARACTERISTICS DC/AC PARAMETERS

The following conditions apply to all the following parameters, unless otherwise specified.
AC / DC: I_L = 5mA[(1)]

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Start}	Start Up Input Voltage	V_O ≥ 4.706V, R_L = 5Ω	(2)		9.0	V	1
I_Q	Quiescent Current	V_I = 7V		-10		mA	1, 2, 3
		V_I = 7.2V, I_L = 1.5A	(3)	-10		mA	1, 2, 3
		V_I = 25V		-10		mA	1, 2, 3
		V_I = 25V, I_L = 1.5A t_{PW} ≤ 10ms	(3)	-10		mA	1, 2, 3
		V_I = 35V		-10		mA	1
Δ_{IQ}	Quiescent Current Change	7V ≤ V_I ≤ 25 V		-0.5	0.5	mA	1, 2, 3
		V_I = 7.2V, 5mA ≤ I_L ≤ 1.5A	(3)	-0.8	0.8	mA	1, 2, 3
V_{RLine}	Line Regulation	7V ≤ V_I ≤ 25V		-50	50	mV	1
				-100	100	mV	2, 3
V_{RLoad}	Load Regulation	V_I = 7.2V, 5mA ≤ I_L ≤ 1.5A		-100	100	mV	1
			(3)	-200	200	mV	2, 3
		V_I = 10V, 1.5A ≥ I_L ≥ 5mA		-100	100	mV	1
			(3)	-200	200	mV	2, 3
		V_I = 25V, t_{PW} < 10ms, 1A ≥ I_L ≥ 20mA,		-50	50	mV	1
V_O	Output Voltage	V_I = 7V, P_1 ≤ 20W		4.6	5.4	V	1, 2, 3
		V_I = 7.2V, I_L = 1.5A, P ≤ 20W	(3)	4.6	5.4	V	1, 2, 3
		V_I = 10V, I_L = 500mA, P ≤ 20W		4.7	5.3	V	1
		V_I = 25V, I_L = 20mA, P ≤ 20W		4.6	5.4	V	1
		V_I = 25V, I_L = 1A, P ≤ 20W, t_{PW} ≤ 10mS		4.6	5.4	V	1, 2, 3
		V_I = 25V, P ≤ 20W		4.6	5.4	V	1, 2, 3
I_{OS}	Short Circuit Current	V_I = 35V			2.8	A	1
RR	Ripple Rejection	f ≤ 120Hz, e_I = 1V_{RMS}, I_L = 500mA		50		dB	4

(1) Human body model, 1.5kΩ in series with 100_PF.
(2) This test is performed by shifting the input voltage in 50mV increments until output reaches 4.706V.
(3) At −55°C & 125°C, I_L = 1A rather than 1.5A.

LM109K ELECTRICAL CHARACTERISTICS DC PARAMETERS

The following conditions apply to all the following parameters, unless otherwise specified.
DC: I_L = 5mA[(1)]

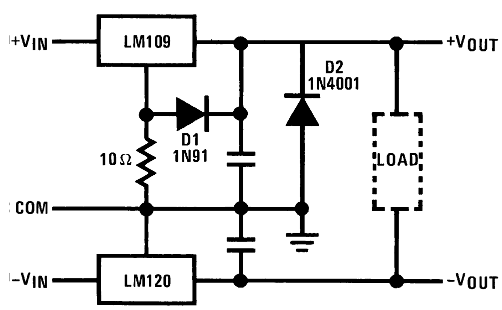
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_N	Output Noise Voltage	10Hz ≤ f ≤ 100KHz	(2)		200	µV	7
ΔV_O / ΔT	Long Term Stability		(2)		10	mV	8

(1) Human body model, 1.5kΩ in series with 100_PF.
(2) Specified parameter, not tested.

APPLICATION HINTS

1. **Bypass the input** of the LM109 to ground with ≥ 0.2 µF ceramic or solid tantalum capacitor if main filter capacitor is more than 4 inches away.
2. **Avoid insertion of regulator into “live” socket** if input voltage is greater than 10V. The output will rise to within 2V of the unregulated input if the ground pin does not make contact, possibly damaging the load. The LM109 may also be damaged if a large output capacitor is charged up, then discharged through the internal clamp zener when the ground pin makes contact.
3. **The output clamp zener** is designed to absorb transients only. It will not clamp the output effectively if a failure occurs in the internal power transistor structure. Zener dynamic impedance is ≈ 4Ω. Continuous RMS current into the zener should not exceed 0.5A.
4. **Paralleling of LM109s** for higher output current is not recommended. Current sharing will be almost nonexistent, leading to a current limit mode operation for devices with the highest initial output voltage. The current limit devices may also heat up to the thermal shutdown point (≈ 175°C). Long term reliability cannot be specified under these conditions.
5. **Preventing latchoff** for loads connected to negative voltage:

If the output of the LM109 is pulled negative by a high current supply so that the output pin is more than 0.5V negative with respect to the ground pin, the LM109 can latch off. This can be prevented by clamping the ground pin to the output pin with a germanium or Schottky diode as shown. A silicon diode (1N4001) at the output is also needed to keep the positive output from being pulled too far negative. The 10Ω resistor will raise $+V_{OUT}$ by ≈ 0.05V.



Crowbar Overvoltage Protection

Figure 3. Input Crowbar

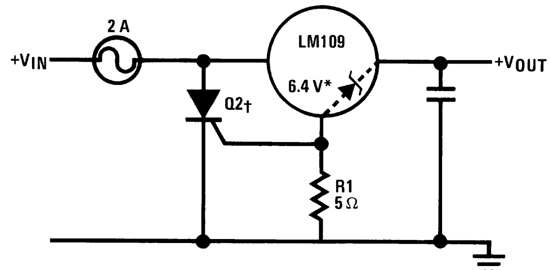
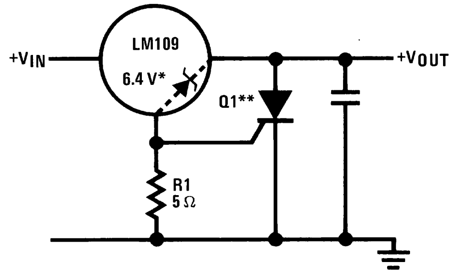


Figure 4. Output Crowbar



*Zener is internal to LM109.
**Q1 must be able to withstand 7A continuous current if fusing is not used at regulator input. LM109 bond wires will fuse at currents above 7A.
†Q2 is selected for surge capability. Consideration must be given to filter capacitor size, transformer impedance, and fuse blowing time.
††Trip point is ≈ 7.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Average Power Dissipation (LM109K)

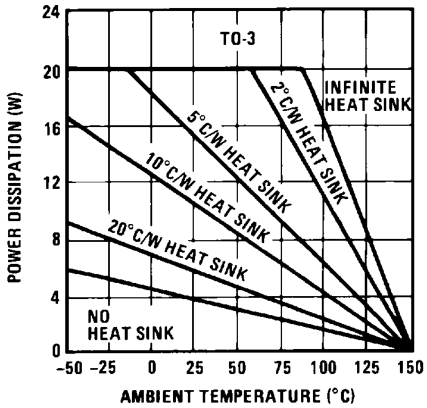


Figure 5.

Output Impedance

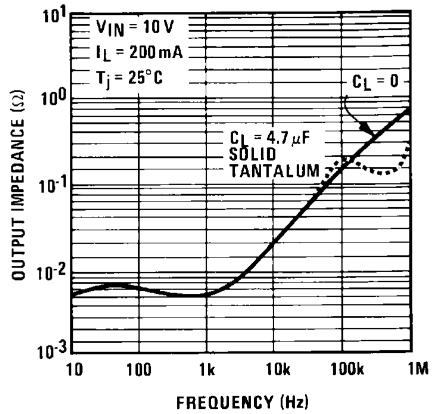


Figure 6.

Maximum Average Power Dissipation (LM109H)

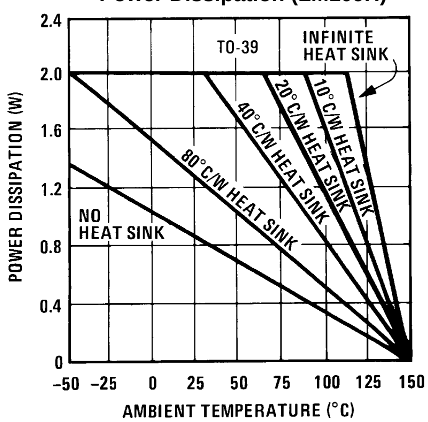


Figure 7.

Ripple Rejection

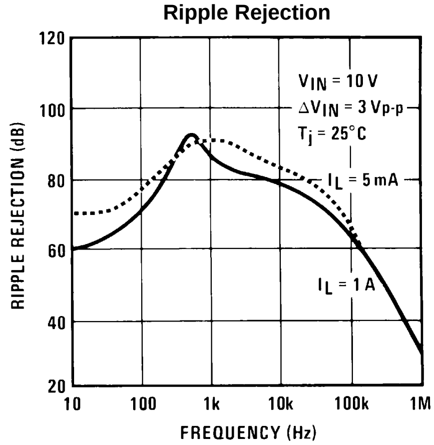
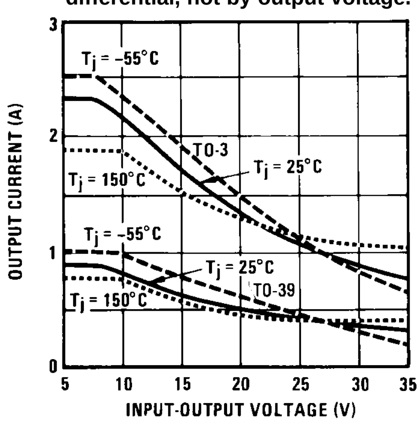


Figure 8.

Current Limit Characteristics docato-extra-info-title Current limiting foldback characteristics are determined by input output differential, not by output voltage.



Current limiting foldback characteristics are determined by input output differential, not by output voltage.

Figure 9.

Thermally Induced Output Voltage Variation

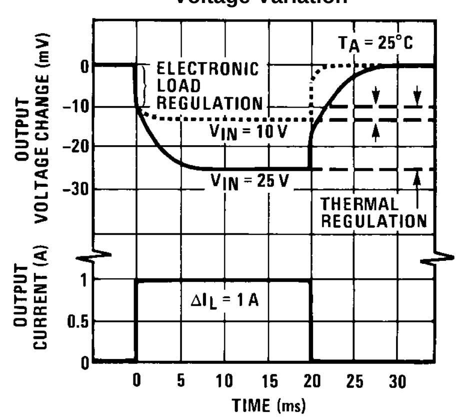


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Ripple Rejection

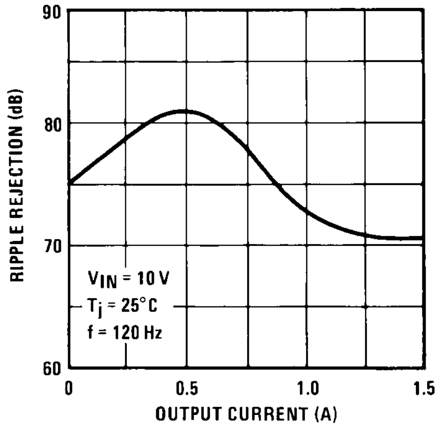


Figure 11.

Input-Output Differential (V)

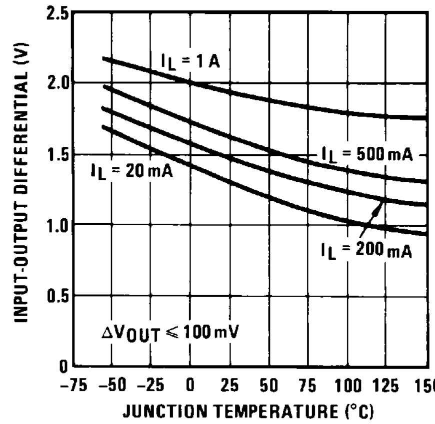


Figure 12.

Output Voltage (V)

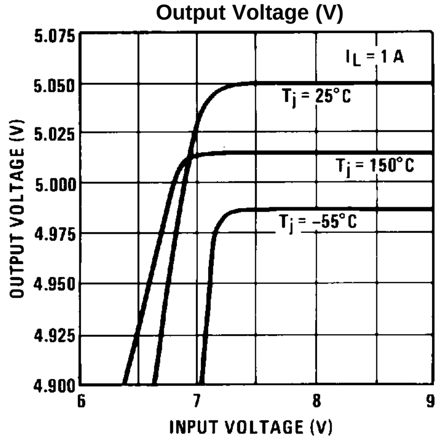


Figure 13.

Output Voltage (V)

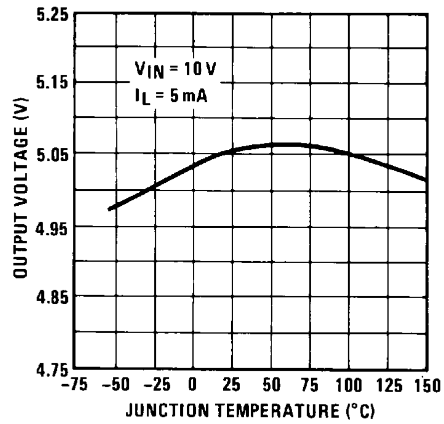


Figure 14.

Quiescent Current

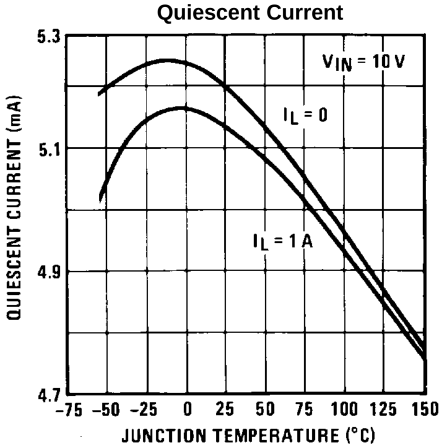


Figure 15.

Quiescent Current

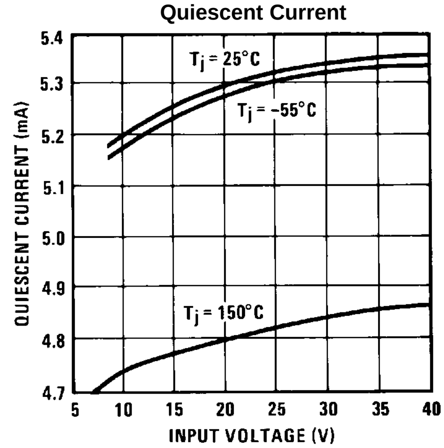


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Voltage Noise

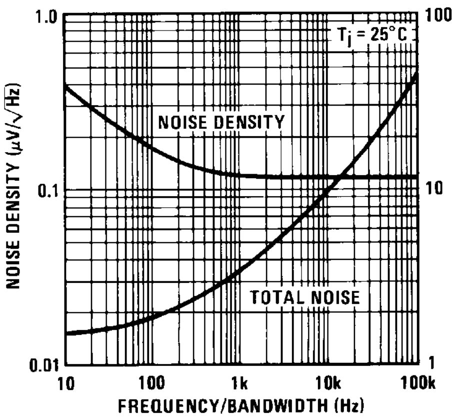


Figure 17.

Line Transient Response

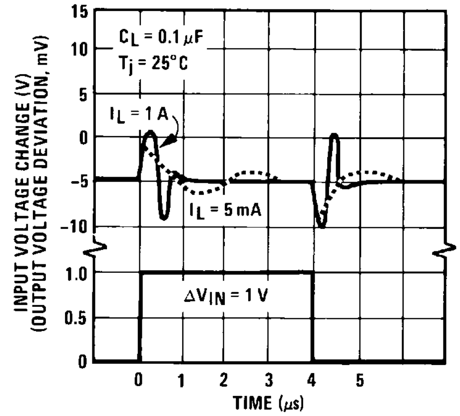


Figure 18.

Load Transient Response

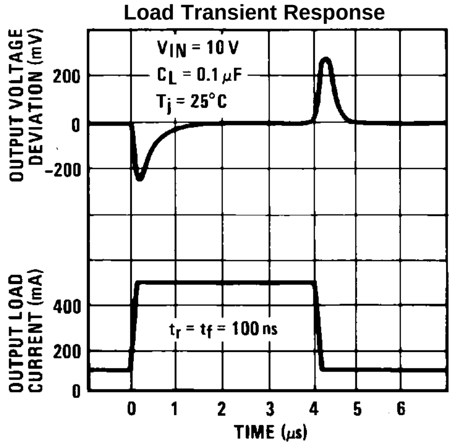
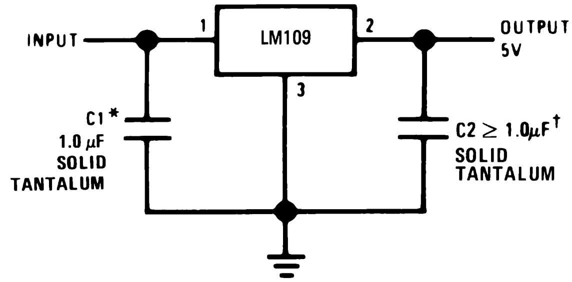


Figure 19.

TYPICAL APPLICATIONS

Figure 20. Fixed 5V Regulator



*Required if regulator is located more than 4″ from power supply filter capacitor.
†Although no output capacitor is needed for stability, it does improve transient response.
C2 should be used whenever long wires are used to connect to the load, or when transient response is critical.
Note: Pin 3 electrically connected to case.

Figure 21. Adjustable Output Regulator

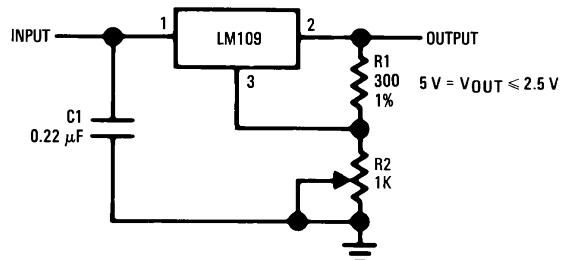
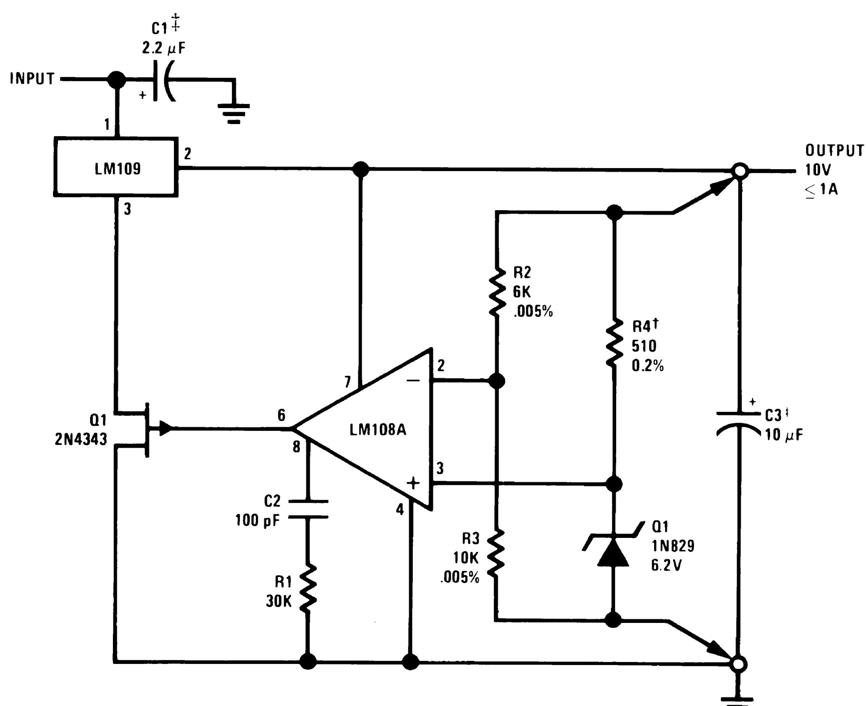
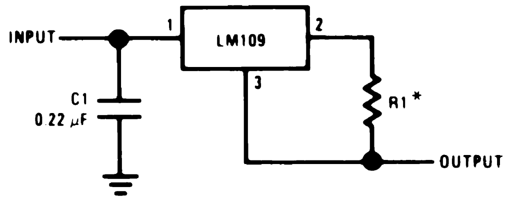


Figure 22. High Stability Regulator*



*Regulation better than 0.01%, load, line and temperature, can be obtained.
†Determines zener current. May be adjusted to minimize thermal drift.
‡Solid tantalum.

Figure 23. Current Regulator



*Determines output current. If wirewound resistor is used, bypass with 0.1 μF.

REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
11/08/05	A	New release to corporate format	L. Lytle	2 MDS datasheets converted into one datasheet in the corporate format. Deleted note 5 & corrected V_{RLoad} of LM109K to ≥ . MNLM109-K Rev 0AL & MNLM109-H Rev 0AL will be archived.
4/22/2013	A	All		Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM109K/883	OBSOLETE	TO	K	2		TBD	Call TI	Call TI		LM109K /883 Q ACO /883 Q >T	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

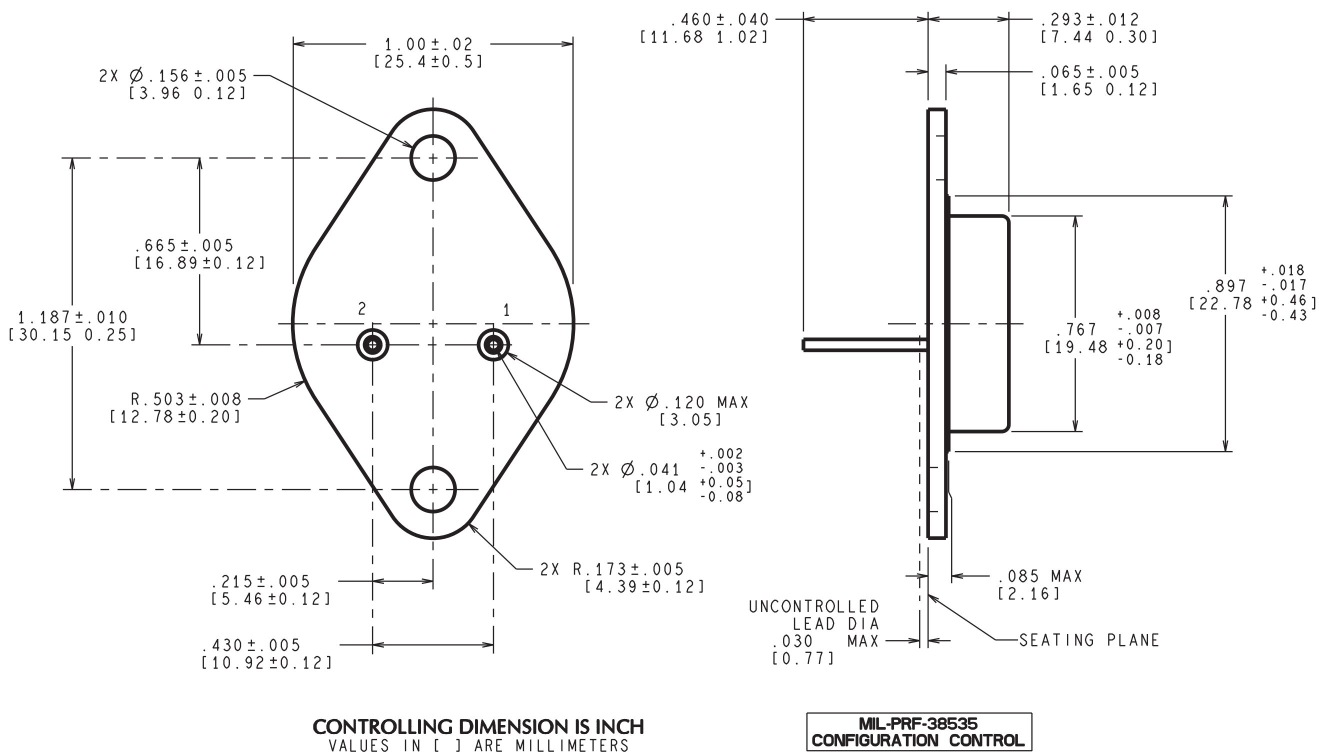
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

K0002C



K02C (Rev E)

4214774/A 03/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. Leads not to be bent greater than 15º

IMPORTANT NOTICE AND DISCLAIMER