LM140K 3-Terminal Positive Regulator

Check for Samples: LM140K

FEATURES

- Complete Specifications at 1A Load
- Output Voltage Tolerances of ±4% at T_j = 25°C
- Internal Thermal Overload Protection
- Internal Short-circuit Current Limit
- Output Transistor Safe Area Protection
- P^+ Product Enhancement Tested

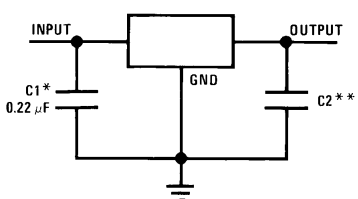
DESCRIPTION

The LM140K monolithic 3-terminal positive voltage regulator employs internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

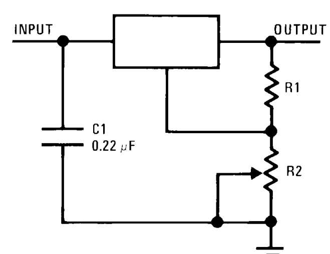
The LM140K is available in 5V, 12V and 15V options in the steel TO-3 power package.

Typical Applications



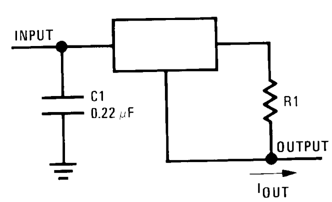
*Required if the regulator is located far from the power supply filter.
**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

Figure 1. Fixed Output Regulator



V_{OUT} = 5V + (5V/R1 + I_Q) R2 5V/R1 > 3 I_Q, load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM140K-5.0).

Figure 2. Adjustable Output Regulator



$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes.

Figure 3. Current Regulator

Connection Diagrams

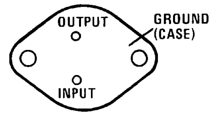


Figure 4. TO-3 Metal Can (Bottom View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

DC Input Voltage		35V
Internal Power Dissipation(4)		Internally Limited
Maximum Junction Temperature		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	TO-3 Package (NDS)	300°C
ESD Susceptibility(5)		2 kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the Electrical Characteristics.
(2) Specifications and availability for military grade LM140H/883 and LM140K/883 can be found in the LM140QML datasheet (SNVS382). Specifications and availability for military and space grade LM140H/JAN and LM140K/JAN can be found in the LM140JAN datasheet (SNVS399).
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) The maximum allowable power dissipation at any ambient temperature is a function of the maximum junction temperature for operation (T_{JMAX} = 125°C or 150°C), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above T_{JMAX} and the electrical specifications do not apply. If the die temperature rises above 150°C, the device will go into thermal shutdown. For the TO-3 package (NDS), the junction-to-ambient thermal resistance (θ_{JA}) is 39°C/W. When using a heatsink, θ_{JA} is the sum of the 4°C/W junction-to-case thermal resistance (θ_{JC}) of the TO-3 package and the case-to-ambient thermal resistance of the heatsink.
(5) ESD rating is based on the human body model, 100 pF discharged through 1.5 kΩ.

Operating Conditions(1)

Temperature Range (T_A)(2)	LM140	−55°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Conditions are conditions under which the device functions but the specifications might not be ensured. For ensured specifications and test conditions see the Electrical Characteristics.
(2) The maximum allowable power dissipation at any ambient temperature is a function of the maximum junction temperature for operation (T_{JMAX} = 125°C or 150°C), the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A). $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above T_{JMAX} and the electrical specifications do not apply. If the die temperature rises above 150°C, the device will go into thermal shutdown. For the TO-3 package (NDS), the junction-to-ambient thermal resistance (θ_{JA}) is 39°C/W. When using a heatsink, θ_{JA} is the sum of the 4°C/W junction-to-case thermal resistance (θ_{JC}) of the TO-3 package and the case-to-ambient thermal resistance of the heatsink.

LM140 Electrical Characteristics

55°C ≤ T_J ≤ + 150°C unless otherwise specified[(1)]

Symbol	Output Voltage		5V			12V			15V			Units
	Input Voltage (unless otherwise noted)		10V			19V			23V			
	Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
V_O	Output Voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1A	4.9	5	5.1	11.75	12	12.25	14.7	15	15.3	V
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A	4.8		5.2	11.5		12.5	14.4		15.6	V
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
ΔV_O	Line Regulation	I_O = 500 mA			10			18			22	mV
		T_J = 25°C, ΔV_{IN}, −55°C ≤ T_J ≤ +150°C		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		T_J = 25°C		3	10		4	18		4	22	mV
		ΔV_{IN}, −55°C ≤ T_J ≤ +150°C		(7.5 ≤ V_{IN} ≤ 20)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)		V
		T_J = 25°C			4			9			10	mV
		Over Temperature			12			30			30	mV
		ΔV_{IN}		(8 ≤ V_{IN} ≤ 12)			(16 ≤ V_{IN} ≤ 22)			(20 ≤ V_{IN} ≤ 26)		V
ΔV_O	Load Regulation	T_J = 25°C, 5 mA ≤ I_O ≤ 1.5A		10	25		12	32		12	35	mV
		T_J = 25°C, 250 mA ≤ I_O ≤ 750 mA			15			19			21	mV
		Over Temperature, 5 mA ≤ I_O ≤ 1A			25			60			75	mV
I_Q	Quiescent Current	T_J = 25°C			6			6			6	mA
		Over Temperature			6.5			6.5			6.5	mA
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A		0.5			0.5			0.5		mA
		T_J = 25°C, I_O = 1A			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(7.5 ≤ V_{IN} ≤ 20)			(14.8 ≤ V_{IN} ≤ 27)			(17.9 ≤ V_{IN} ≤ 30)		V
		I_O = 500 mA			0.8			0.8			0.8	mA
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 25)			(15 ≤ V_{IN} ≤ 30)			(17.9 ≤ V_{IN} ≤ 30)		V
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40			75			90		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	T_J = 25°C, f = 120 Hz, I_O = 1A	68	80		61	72		60	70		dB
		or f = 120 Hz, I_O = 500 mA,	68			61			60			dB
		Over Temperature,										
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}		(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		V
R_O	Dropout Voltage	T_J = 25°C, I_O = 1A		2.0			2.0			2.0		V
	Output Resistance	f = 1 kHz		8			18			19		mΩ
	Short-Circuit Current	T_J = 25°C		2.1			1.5			1.2		A
	Peak Output Current	T_J = 25°C		2.4			2.4			2.4		A
	Average TC of V_O	Min, T_J = 0°C, I_O = 5 mA		−0.6			−1.5			−1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_J = 25°C	7.5			14.5			17.5			V

(1) All characteristics are measured with a 0.22 µF capacitor from input to ground and a 0.1 µF capacitor from output to ground. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

Maximum Average Power Dissipation

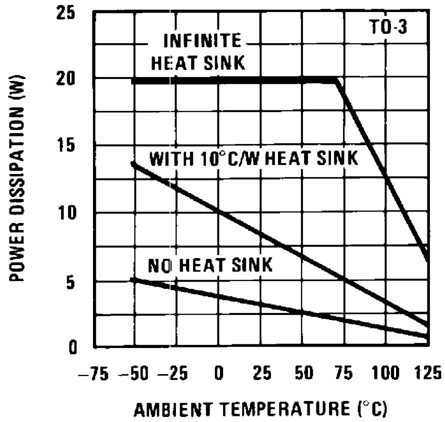


Figure 5.

Output Voltage (Normalized to 1V at T_J = 25°C)

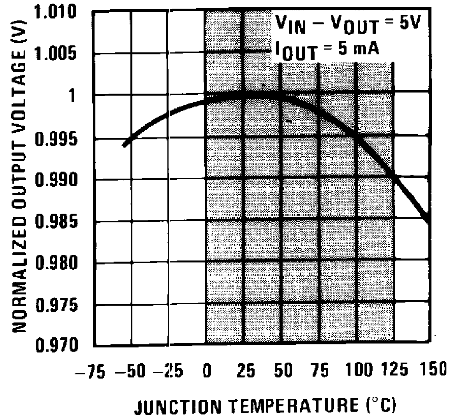


Figure 6.

Ripple Rejection

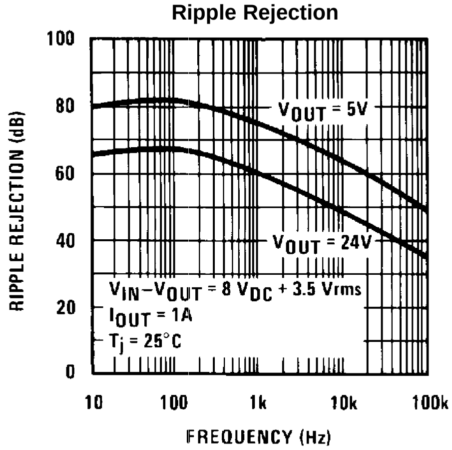


Figure 7.

Ripple Rejection

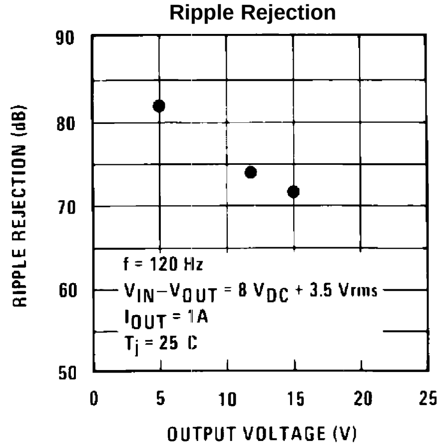


Figure 8.

Output Impedance

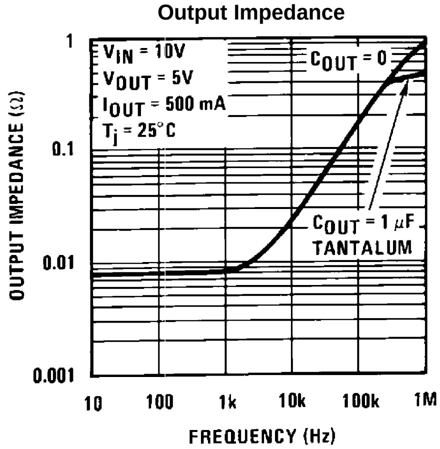


Figure 9.

Dropout Characteristics

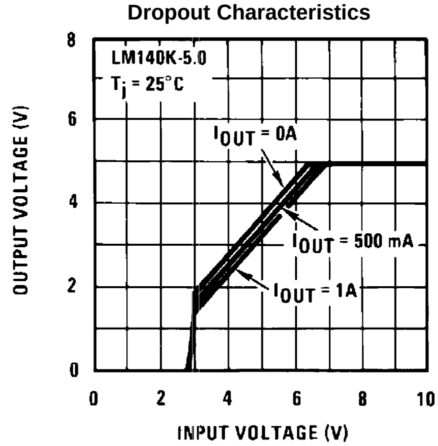


Figure 10.

Typical Performance Characteristics (continued)

Quiescent Current

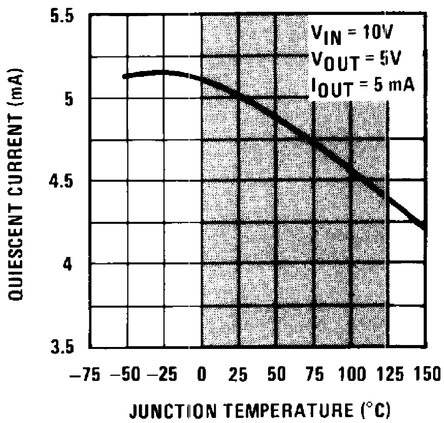


Figure 11.

Peak Output Current

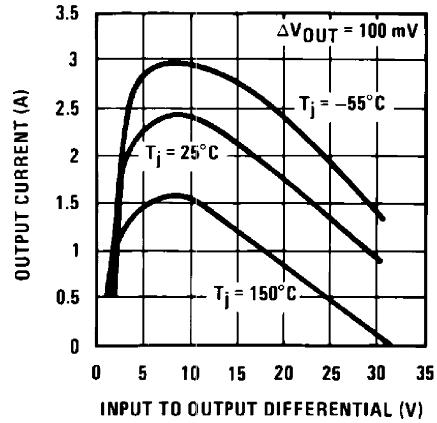


Figure 12.

Dropout Voltage

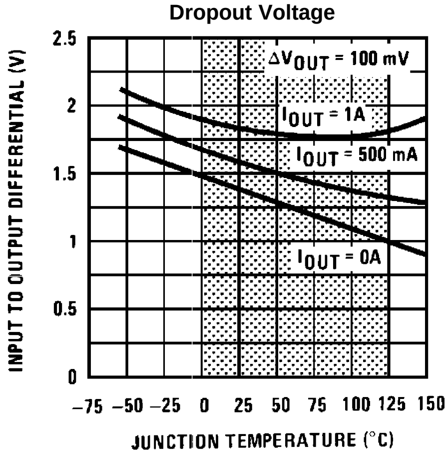


Figure 13.

Quiescent Current

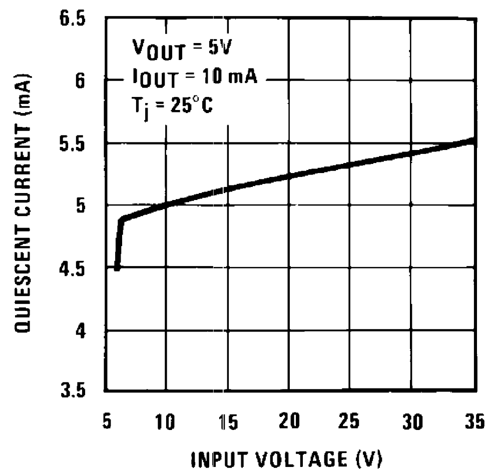


Figure 14.

Line Regulation
140K, I_{OUT} = 1A, T_A = 25°C

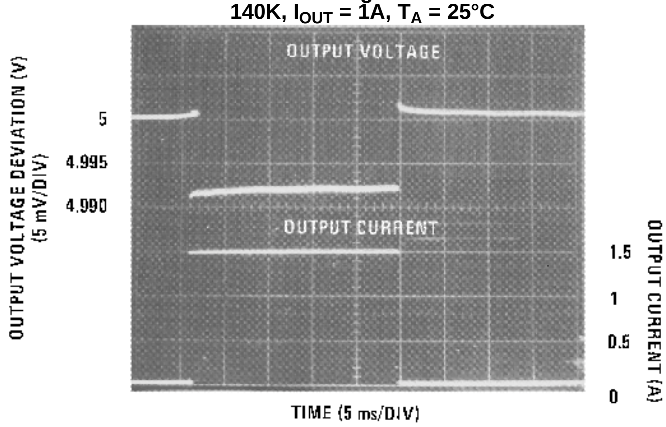


Figure 15.

Line Regulation
140K, V_{IN} = 10V, T_A = 25°C

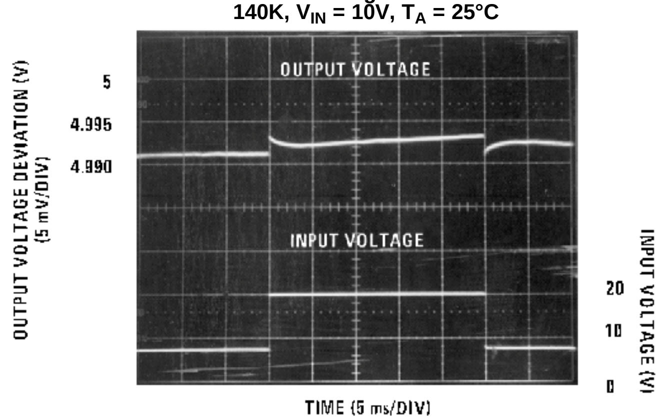
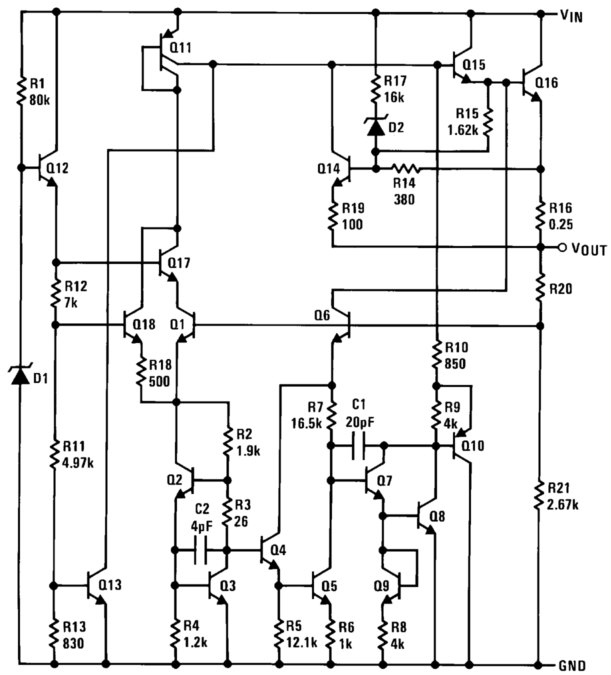


Figure 16.

Equivalent Schematic



APPLICATION HINTS

The LM140K is designed with thermal protection, output short-circuit protection and output transistor safe area protection. However, as with *any* IC regulator, it becomes necessary to take precautions to assure that the regulator is not inadvertently damaged. The following describes possible misapplications and methods to prevent damage to the regulator.

SHORTING THE REGULATOR INPUT

When using large capacitors at the output of these regulators, a protection diode connected input to output (Figure 17) may be required if the input is shorted to ground. Without the protection diode, an input short will cause the input to rapidly approach ground potential, while the output remains near the initial V_{OUT}because of the stored charge in the large output capacitor. The capacitor will then discharge through a large internal input to output diode and parasitic transistors. If the energy released by the capacitor is large enough, this diode, low current metal and the regulator will be destroyed. The fast diode in Figure 17 will shunt most of the capacitors discharge current around the regulator. Generally no protection diode is required for values of output capacitance ≤ 10 μF.

RAISING THE OUTPUT VOLTAGE ABOVE THE INPUT VOLTAGE

Since the output of the device does not sink current, forcing the output high can cause damage to internal low current paths in a manner similar to that just described in the “Shorting the Regulator Input” section.

REGULATOR FLOATING GROUND (Figure 18)

When the ground pin alone becomes disconnected, the output approaches the unregulated input, causing possible damage to other circuits connected to V_{OUT}. If ground is reconnected with power “ON”, damage may also occur to the regulator. This fault is most likely to occur when plugging in regulators or modules with on card regulators into powered up sockets. Power should be turned off first, thermal limit ceases operating, or ground should be connected first if power must be left on.

TRANSIENT VOLTAGES

If transients exceed the maximum rated input voltage of the device, or reach more than 0.8V below ground and have sufficient energy, they will damage the regulator. The solution is to use a large input capacitor, a series input breakdown diode, a choke, a transient suppressor or a combination of these.

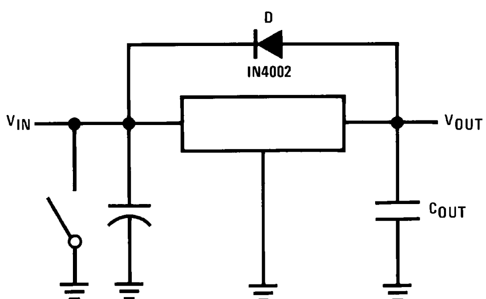


Figure 17. Input Short

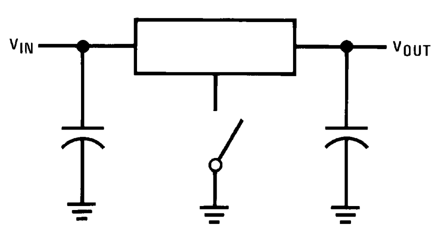


Figure 18. Regulator Floating Ground

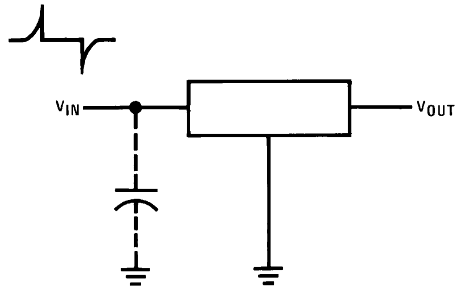
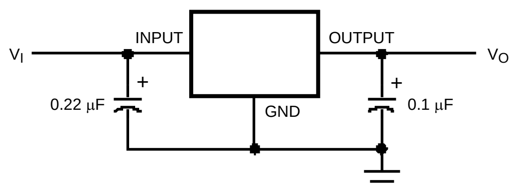


Figure 19. Transients

When a value for $\theta_{(H–A)}$ is found using the equation shown, a heatsink must be selected that has *a value that is less than or equal to this number.*

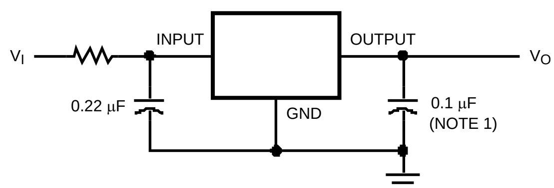
$\theta_{(H–A)}$ is specified numerically by the heatsink manufacturer in this catalog, or shown in a curve that plots temperature rise vs power dissipation for the heatsink.

Typical Applications



Bypass capacitors are recommended for optimum stability and transient response, and should be located as close as possible to the regulator.

Figure 20. Fixed Output Regulator



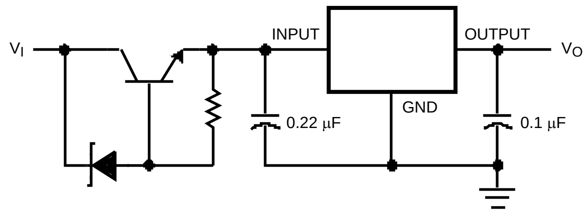
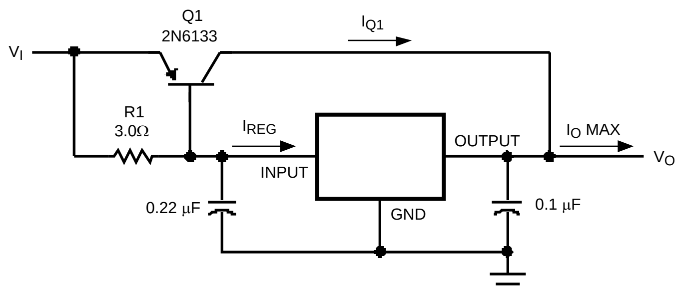


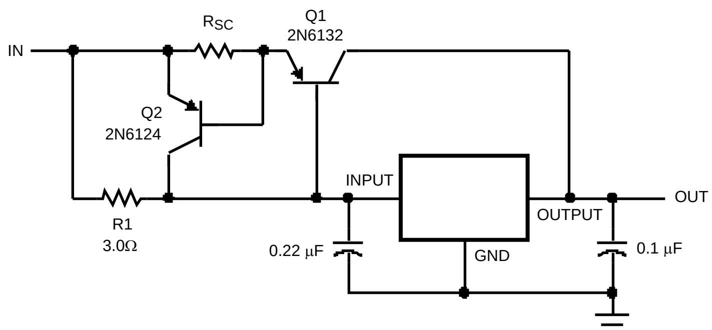
Figure 21. High Input Voltage Circuits



$$\beta(Q1) \geq \frac{I_{O\,Max}}{I_{REG\,Max}}$$

$$R1 = \frac{0.9}{I_{REG}} = \frac{\beta(Q1)\,V_{BE(Q1)}}{I_{REG\,Max}\,(\beta + 1) - I_{O\,Max}}$$

Figure 22. High Current Voltage Regulator



$$R_{SC} = \frac{0.8}{I_{SC}}$$

$$R1 = \frac{\beta V_{BE(Q1)}}{I_{REG\,Max}\,(\beta + 1) - I_{O\,Max}}$$

Figure 23. High Output Current, Short Circuit Protected

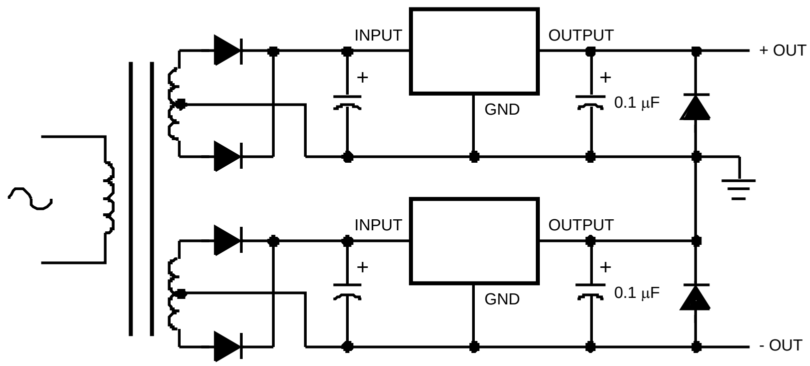


Figure 24. Positive and Negative Regulator

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM140K-12	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	No	Call TI	Call TI	-55 to 125	LM140K 12P+
LM140K-12/NOPB	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM140K 12P+
LM140K-15	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	No	Call TI	Call TI	-55 to 125	LM140K 15P+
LM140K-15/NOPB	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM140K 15P+
LM140K-5.0	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	No	Call TI	Call TI	-55 to 125	LM140K 5.0P+
LM140K-5.0/NOPB	Active	Production	TO-3 (NDS) | 2	50 | TRAY NON-STD	Yes	Call TI	Level-1-NA-UNLIM	-55 to 125	LM140K 5.0P+

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

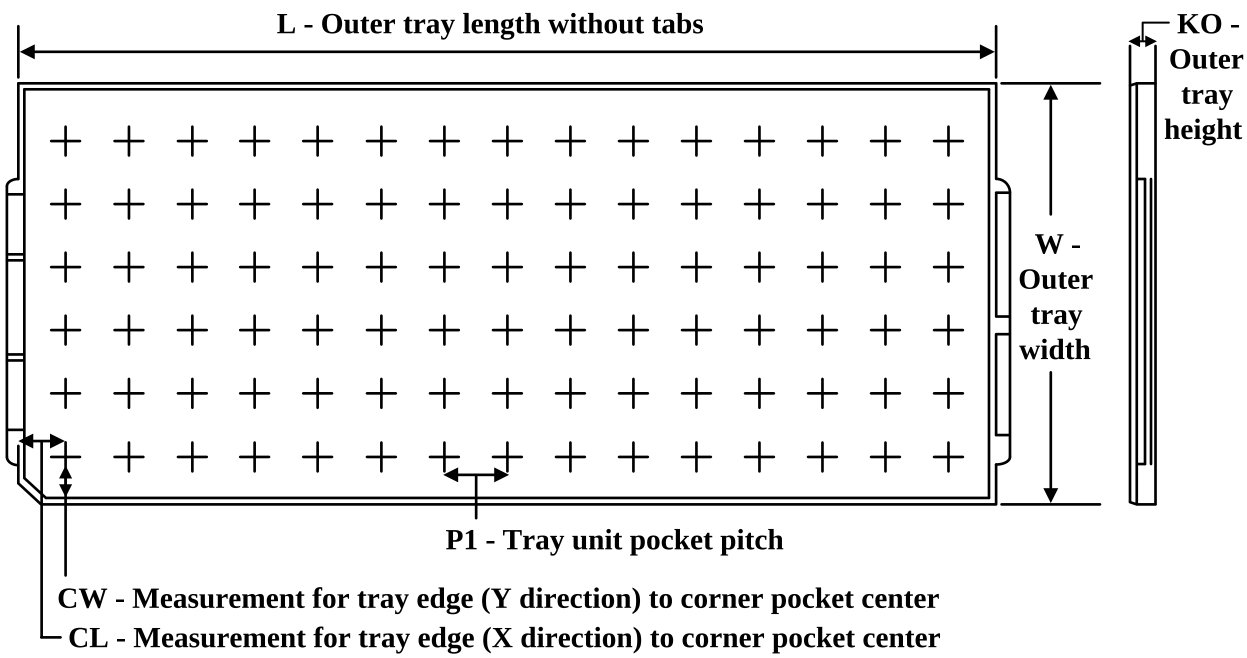
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

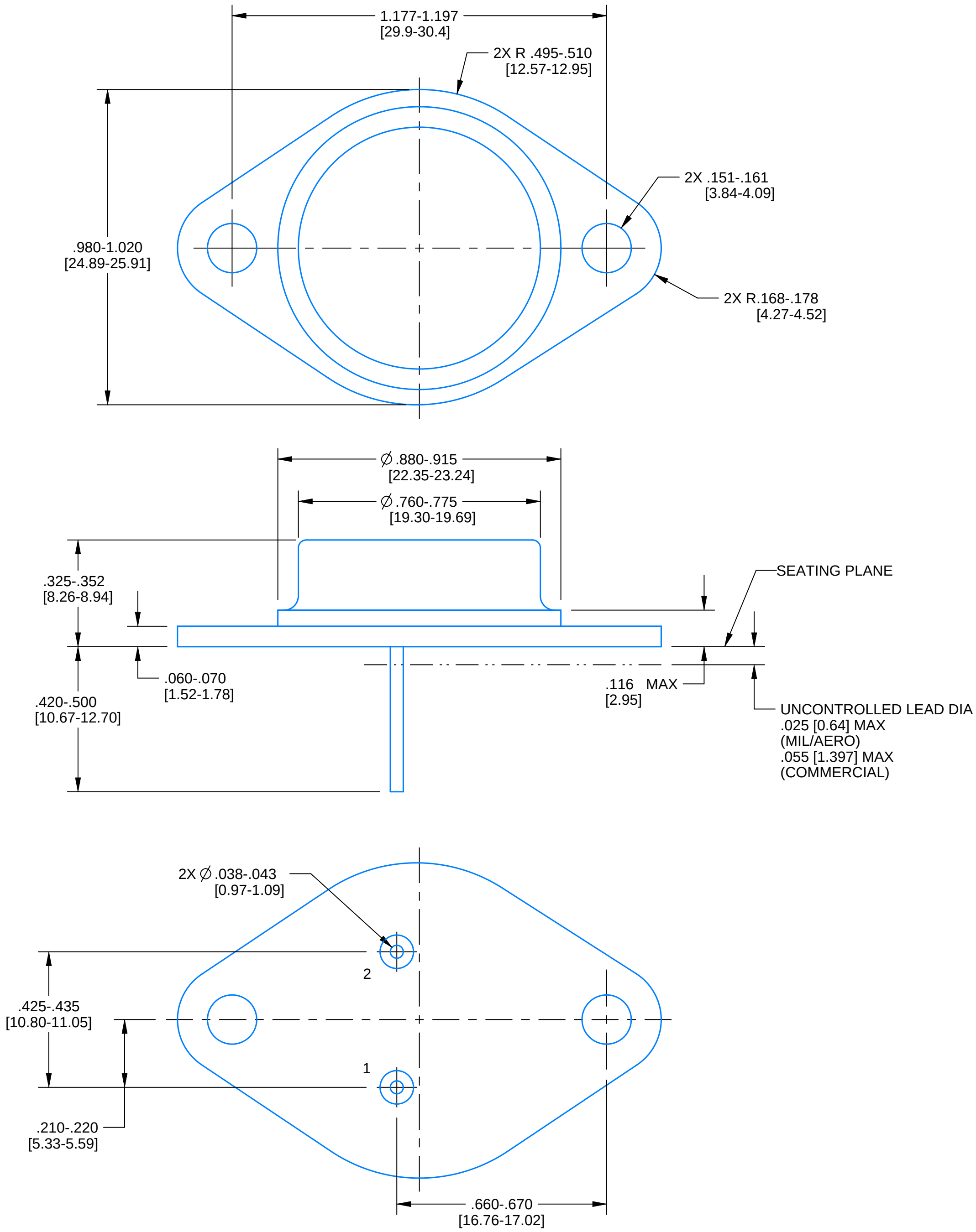
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LM140K-12	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4
LM140K-12/NOPB	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4
LM140K-15	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4
LM140K-15/NOPB	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4
LM140K-5.0	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4
LM140K-5.0/NOPB	NDS	TO-CAN	2	50	9 X 6	NA	292.1	215.9	25654	3.87	22.3	25.4

PACKAGE OUTLINE

TO-CAN - 8.94 mm max height

TRANSISTOR OUTLINE



4214773/B 09/2024

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.