

LM49270 Boomer® Audio Power Amplifier Series Filterless 2.2W Stereo Class D Audio Subsystem with OCL Headphone Amplifier, 3D Enhancement, and Headphone Sense

Check for Samples: LM49270

FEATURES

- Stereo Filterless Class D Amplifier
- Selectable OCL/CC Headphone Amplifier
- **Headphone Sense Ability**
- TI's 3D Enhancement
- **RF Suppression**
- I²C Control Interface
- 32-Step Digital Volume Control
- **6 Operating Modes**
- **Output Short Circuit Protection and Thermal** Shutdown Protection
- **Minimum External Components**
- **Click and Pop Suppression**
- **Micro-Power Shutdown**
- **Independent Speaker and Headphone Volume** Controls
- Available in Space-Saving 28 Pin WQFN **Package**

APPLICATIONS

- **Portable DVD Players**
- **Smart Phones**
- **PDAs**
- Laptops

KEY SPECIFICATIONS

- Stereo Class D Amplifier Efficiency:
 - V_{DD} = 3.3V, 450mW/Ch into 8Ω 84%
 - V_{DD} = 5V, 1W/Ch into 8Ω 84%
- Quiescent Power Supply Current, $V_{DD} = 3.3V$
 - Speaker Mode 5.5 mA
 - Headphone Mode (OCL) 4 mA
- Power Output/Channel, $V_{DD} = 5V$
 - Class D Speaker Amplifier:
 - R_1 = 4Ω, THD+N = ≤ 10% 2.3 W
 - R_L = 8Ω, THD+N = ≤ 1% 106 W

- Headphone Amplifier:

- R_L = 16Ω, THD+N = ≤ 1% 155 mW
- R_L = 32Ω, THD+N = ≤ 1% 90 mW
- Shutdown Current 0.02µA

DESCRIPTION

The LM49270 is a fully integrated audio subsystem designed for stereo multimedia applications. The LM49270 combines a 2.2W stereo Class D amplifier with a 155mW stereo headphone amplifier, volume control, headphone sense, and TI's unique 3D sound enhancement into a single device. The LM49270 uses flexible I²C control interface for multiple application requirements.

The filterless stereo class D amplifiers delivers 2.2W/channel into a 4Ω load with less than 10% THD+N with a 5V supply. The headphone amplifier features Output Capacitor-less (OCL) architecture that eliminates the output coupling capacitors required by traditional headphone amplifiers.

The IC features a headphone sense input (HPS) that automatically detects the presence of a headphone and configures the device accordingly. The LM49270 can automatically switch from OCL headphone output to a line driver output. If the VOC pin is pulled to GND, the VOC amplifier is disabled and the VOC pin is internally set to GND. This feature allows the LM49270 to be used as a line driver in OCL mode without a GND conflict on the headphone jack sleeve. Additionally, the headphone amplifier can be configured as capacitively coupled (CC).

The LM49270 features a 32 step volume control for the headphone and stereo outputs. The device mode select and volume are controlled through an I²C compatible interface.

Output short circuit and thermal shutdown protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM49270 is available in a space saving 28-pin, 5x5mm WQFN package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet. All trademarks are the property of their respective owners.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Typical Application

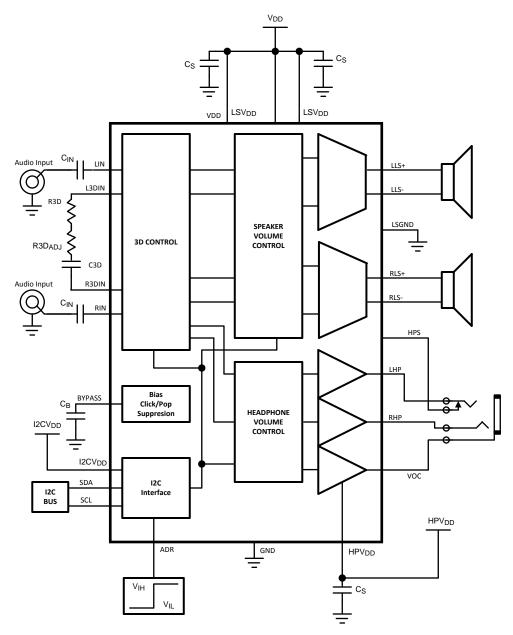


Figure 1. Typical Audio Amplifier Application Circuit



Connection Diagram

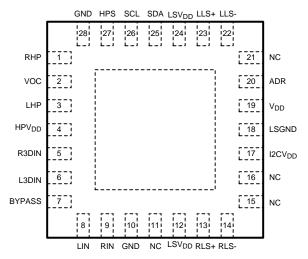


Figure 2. WQFN Package 5mm x 5mm x 0.8mm Top View See Package Number RSG0028A

Pin Descriptions

PIN	NAME	DESCRIPTION
1	RHP	Right channel headphone output
2	VOC	VDD/2 buffer output
3	LHP	Left channel headphone output
4	HPV _{DD}	Headphone supply input
5	R3DIN	Right channel 3D input
6	L3DIN	Left channel 3D input
7	BYPASS	Bias bypass
8	LIN	Left channel input
9	RIN	Right channel input
10	GND	Analog ground
11	NC	No connect
12	LSV _{DD}	Speaker supply voltage input
13	RLS+	Right channel non-inverting speaker output
14	RLS-	Right channel inverting speaker output
15	NC	No connect
16	NC	No connect
17	I2CV _{DD}	I2C supply voltage input
18	LSGND	Speaker ground
19	V_{DD}	Power supply
20	ADR	Address
21	NC	No connect
22	LLS-	Left channel inverting speaker output
23	LLS+	Left channel non-inverting speaker output
24	LSV _{DD}	Speaker supply voltage input
25	SDA	Serial data input
26	SCL	Serial clock input
27	HPS	Headphone sense input



Pin Descriptions (continued)

PIN	NAME	DESCRIPTION	
28	GND	Headphone ground	

Absolute Maximum Ratings (1)(2)(3)

(1)			
Supply Voltage (1)		6.0V	
Storage Temperature		−65°C to +150°C	
Input Voltage	-0.3V to V _{DD} +0.3V		
Power Dissipation (4)	Internally Limited		
ESD Susceptibility ⁽⁵⁾		2000V	
ESD Susceptibility (6)		200V	
Junction Temperature (T _{JMAX})	Junction Temperature (T _{JMAX})		
Thermal Resistance	θ_{JA}	35.1°C/W	

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which specify performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is P_{DMAX} = (T_{JMAX} T_A)/ θ_{JA} or the number given in Absolute Maximum Ratings, whichever is lower. For the LM49270 see power derating currents for more information.
- (5) Human body model, 100pF discharged through a $1.5k\Omega$ resistor.
- (6) Machine Model, 220pF–240pF discharged through all pins.

Operating Ratings (1)

-		
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	-40°C ≤ T _A ≤ 85°C
Supply Voltage (V _{DD} , LSV _{DD} , HPV _{DD})		$2.4 \text{V} \leq \text{V}_{\text{DD}} \leq 5.5 \text{V}$
I ² C Voltage (I ² CV _{DD})		$2.4V \le I^2CV_{DD} \le 5.5V$

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.

Submit Documentation Feedback



Electrical Characteristics $V_{DD} = 3.3V$

⁽¹⁾The following specifications apply for Headphone: $A_V = 0$ dB, $R_{L(HP)} = 32\Omega$; for Loudspeakers: $A_V = 6$ dB, $R_{L(SP)} = 15\mu$ H + 8Ω + 15μH , f = 1kHz, unless otherwise specified. Limits apply for $T_A = 25$ °C.

Symbol	Parameter	Conditions		9270	Units
Symbol	Parameter	Conditions	Typical ⁽²⁾	Limit ^{(3) (4)}	(Limits)
I _{DD}	Supply Current	V _{IN} = 0, R _L = No Load, Both channels active Speaker ON, HP OFF Speaker OFF, CC HP ON Speaker OFF, OCL HP ON	5.5 3 4	7.6 4.7 5.75	mA (max) mA (max) mA (max)
I _{SD}	Shutdown Supply Current	-	0.02	2	μA (max)
Vos	Output Offset Voltage	Headphone Speaker	10 10	25 60	mV (max) mV (max)
		Speaker Mode, f = 1kHz	,		
		$\begin{aligned} THD+N &= 1\% \\ R_L &= 4\Omega \\ R_L &= 8\Omega \end{aligned}$	700 450	400	mW mW (min
		$\begin{aligned} THD+N &= 10\% \\ R_L &= 4\Omega \\ R_L &= 8\Omega \end{aligned}$	870 560		mW mW
		CC Headphone Mode, f = 1kHz			
P _{OUT}	Output Power	$\begin{aligned} THD+N &= 1\% \\ R_L &= 16\Omega \\ R_L &= 32\Omega \end{aligned}$	60 36	30	mW mW (min
			74 55		mW mW
		OCL Headphone Mode, f = 1kHz	+	+	
			60 36	30	mW mW (min
			73 55		mW mW
		Speaker Mode, $f = 1kHz$ $P_{OUT} = 100mW$, $R_L = 8\Omega$	0.02		%
THD+N	Total Harmonic Distortion + Noise	CC Headphone Mode, f = 1kHz $P_{OUT} = 12mW, R_L = 32\Omega$	0.015		%
		OCL Headphone Mode, f = 1kHz	0.02		%
		$P_{OUT} = 12$ mW, $R_L = 32\Omega$ Speaker Mode,	47		μV
e _N	Noise	A-Wtg, Input Referred CC Headphone Mode,	10		μV
14		A-Wtg, Input Referred OCL Headphone Mode, A-Wtg, Input Referred	11		μV
η	Efficiency	Speaker Mode $R_L = 8\Omega$	84		%
		Speaker Mode, f = 1kHz, V _{IN} = 1Vp-p	71		dB
Xtalk	Crosstalk	CC Headphone Mode, f = 1kHz, V _{IN} = 1Vp-p	70		dB
		OCL Headphone Mode, f = 1kHz, V _{IN} = 1Vp-p	55		dB

All voltages are measured with respect to the ground pin, unless otherwise specified.

Copyright © 2006–2007, Texas Instruments Incorporated

Typicals are measured at 25°C and represent the parametric norm.

Limits are specified to AOQL (Average Outgoing Quality Level).

Data sheet min and max specification limits are specified by design, test, or statistical analysis.



Electrical Characteristics $V_{DD} = 3.3V$ (continued)

⁽¹⁾ The following specifications apply for Headphone: $A_V = 0$ dB, $R_{L(HP)} = 32\Omega$; for Loudspeakers: $A_V = 6$ dB, $R_{L(SP)} = 15\mu$ H + 8Ω + 15μH , f = 1kHz, unless otherwise specified. Limits apply for $T_A = 25$ °C.

Symbol	Baramatan	Conditions	LM4	9270	Units
	Parameter	Conditions	Typical ⁽²⁾	Limit ^{(3) (4)}	(Limits)
T _{ON}	Turn-on Time		30		ms
T _{OFF}	Turn-off Time		64		ms
7	lanut Impadance	Maximum Gain	23.5		kΩ
Z _{IN}	Input Impedance	Minimum Gain	210		kΩ
		Maximum Gain, Speaker Mode	30		dB
۸	Cain	Minimum Gain, Speaker Mode	-47		dB
A_V	Gain	Maximum Gain, Headphone Mode	18		dB
		Minimum Gain, Headphone Mode	-59		dB
		Speaker Mode, V _{RIPPLE} = 200mVp-p Sine f = 217Hz f = 1kHz	68 68		dB dB
PSRR	Power Supply Rejection Ratio	Headphone Mode, V _{RIPPLE} = 200mVp-p Sine, CC Mode f = 217Hz f = 1kHz	73 73		dB dB
		Headphone Mode, V _{RIPPLE} = 200mVp-p Sine, OCL Mode f = 217Hz f = 1kHz	75 79		dB dB
LIDO	Handahana Canas Threshold	Detect Headphone		2.9	V (min)
HPS _(Th)	Headphone Sense Threshold	Detect no Headphone		1.8	V (max)

Electrical Characteristics $V_{DD} = 5.0V$

⁽¹⁾The following specifications apply for Headphone" $A_V = 0$ dB, $R_{L(HP)} = 32Ω$,: for Loudspeakers: $A_V = 6$ dB, $R_{L(SP)} = 15μH + 8Ω + 15μH$, f = 1kHz unless otherwise specified. Limits apply for $T_A = 25$ °C.

Symbol	Barranatar	O and this area	LM4	Units		
	Parameter	Conditions	Typical (2)	Limit ⁽³⁾ (4)	(Limits)	
I _{DD}	Supply Current	V _{IN} = 0, R _L = No Load, Both channels active Speaker ON, HP OFF Speaker OFF, CC HP ON Speaker OFF, OCL HP ON	8.5 3.6 4.7	12.4 5.5 6.5	mA (max) mA (max) mA (max)	
I _{SD}	Shutdown Supply Current		0.15	2	μA (max)	
V _{OS}	Output Offset Voltage	Headphone Speaker	10 10	25 60	mV (max) mV (max)	

¹⁾ All voltages are measured with respect to the ground pin, unless otherwise specified.

⁽²⁾ Typicals are measured at 25°C and represent the parametric norm.

⁽³⁾ Limits are specified to AOQL (Average Outgoing Quality Level).

⁽⁴⁾ Data sheet min and max specification limits are specified by design, test, or statistical analysis.



Electrical Characteristics $V_{DD} = 5.0V$ (continued)

 $^{(1)}$ The following specifications apply for Headphone" A_V = 0dB, $R_{L(HP)}$ = 32 Ω ,: for Loudspeakers: A_V = 6dB, $R_{L(SP)}$ = 15 μ H + 8 Ω + 15 μ H, f = 1kHz unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions		LM49270		
Symbol	raidilleter	Conditions	Typical (2)	Limit ^{(3) (4)}	(Limits)	
		Speaker Mode, f = 1kHz,				
		$THD+N=1\%$ $R_L=4\Omega$ $R_L=8\Omega$	1.75 1.06		W W	
		$THD+N=10~\%$ $R_L=4\Omega$ $R_L=8\Omega$	2.2 1.35		W W	
		CC Headphone Mode, f = 1kHz,				
P _{OUT}	Output Power	$THD+N=1\%$ $R_L=16\Omega$ $R_L=32\Omega$	155 90		mW mW	
		$THD+N=10\%$ $R_L=16\Omega$ $R_L=32\Omega$	177 140		mW mW	
		OCL Headphone Mode, f = 1kHz,				
		$THD+N=1\%$ $R_L=16\Omega$ $R_L=32\Omega$	155 90		mW mW	
		$THD+N=10\%$ $R_L=16\Omega$ $R_L=32\Omega$	175 140		mW mW	
		Speaker Mode, $f = 1kHz$ $P_{OUT} = 100mW$, $R_L = 8\Omega$	0.03		%	
THD+N	Total Harmonic Distortion + Noise	CC Headphone Mode, $f = 1kHz$ $P_{OUT} = 12mW, R_L = 32\Omega$	0.02		%	
		OCL Headphone Mode, f = 1kHz $P_{OUT} = 12mW, R_L = 32\Omega$	0.03		%	
		Speaker Mode, A-Wtg, Input Referred	47		μV	
e _N	Noise	CC Headphone Mode, A-Wtg, Input Referred	10		μV	
		OCL Headphone Mode, A-Wtg, Input Referred	11		μV	
η	Efficiency	Speaker Mode $R_L = 8\Omega$	84		%	
		Speaker Mode, f = 1kHz, V _{IN} = 1Vp-p	-85		dB	
Xtalk	Crosstalk	CC Headphone Mode, f = 1kHz, V _{IN} = 1Vp-p	-70		dB	
		OCL Headphone Mode, f = 1kHz, V _{IN} = 1Vp-p	-58		dB	
T _{ON}	Turn-on Time		43		ms	
T _{OFF}	Turn-off Time		100		ms	
Z _{IN}	Input Impedance	Maximum Gain	23.5		kΩ	
	pat impodanoo	Minimum Gain	210		kΩ	
		Maximum Gain, Speaker Mode	30		dB	
A_V	Gain	Minimum Gain, Speaker Mode	-47		dB	
· ·v		Maximum Gain, Headphone Mode	18		dB	
		Minimum Gain, Headphone Mode	-59		dB	



Electrical Characteristics $V_{DD} = 5.0V$ (continued)

 $^{(1)}$ The following specifications apply for Headphone" A_V = 0dB, $R_{L(HP)}$ = 32 Ω ,: for Loudspeakers: A_V = 6dB, $R_{L(SP)}$ = 15 μ H + 8 Ω + 15 μ H, f = 1kHz unless otherwise specified. Limits apply for T_A = 25°C.

Counch of	Donomotor	Conditions	LM4	LM49270		
Symbol	Parameter	Conditions	Typical ⁽²⁾	Limit ^{(3) (4)}	(Limits)	
PSRR Por		Speaker Mode, V _{RIPPLE} = 200mVp-p Sine f = 217Hz f = 1kHz	61 61		dB dB	
	Power Supply Rejection Ratio	Headphone Mode, V _{RIPPLE} = 200mVp-p Sine, CC Mode f = 217Hz f = 1kHz	75 74		dB min	
		Headphone Mode, V _{RIPPLE} = 200mVp-p Sine, OCL Mode f = 217Hz f = 1kHz	78 75		dB dB	
UDC	Headphone Sense Threshold	Detect Headphone		4.4	V (min)	
HPS _(Th)	Heauphone Sense Threshold	Detect no Headphone		3	V (max)	



Typical Performance Characteristics

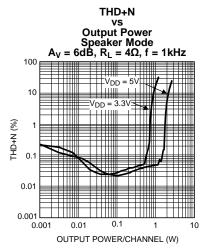
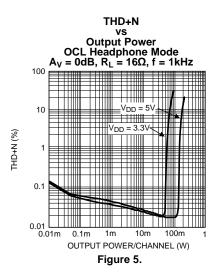
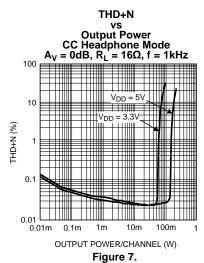


Figure 3.





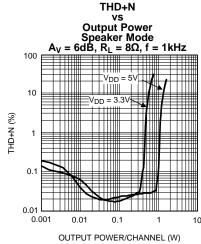
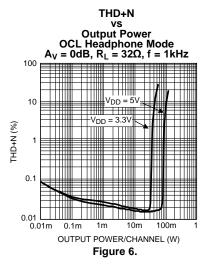


Figure 4.



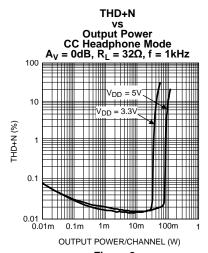


Figure 8.



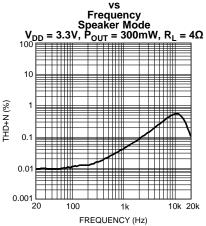
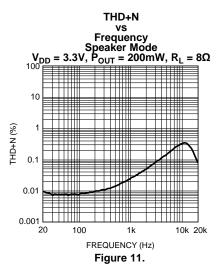
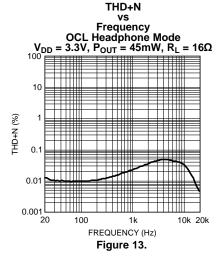


Figure 9.





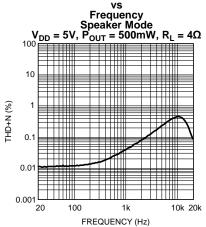


Figure 10.

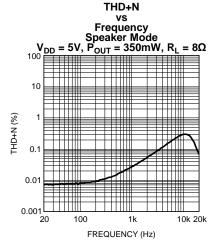
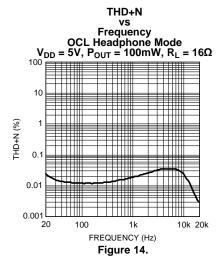


Figure 12.



Submit Documentation Feedback



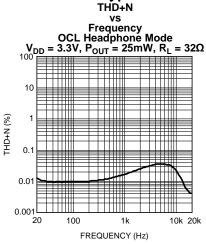


Figure 15.

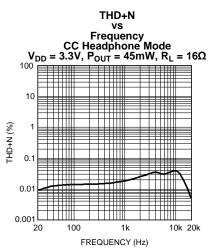
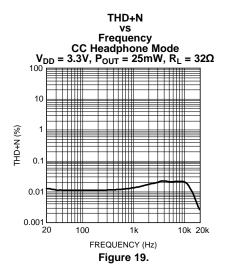


Figure 17.



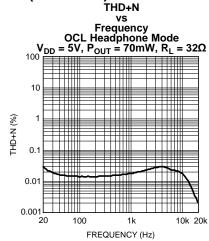
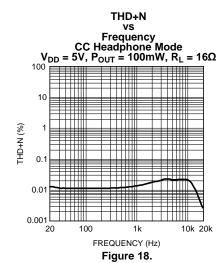


Figure 16.



THD+N vs Frequency CC Headphone Mode $V_{DD} = 5V, P_{OUT} = 70mW, R_{L} = 32\Omega$ 100 10 (%) N+QHL 0.1 0.01 0.001 20 100 1k 10k 20k FREQUENCY (Hz)

Figure 20.



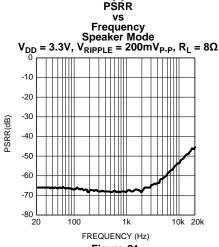


Figure 21.

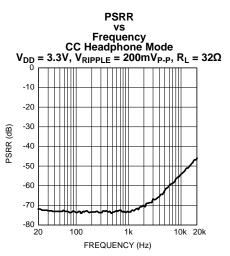
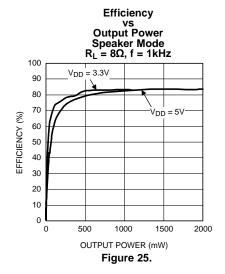


Figure 23.



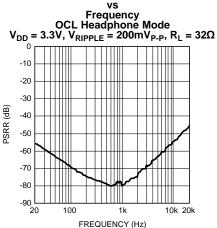


Figure 22.

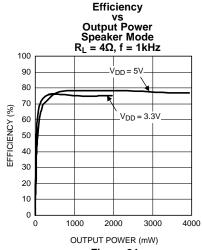


Figure 24.

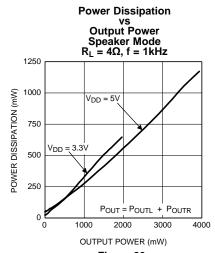
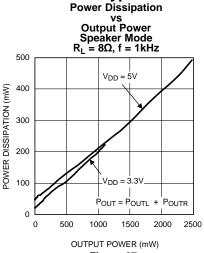


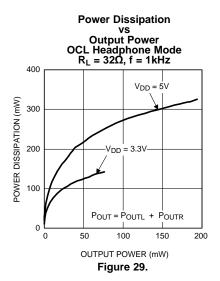
Figure 26.

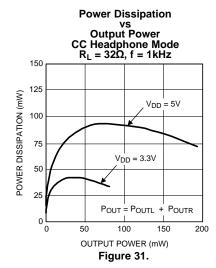
Submit Documentation Feedback











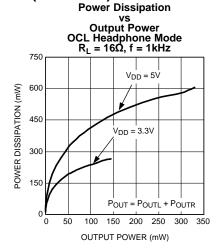


Figure 28.

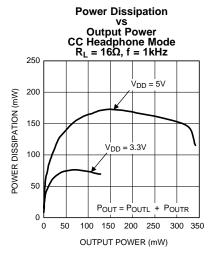
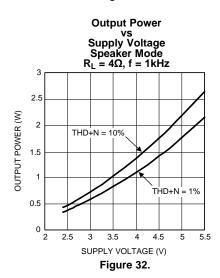
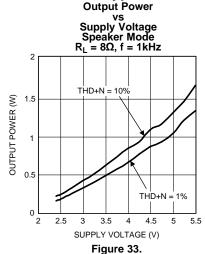
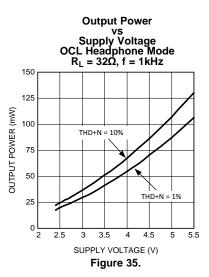


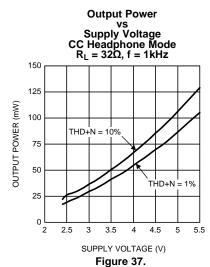
Figure 30.

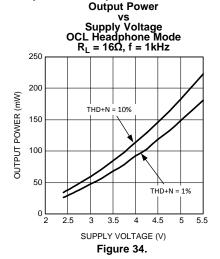


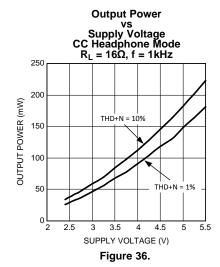












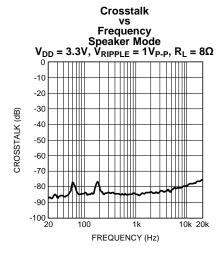
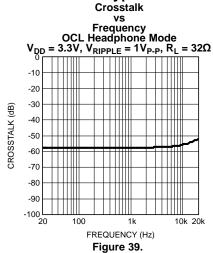


Figure 38.

Submit Documentation Feedback





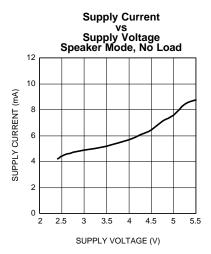
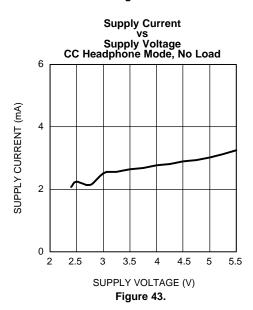


Figure 41.



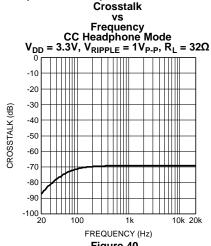
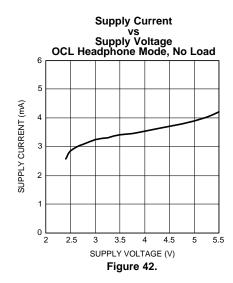


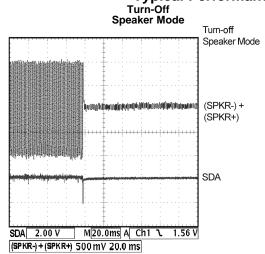
Figure 40.



Turn-On Speaker Mode Turn-on Speaker Mode (SPKR-)+ (SPKR+) SDA SDA 2.00 V M20.0ms A Ch1 J (SPKR-)+(SPKR+) 500 mV 20.0 ms

Figure 44.





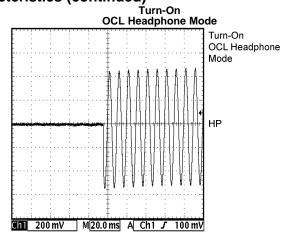
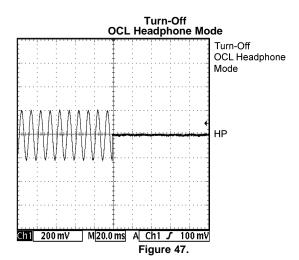
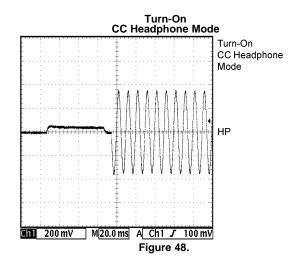
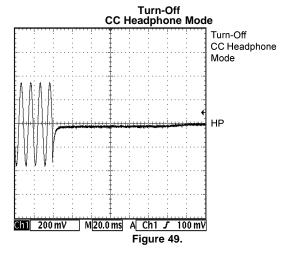


Figure 45.

Figure 46.







Submit Documentation Feedback

Copyright © 2006–2007, Texas Instruments Incorporated



APPLICATION INFORMATION

12C COMPATIBLE INTERFACE

The LM49270 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open-collector), although the LM49270 does not write to the I²C bus. The LM49270 and the master can communicate at clock rates up to 400kHz. Figure 51 shows the I²C interface timing diagram. The LM49270 is a transmit/receive slave-only device, reliant upon the master to generate a clock signal.

The master device communicates to the LM49270 by transmitting the proper device address followed by a command word. Each transmission sequence is framed by a START condition and a STOP condition. Each word (register address + register content) transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse.

To avoid an address conflict with another device on the I^2C bus, the LM49270 address is determined by the ADR pin, the state of ADR determines address bit A1 (Table 1). When ADR = 0, the address is 1111 1000. When ADR = 1 the device address is 1111 1010.

Table 1. Device Address

ADR	A7	A6	A5	A4	А3	A2	A 1	Α0
Х	1	1	1	1	1	0	X	0
0	1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	1	0

Table 2. I²C Control Registers

REG	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0	Shutdown Control	0	0	_	_	HP3DSEL	LS3DSEL	OCL/CC	PWR_ON
1	Headphone Gain Control	0	1	_	HP4	HP3	HP2	HP1	HP0
2	Speaker Gain Control	1	0	_	LS4	LS3	LS2	LS1	LS0

NOTE

OCL/CC = 1 selects OCL mode; OCL/CC = 0 selects cap coupled mode

PWR_ON = 0 puts part in shutdown

BUS FORMAT

The I²C bus format is shown in Figure 50. The "start" signal is generated by lowering the data signal while the clock is high. The start signal alerts all devices on the bus that a device address is being written to the bus.

The 8-bit device address is written to the bus next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock is high.

After the last address bit is sent, the master device releases the data line, during which time, an acknowledge clock pulse is generated. If the LM49270 receives the address correctly, then the LM49270 pulls the data line low, generating an acknowledge bit (ACK).

Once the master device has registered the ACK bit, the 8-bit register address/data word is sent. Each data bit should be stable while the clock level is high. After the 8-bit word is sent, the LM49270 sends another ACK bit. Following the acknowledgement of the data word, the master device issues a "stop" bit, allowing SDA to go high while the clock signal is high.

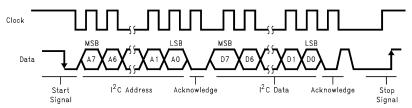


Figure 50. I²C Bus Format

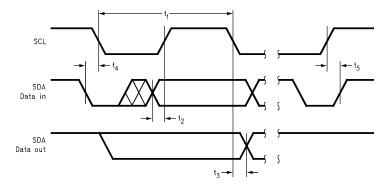


Figure 51. I²C Timing Diagram

GENERAL AMPLIFIER FUNCTION

Class D Amplifier

The LM49270 features a high-efficiency, filterless, Class D stereo amplifier. The LM49270 Class D amplifiers feature a filterless modulation scheme known as Class BD. The differential outputs of each channel switch at 300kHz from V_{DD} to GND. When there is no input signal applied, the two outputs (LLS+ and LLS-) switch in phase with a 50% duty cycle. Because the outputs of the LM49270 are differential, there is in no net voltage across the speaker, thus no load current during the idle state conserving power.

When an input signal is applied, the duty cycle (pulse width) of each output changes. For increasing output voltages, the duty cycle of LLS+ increases, while the duty cycle of LLS- decreases. For decreasing output voltages, the converse occurs. The duty cycle of LLS- increases while the duty cycle of LLS+ decreases. The difference between the two pulse widths yields the differential output voltage.

Headphone Amplifier

The LM49270 headphone amplifier features two different operating modes, output capacitor-less (OCL) and capacitor coupled (CC). The OCL architecture eliminates the bulky, expensive output coupling capacitors required by traditional headphone amplifiers. The LM49270 headphone section uses three amplifiers. Two amplifiers drive the headphones while the third (VOC) is set to the internally generated bias voltage (typically $V_{DD}/2$). The third amplifier is connected to the return terminal (sleeve) of the headphone jack. In this configuration, the signal side of the headphones are biased to $V_{DD}/2$, the return is biased to $V_{DD}/2$, thus there is no net DC voltage across the headphone eliminating the need for an output coupling capacitor. Removing the output coupling capacitors from the headphone signal path reduces component count, reducing system cost and board space consumption, as well as improving low frequency performance and sound quality. The voltage on the return sleeve is not an issue when driving headphones. However, if the headphone output is used as a line out, the $V_{DD}/2$ can conflict with the GND potential that a line-in would expect on the return sleeve. When the return of the headphone jack is connected to GND, the LM49270 detects an output short circuit condition and the VOC amplifier is disabled preventing damage to the LM49270 and allowing the headphone return to be biased at GND.



Capacitor Coupled Headphone Mode

In capacitor coupled (CC) mode, the VOC pin is disabled, and the headphone outputs are coupled to the jack through series capacitors, allowing the headphone return to be connected to GND (Figure 52). In CC mode, the LM49270 requires output coupling capacitors to block the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and speaker impedance form a high pass filter with a -3dB roll-off determined by:

$$f_{-3dB} = 1 / 2\pi R_L C_{OUT}$$

Where R_L is the headphone impedance, and C_{OUT} is the output coupling capacitor. Choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high results in poor low frequency performance. Select capacitor dielectric types with low ESR to minimize signal loss due to capacitor series resistance and maximize power transfer to the load.

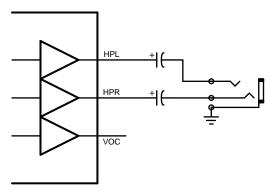


Figure 52. Capacitor Coupled Headphone Mode

Headphone Sense

The LM49270 features a headphone sense input (HPS) that monitors the headphone jack and configures the device depending on the presence of a headphone. When the HPS pin is low, indicating that a headphone is not present, the LM49270 speaker amplifiers are active and the headphone amplifiers are disabled. When the HPS pin is high, indicating that a headphone is present, the headphone amplifiers are active while the speaker amplifiers are disabled.

POWER DISSIPATION AND EFFICIENCY

The major benefit of Class D amplifier is increased efficiency versus Class AB. The efficiency of the LM49270 speaker amplifiers is attributed to the output transistors' region of operation. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance $(R_{DS(ON)})$, along with the switching losses due to gate charge.

The maximum power dissipation per headphone channel in Capacitor Coupled mode is given by:

$$P_{DMAX(CC)} = V_{DD}^2/2\pi^2R_L$$

In OCL mode, the maximum power dissipation increases due to the use of a third amplifier as a buffer. The power dissipation is given by:

$$P_{DMAX(OCL)} = V_{DD}^2/\pi^2 R_L$$

SHUTDOWN FUNCTION

The LM49270 features a shutdown mode configured through the I^2C interface. Bit D0 (PWR_ON) in the Shutdown Control register shuts down/turns on the entire device. Set PWR_ON = 1 to enable the LM49270, set PWR ON = 0 to disable the device.

AUDIO AMPLIFIER GAIN SETTING

Each channel of the LM49270 features a 32 step volume control. The loudspeaker volume has a range of -47dB to 30dB and the headphone has a range of -59dB to 18dB (see Table 3).



Table 3. Volume Control

Table 3. Volume Control										
Volume Step	LS4/HP4	LS3/HP3	LS2/HP2	LS1/HP1	LS0/HP0	LS Gain (dB)	HP Gain (dB)			
1	0	0	0	0	0	-47	– 59			
2	0	0	0	0	1	-36	-48			
3	0	0	0	1	0	-28.5	-46.5			
4	0	0	0	1	1	-22.5	-34.5			
5	0	0	1	0	0	-18	-30			
6	0	0	1	0	1	-15	-27			
7	0	0	1	1	0	-12	-24			
8	0	0	1	1	1	-9	-21			
9	0	1	0	0	0	-6	-18			
10	0	1	0	0	1	-3	-15			
11	0	1	0	1	0	-1.5	-13.5			
12	0	1	0	1	1	0	-12			
13	0	1	1	0	0	1.5	-10.5			
14	0	1	1	0	1	3	-9			
15	0	1	1	1	0	4.5	-7.5			
16	0	1	1	1	1	6	-6			
17	1	0	0	0	0	7.5	-4.5			
18	1	0	0	0	1	9	-3			
19	1	0	0	1	0	10.5	-1.5			
20	1	0	0	1	1	12	0			
21	1	0	1	0	0	13.5	1.5			
22	1	0	1	0	1	15	3			
23	1	0	1	1	0	16.5	4.5			
24	1	0	1	1	1	18	6			
25	1	1	0	0	0	19.5	7.5			
26	1	1	0	0	1	21	9			
27	1	1	0	1	0	22.5	10.5			
28	1	1	0	1	1	24	12			
29	1	1	1	0	0	25.5	13.5			
30	1	1	1	0	1	27	15			
31	1	1	1	1	0	28.5	16.5			
32	1	1	1	1	1	30	18			

3D ENHANCEMENT

The LM49720 features TI's 3D sound enhancement. 3D sound improves the apparent stereo channel separation whenever the left and right speakers are located close to each other, widening the perceived sound stage in devices with a small form factor that prohibits proper speaker placement.

An external RC network , shown in Figure 1, enables the 3D effect. R3D sets the level of the 3D effect; decreasing the value of R3D will increase the 3D effect. The 3D network acts like a high pass filter C3D sets the frequency response; increasing the value of C3D will decrease the low cutoff frequency at which the 3D effect starts to occur, as shown by this equation:

$$f_{3D(-3dB)} = 1/2\pi(R3D)(C3D)$$
 (1)

Enabling the 3D effect increases the gain by a multiplication factor of $(1 + 20k\Omega/R3D)$. Setting R3D to $20k\Omega$ results in a 6dB increase (doubling) of the gain, increasing the 3D effect. The level of 3D effect is also dependent on other factors such as speaker placement and the distance from the speakers to the listener. The values of R3D and C3D should be chosen for each application individually, taking into account the physical factors noted before.

Submit Documentation Feedback

Copyright © 2006–2007, Texas Instruments Incorporated



POWER SUPPLIES

The LM49270 uses different supplies for each portion of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The speaker amplifier gain stage is powered from V_{DD} , while the output stage is powered from LSV_{DD}. The headphone amplifiers, input amplifiers and volume control stages are powered from HPV_{DD}. The separate power supplies allow the speakers to operate from a higher voltage for maximum headroom, while the headphones operate from a lower voltage, improving power dissipation. HPV_{DD} may be driven by a linear regulator to further improve performance in noisy environments. The I^2 C portion if powered from I^2 CV_{DD}, allowing the I^2 C portion of the LM49270 to interface with lower voltage digital controllers.

PROPER SELECTION OF EXTERNAL COMPONENTS

Audio Amplifier Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitor as close to the device as possible. Typical applications employ a voltage regulator with $10\mu\text{F}$ and $0.1\mu\text{F}$ bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM49270 supply pins. A $1\mu\text{F}$ capacitor is recommended.

Bypass Capacitor Selection

The LM49270 generates a $V_{DD}/2$ common-mode bias voltage internally. The BYPASS capacitor, C_B , improves PSRR and THD+N by reducing noise at the BYPASS node. Use a 1 μ F capacitor, placed as close to the device as possible for C_B .

Audio Amplifier Input Capacitor Selection

Input capacitors, C_{IN} , in conjunction with the input impedance of the LM49270 forms a high pass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimal DC level. Assuming zero source impedance, the -3dB point of the high pass filter is given by:

$$f_{(-3dB)} = 1/2\pi R_{IN} C_{IN}$$
 (2)

Choose C_{IN} such that f_{-3dB} is well below that lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency responses of the amplifier. Use capacitors with low voltage coefficient dielectrics, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies. Other factors to consider when designing the input filter include the constraints of the overall system. Although high fidelity audio requires a flat frequency response between 20Hz and 20kHz, portable devices such as cell phones may only concentrate on the frequency range of the frequency range of the spoken human voice (typically 300Hz to 4kHz). In addition, the physical size of the speakers used in such portable devices limits the low frequency response; in this case, frequencies below 150Hz may be filtered out.



REVISION TABLE

Rev Date		Date	Description					
	1.0	12/19/06	Initial release.					

Submit Documentation Feedback

www.ti.com 11-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
LM49270SQ/NOPB	Active	Production	WQFN (RSG) 28	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	49270SQ
LM49270SQ/NOPB.A	Active	Production	WQFN (RSG) 28	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	49270SQ

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

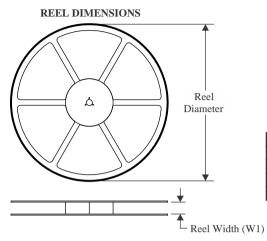
⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

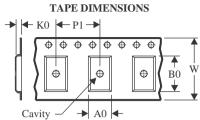
⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

www.ti.com 1-Aug-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

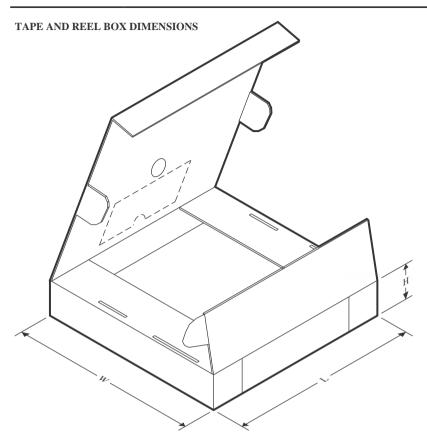


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49270SQ/NOPB	WQFN	RSG	28	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

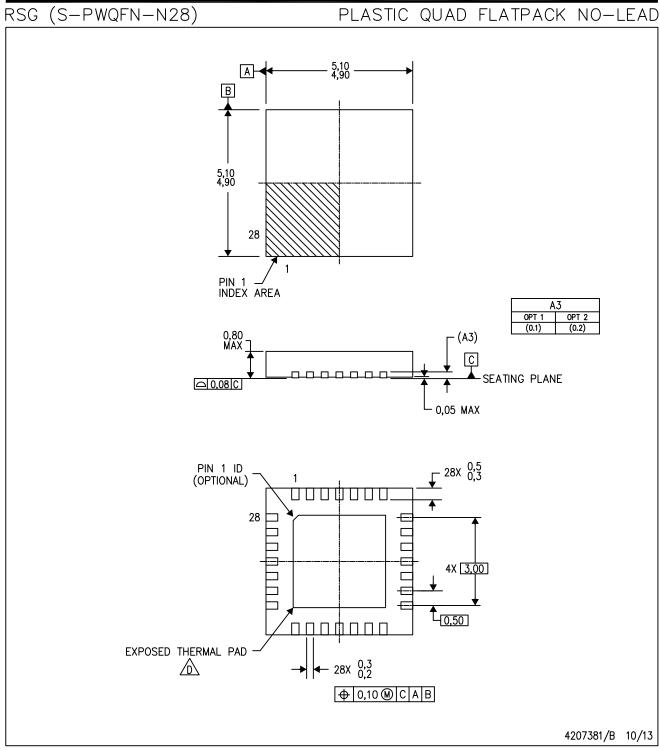
PACKAGE MATERIALS INFORMATION

www.ti.com 1-Aug-2025



*All dimensions are nominal

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	LM49270SQ/NOPB	WQFN	RSG	28	1000	208.0	191.0	35.0	



- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025