LPC660 Low Power CMOS Quad Operational Amplifier

Check for Samples: LPC660

FEATURES

- **Rail-to-rail output swing**
- **Micropower operation: (1 mW)**
- **Specified for 100 kΩ and 5 kΩ loads**
- **High voltage gain: 120 dB**
- **Low input offset voltage: 3 mV**
- **Low offset voltage drift: 1.3 µV/°C**
- **Ultra low input bias current: 2 fA**
- **Input common-mode includes V^-**
- **Operation range from +5V to +15V**
- **Low distortion: 0.01% at 1 kHz**
- **Slew rate: 0.11 V/µs**
- **Full military temp. range available**

APPLICATIONS

- **High-impedance buffer**
- **Precision current-to-voltage converter**
- **Long-term integrator**
- **High-impedance preamplifier**
- **Active filter**
- **Sample-and-Hold circuit**
- **Peak detector**

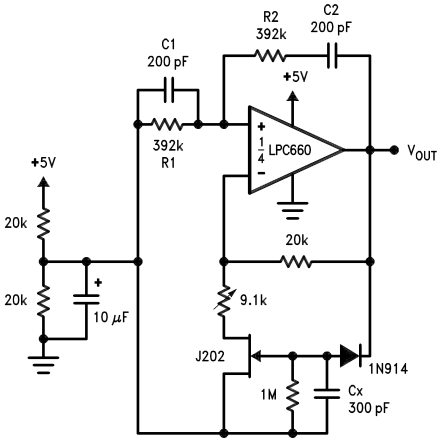
DESCRIPTION

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltages from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Application Circuit



Oscillator frequency is determined by R1, R2, C1, and C2:
$f_{OSC} = 1/2\pi RC$
where R = R1 = R2 and C = C1 = C2.

Figure 1. Sine-Wave Oscillator

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(2)
Output Short Circuit to V^-	(3)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (4)	150°C
ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(4)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Power Supply Pin	35 mA

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.
(3) Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)\theta_{JA}$.

Operating Ratings (1)

Temperature Range	
LPC660AM	−55°C ≤ T_J ≤ +125°C
LPC660AI	−40°C ≤ T_J ≤ +85°C
LPC660I	−40°C ≤ T_J ≤ +85°C
Supply Range	4.75V to 15.5V
Power Dissipation	(2)
Thermal Resistance (θ_{JA}), (3)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SOIC	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
(3) All numbers apply for packages soldered directly into a PC board.

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DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883 Limit (1) (2)	LPC660AI Limit (1)	LPC660I Limit (1)	Units
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				µV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V	94	84	84	74	dB
			82	**83**	**73**	min
Input Common Mode Voltage Range	V^+ = 5V & 15V For CMRR > 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		V^+ − 1.9	V^+ − 2.3	V^+ − 2.3	V^+ − 2.3	V
			V^+ − 2.6	**V^+ − 2.5**	**V^+ − 2.5**	min
Large Signal	R_L = 100 kΩ (3)	1000	400	400	300	V/mV
Voltage Gain	Sourcing		**250**	**300**	**200**	min
	Sinking	500	180	180	90	V/mV
			70	**120**	**70**	min
	R_L = 5 kΩ (3)	1000	200	200	100	V/mV
	Sourcing		**150**	**160**	**80**	min
	Sinking	250	100	100	50	V/mV
			35	**60**	**40**	min

(1) Limits are guaranteed by testing or correlation.
(2) A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.
(3) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

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DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883 Limit (1) (2)	LPC660AI Limit (1)	LPC660I Limit (1)	Units
Output Swing	V^+ = 5V R_L = 100 kΩ to V^+/2	4.987	4.970	4.970	4.940	V
			4.950	**4.950**	**4.910**	min
		0.004	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 5V R_L = 5 kΩ to V^+/2	4.940	4.850	4.850	4.750	V
			4.750	**4.750**	**4.650**	min
		0.040	0.150	0.150	0.250	V
			0.250	**0.250**	**0.350**	max
	V^+ = 15V R_L = 100 kΩ to V^+/2	14.970	14.920	14.920	14.880	V
			14.880	**14.880**	**14.820**	min
		0.007	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 15V R_L = 5 kΩ to V^+/2	14.840	14.680	14.680	14.580	V
			14.600	**14.600**	**14.480**	min
		0.110	0.220	0.220	0.320	V
			0.300	**0.300**	**0.400**	max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA
			12	**14**	**11**	min
	Sinking, V_O = 5V	21	16	16	13	mA
			12	**14**	**11**	min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA
			19	**25**	**20**	min
	Sinking, V_O = 13V (4)	39	19	28	23	mA
			19	**24**	**19**	min
Supply Current	All Four Amplifiers V_O = 1.5V	160	200	200	240	µA
			250	**230**	**270**	max

(4) Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.

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AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM / LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (1) (2)	Limit (1)	Limit (1)	
Slew Rate	(3)	0.11	0.07	0.07	0.05	V/µs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(4)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
Total Harmonic Distortion	F = 1 kHz, A_V = −10 R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

(1) Limits are guaranteed by testing or correlation.
(2) A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.
(3) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred. V^+ = 15V and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

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Typical Performance Characteristics

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Supply Current vs. Supply Voltage

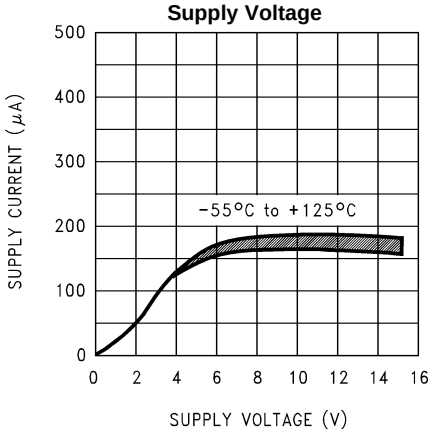


Figure 2.

Input Bias Current vs. Temperature

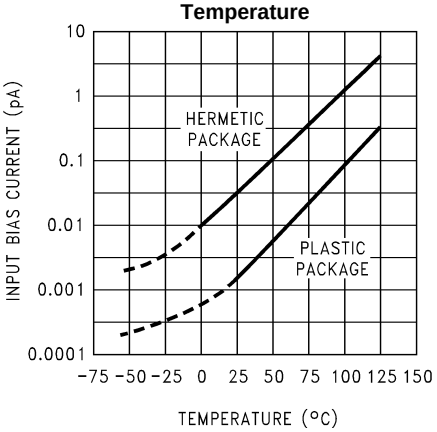


Figure 3.

Common-Mode Voltage Range vs. Temperature

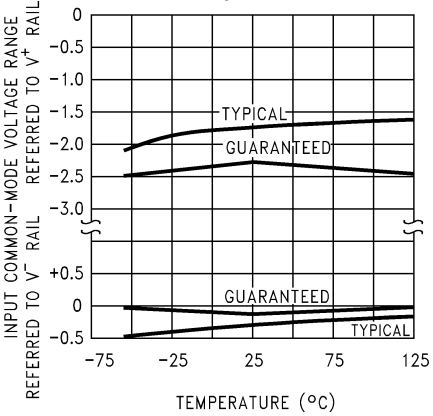


Figure 4.

Output Characteristics Current Sinking

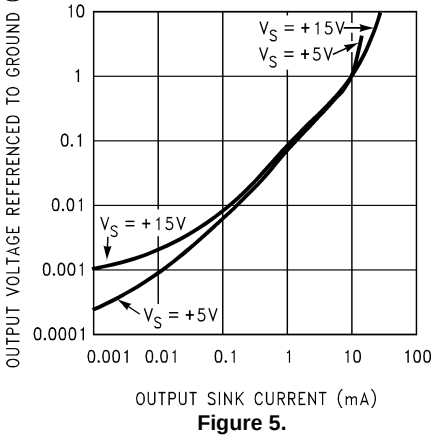


Figure 5.

Output Characteristics Current Sourcing

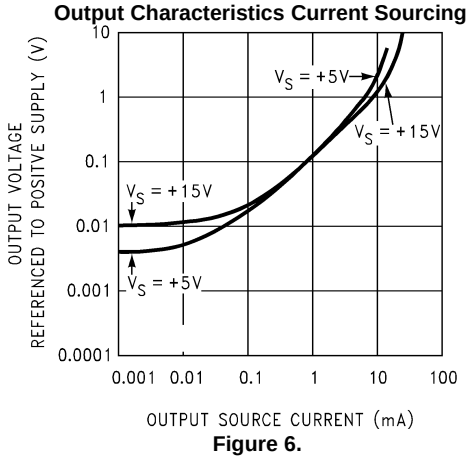


Figure 6.

Input Voltage Noise vs. Frequency

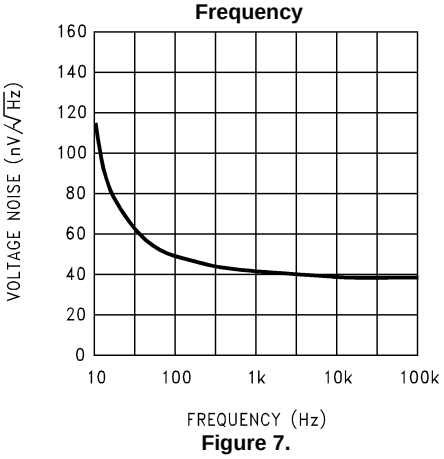


Figure 7.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Crosstalk Rejection vs. Frequency

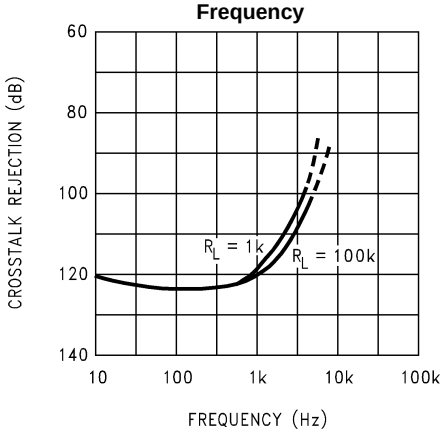


Figure 8.

CMRR vs. Frequency

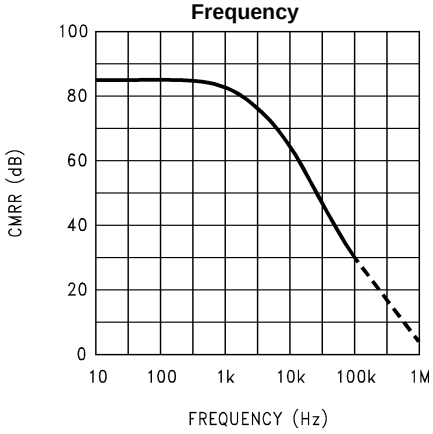


Figure 9.

CMRR vs. Temperature

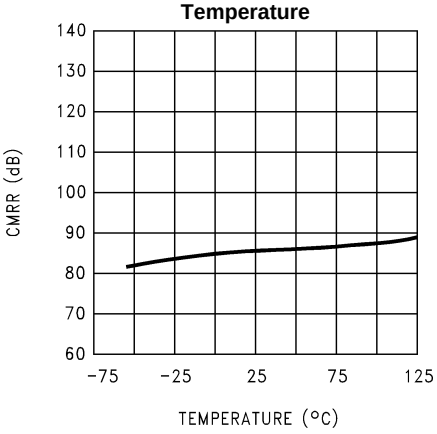


Figure 10.

Power Supply Rejection Ratio vs. Frequency

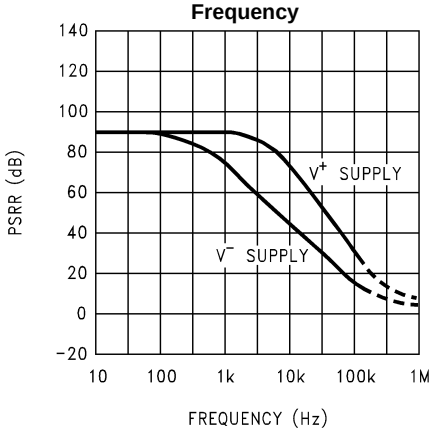


Figure 11.

Open-Loop Voltage Gain vs. Temperature

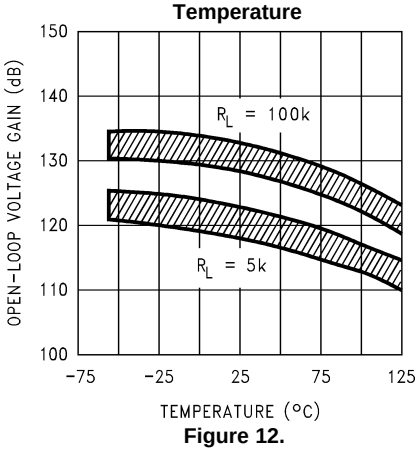


Figure 12.

Open-Loop Frequency Response

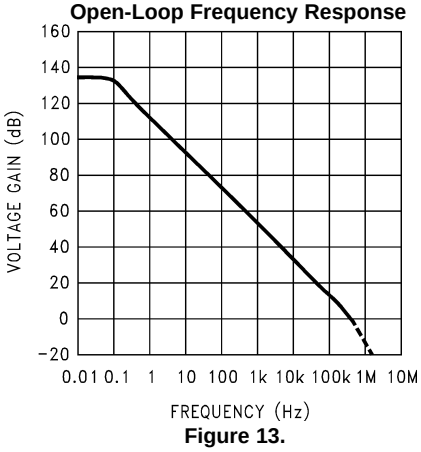


Figure 13.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Gain and Phase Responses vs. Load Capacitance

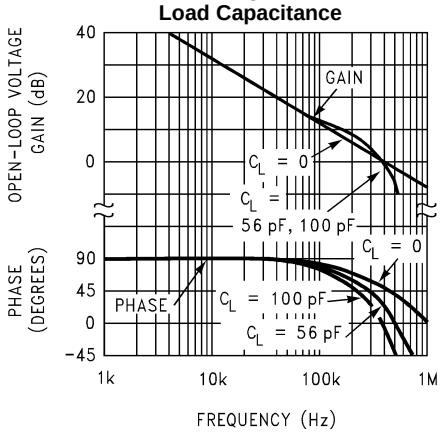


Figure 14.

Gain and Phase Responses vs. Temperature

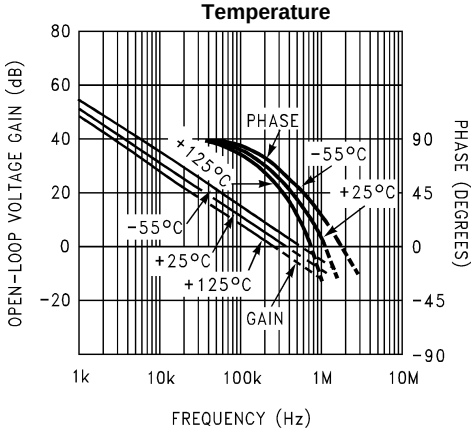


Figure 15.

Gain Error (V_{OS} vs. V_{OUT})

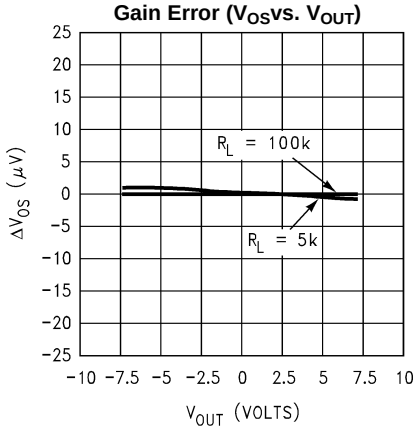


Figure 16.

Non-Inverting Slew Rate vs. Temperature

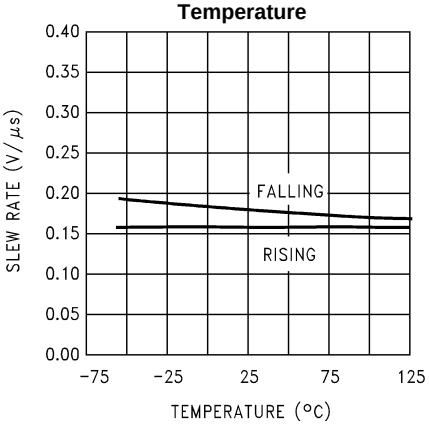


Figure 17.

Inverting Slew Rate vs. Temperature

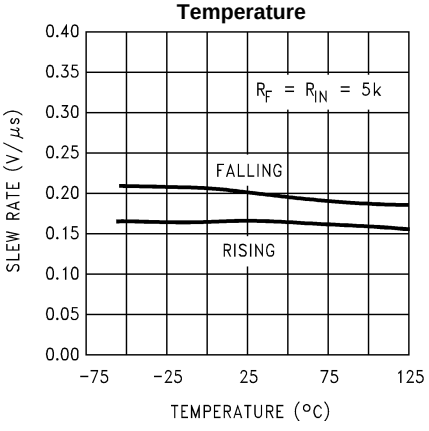


Figure 18.

Large-Signal Pulse Non-Inverting Response (A_V = +1)

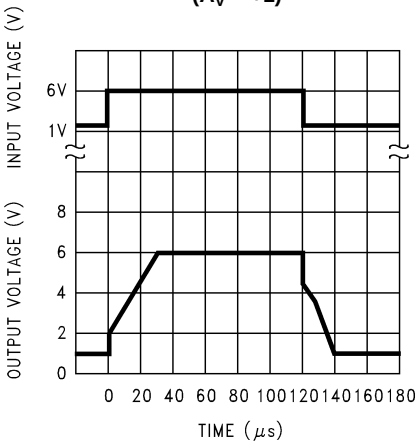


Figure 19.

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Typical Performance Characteristics (continued)

V_S = ±7.5V, T_A = 25°C unless otherwise specified

Non-Inverting Small Signal Pulse Response
(A_V = +1)

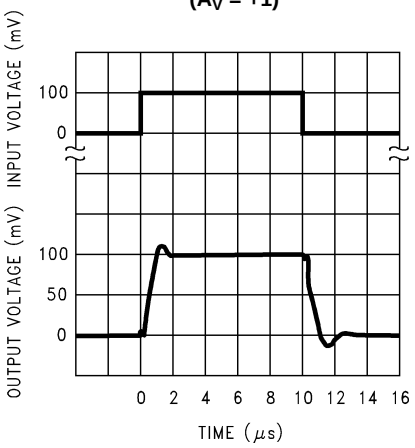


Figure 20.

Inverting Large-Signal Pulse Response

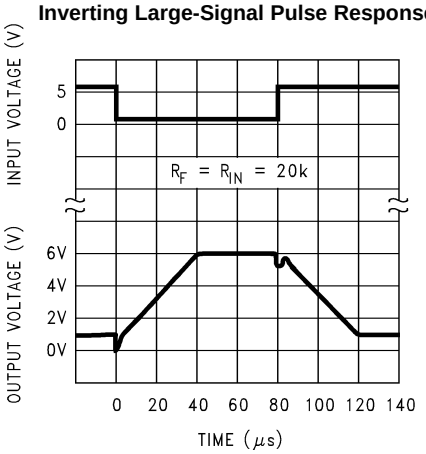


Figure 21.

Inverting Small-Signal Pulse Response

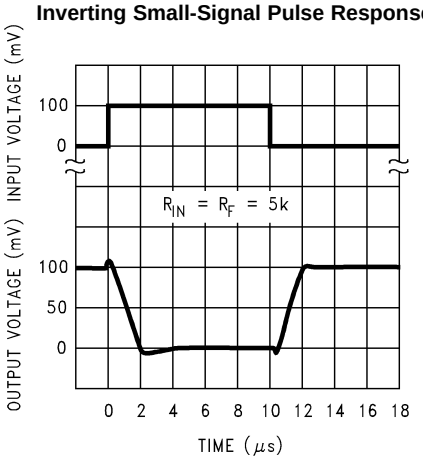
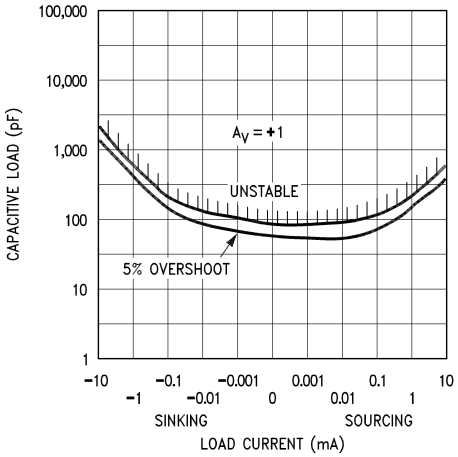


Figure 22.

Stability vs. Capacitive Load



Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Figure 23.

Stability vs. Capacitive Load

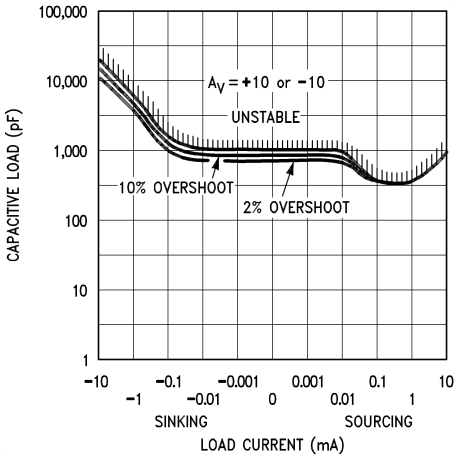


Figure 24.

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Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

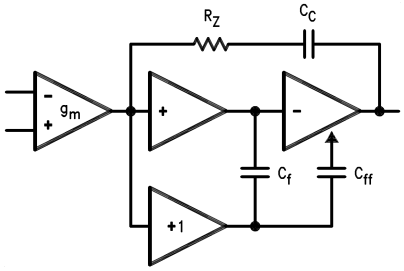


Figure 25. LPC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 kΩ. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 kΩ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

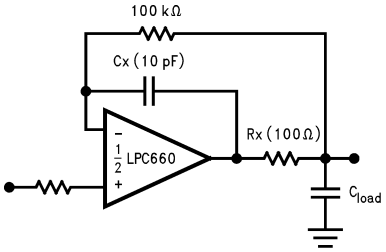


Figure 26. Rx, Cx Improve Capacitive Load Tolerance

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Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 27). Typically a pull up resistor conducting 50 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

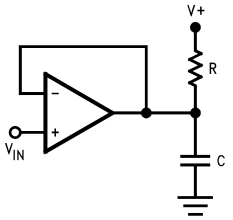


Figure 27. Compensating for LargeCapacitive Loads with A Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 28. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figure 29*a*, Figure 30*b*, Figure 31*c* for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 32*d*.

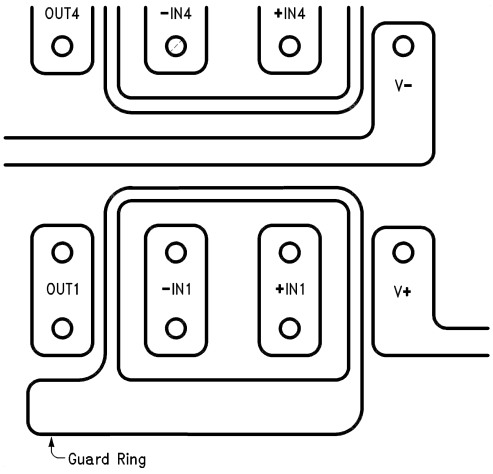


Figure 28. Example of Guard Ring in P.C. Board Layout using the LPC660

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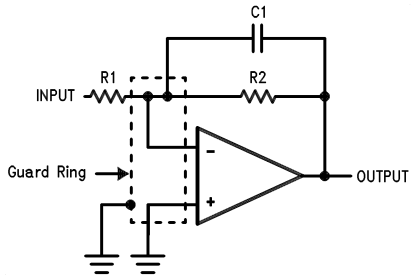


Figure 29. (a) Inverting Amplifier

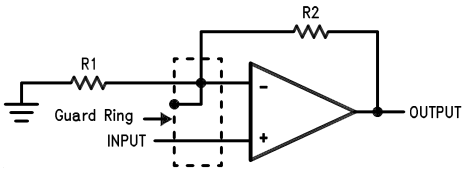


Figure 30. (b) Non-Inverting Amplifier

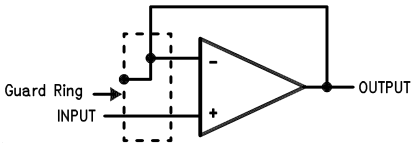


Figure 31. (c) Follower

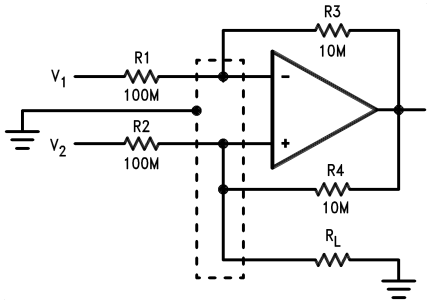
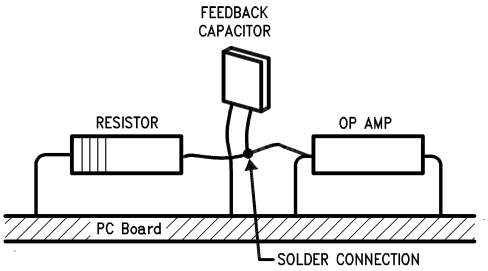


Figure 32. (d) Howland Current Pump

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 33.

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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

Figure 33. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 34 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2. \quad (1)$$

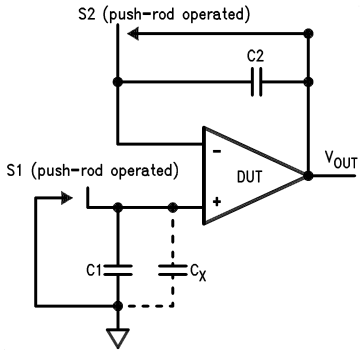


Figure 34. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

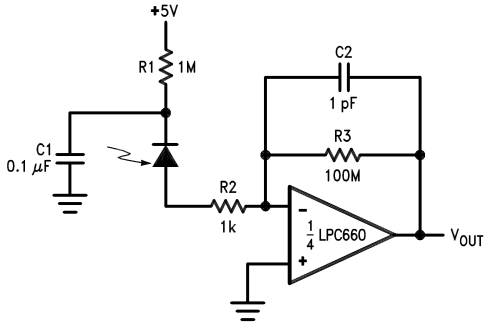
$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_X) \quad (2)$$

where C_X is the stray capacitance at the + input.

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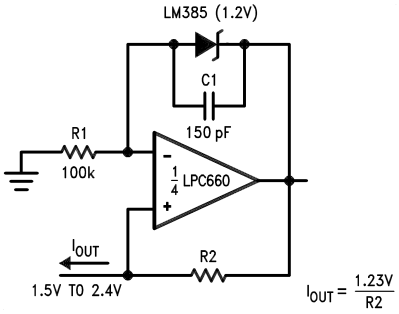
Typical Single-Supply Applications — (V^+ = 5.0 V_{DC})

Figure 35. Photodiode Current-to-Voltage Converter



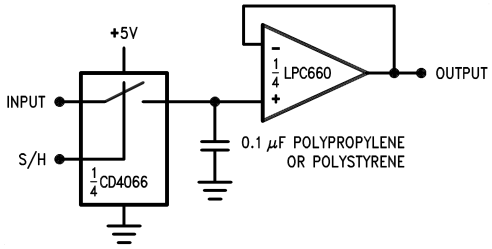
Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Figure 36. Micropower Current Source



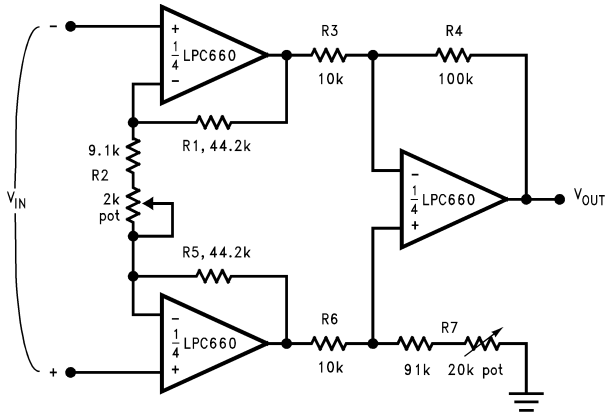
Note: (Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Figure 37. Low-Leakage Sample-and-Hold



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Figure 38. Instrumentation Amplifier



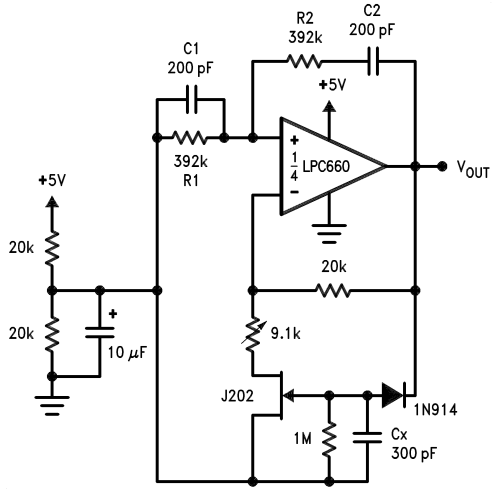
If R1 = R5, R3 = R6, and R4 = R7;

then $\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R1} \times \frac{R4}{R3}$

$\therefore A_V \approx 100$ for circuits shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Figure 39. Sine-Wave Oscillator

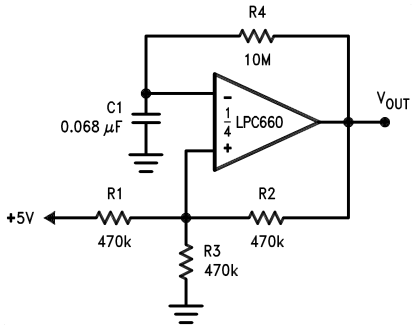


Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

Figure 40. 1 Hz Square-Wave Oscillator



This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

Figure 41. Power Amplifier

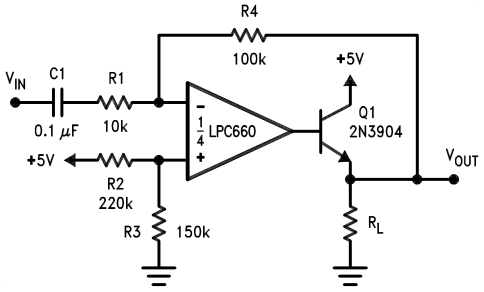
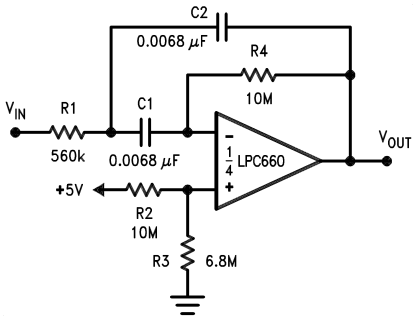
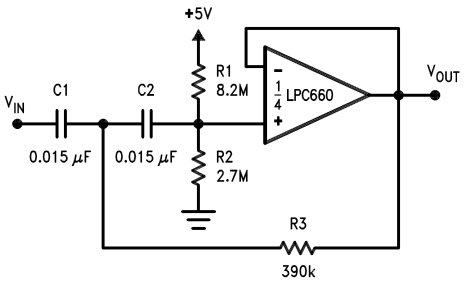


Figure 42. 10 Hz Bandpass Filter



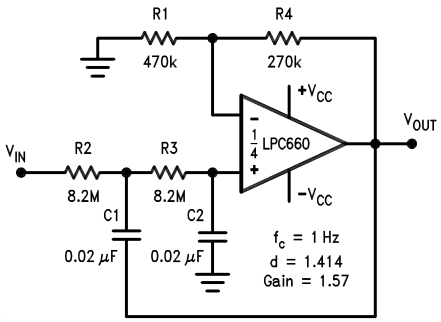
f_O = 10 Hz
Q = 2.1
Gain = −8.8

Figure 43. 10 Hz High-Pass Filter (2 dB Dip)



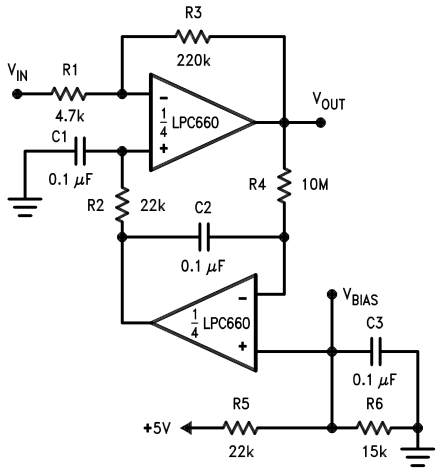
f_c = 10 Hz
d = 0.895
Gain = 1

Figure 44. 1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



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Figure 45. High Gain Amplifier with Offset Voltage Reduction



Gain = −46.8
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS}.

Connection Diagram

Top View

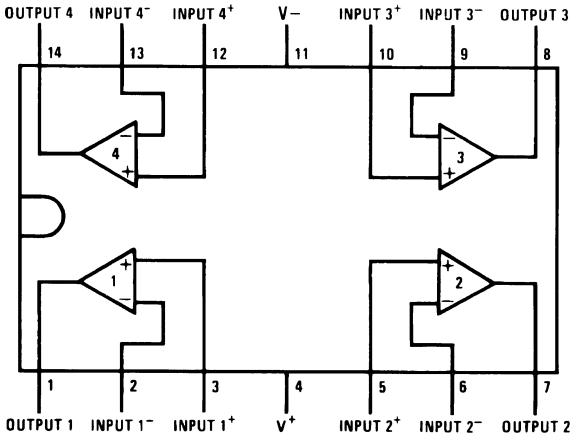


Figure 46. 14-Pin SOIC Package
See Package Number D0014A

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	17

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPC660AIM/NOPB	LIFEBUY	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM	
LPC660AIMX/NOPB	LIFEBUY	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPC660AIM	
LPC660IM/NOPB	LIFEBUY	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM	
LPC660IMX/NOPB	LIFEBUY	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LPC660IM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

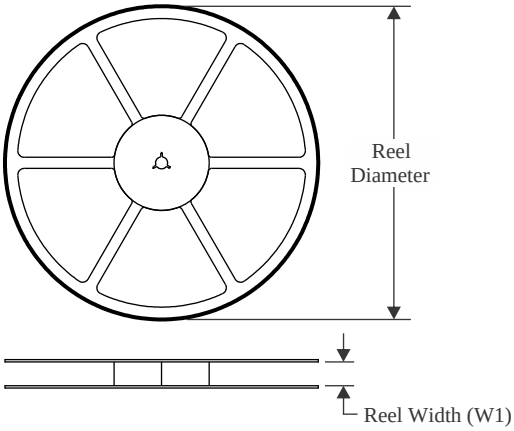
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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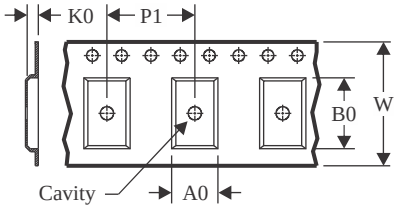
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

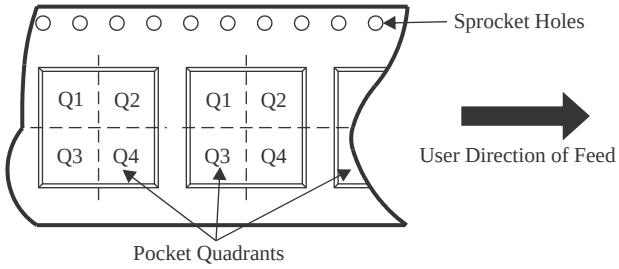


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

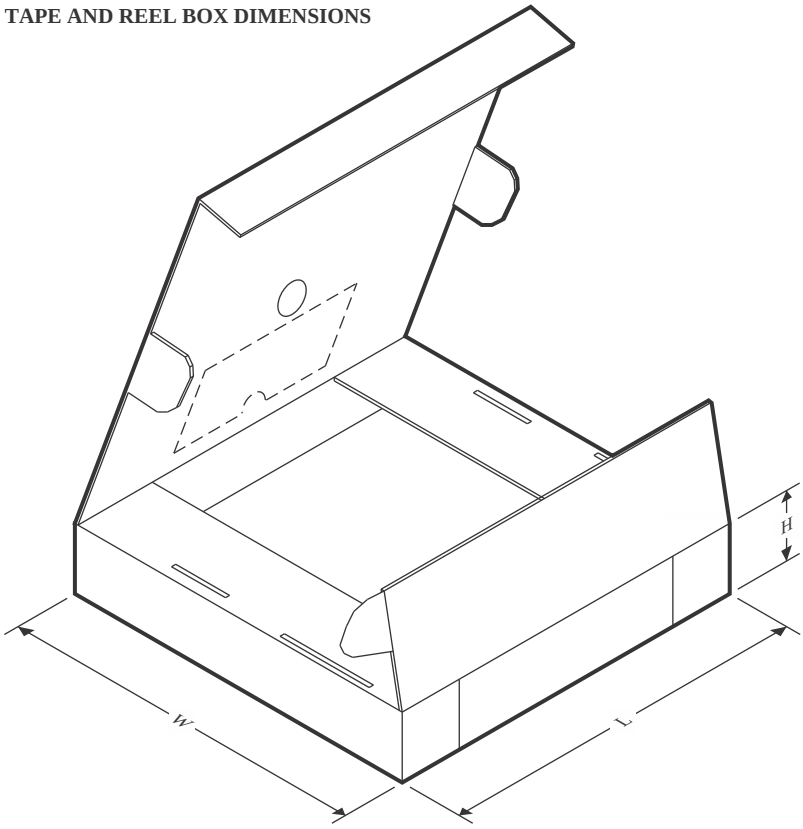
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPC660AIMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LPC660IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

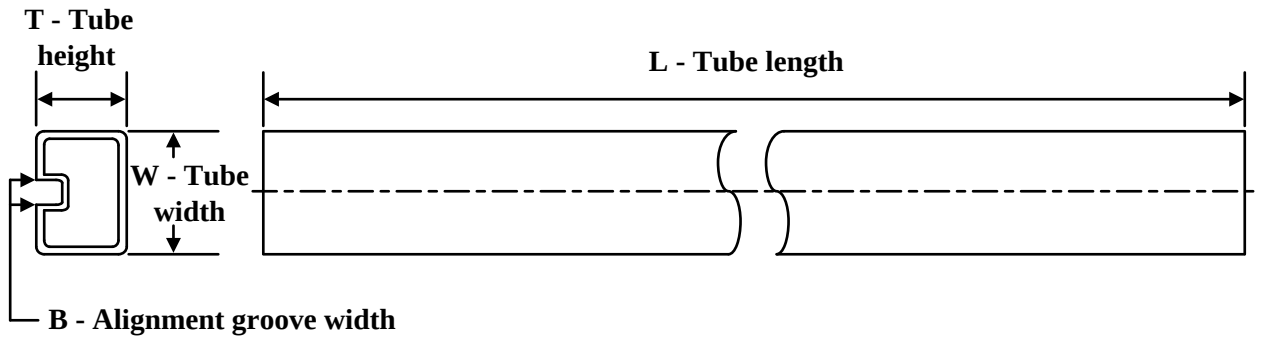
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPC660AIMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LPC660IMX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

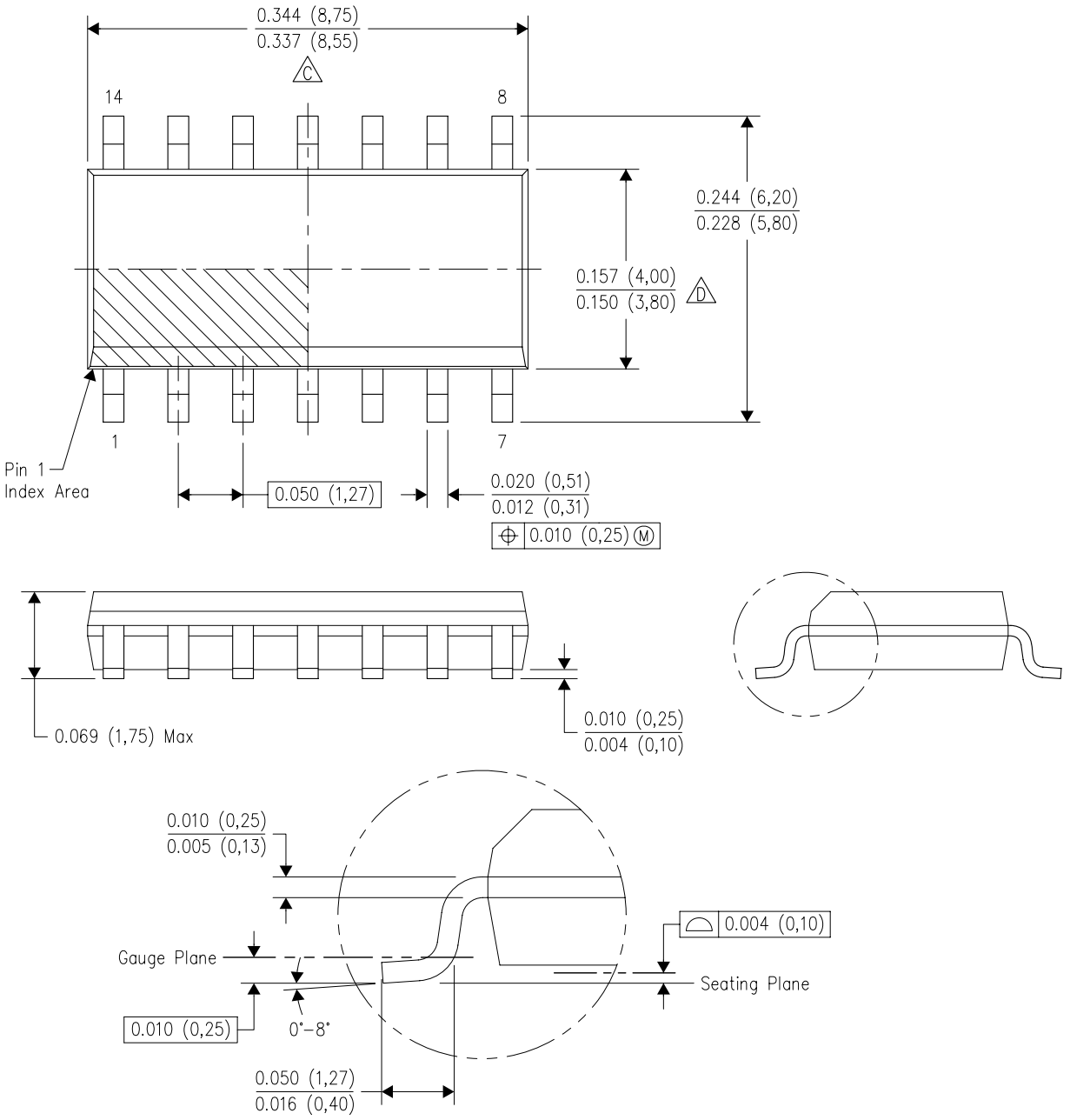
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LPC660AIM/NOPB	D	SOIC	14	55	495	8	4064	3.05
LPC660IM/NOPB	D	SOIC	14	55	495	8	4064	3.05

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

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