

SN5476, SN54LS76A
SN7476, SN74LS76A
DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR
SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

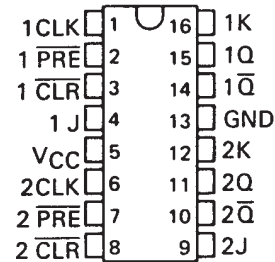
description

The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flip-flop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predicatble operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7476 and the SN74LS76A are characterized for operation from 0°C to 70°C .

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



'76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	\downarrow	L	L	Q ₀	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	TOGGLE

'LS76A
FUNCTION TABLE

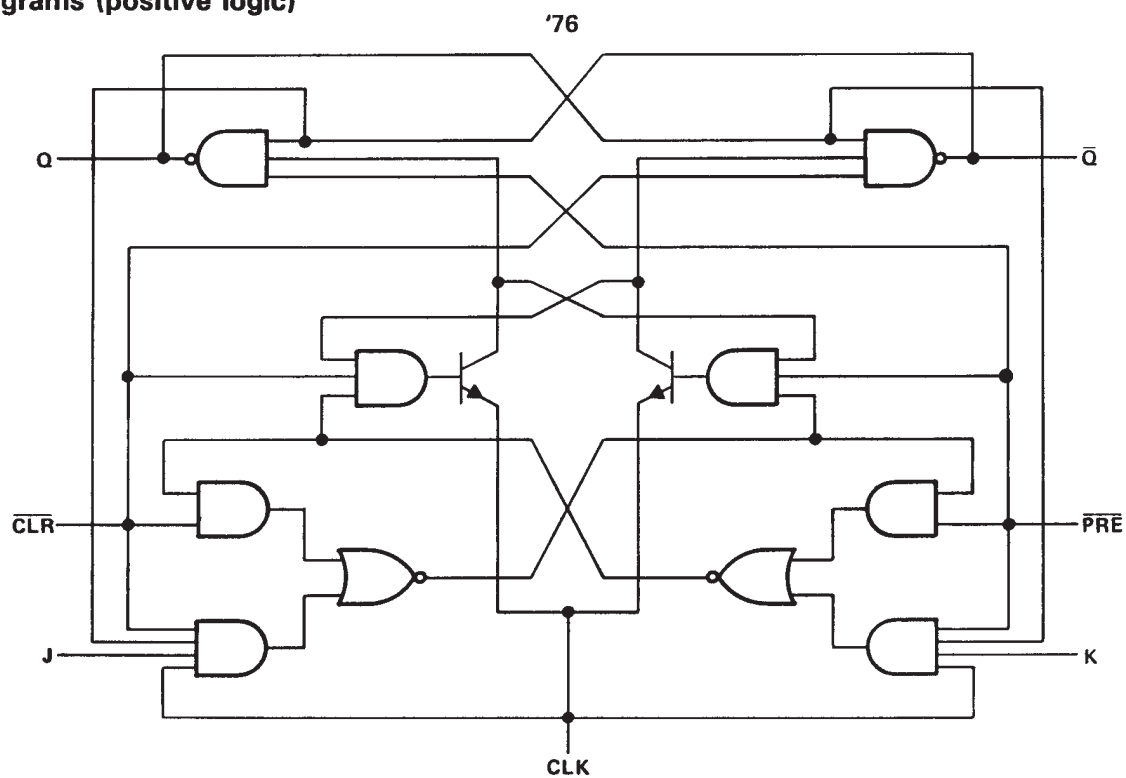
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	\downarrow	L	L	Q ₀	\bar{Q}_0
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\bar{Q}_0

[†] This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

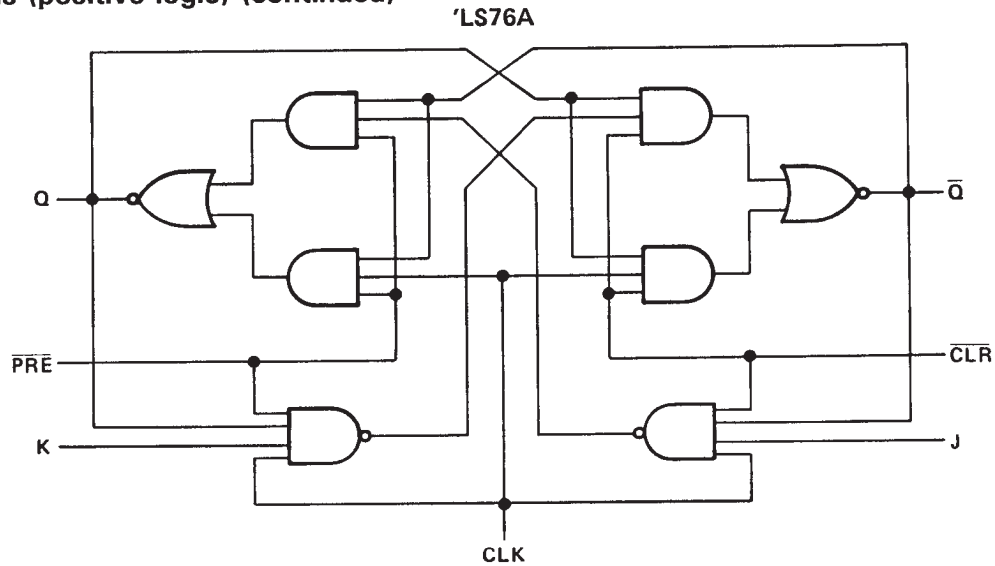
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DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

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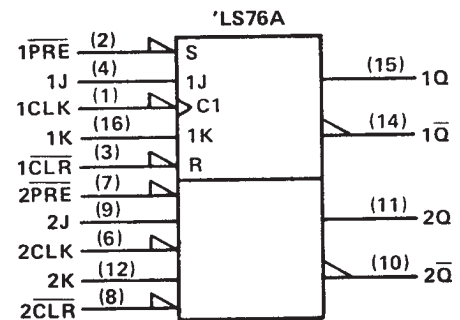
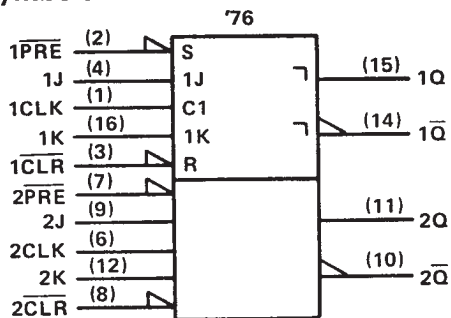
logic diagrams (positive logic)



logic diagrams (positive logic) (continued)

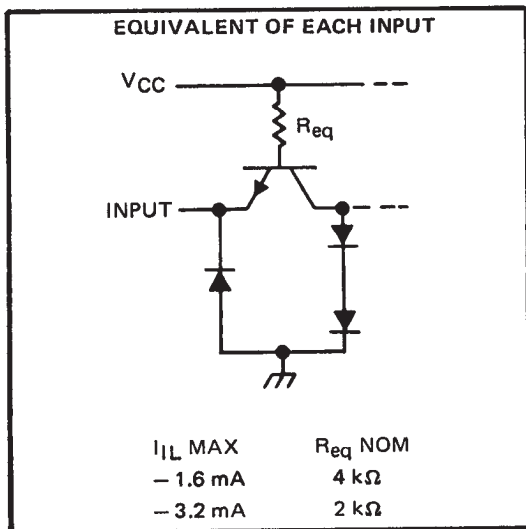


logic symbols†

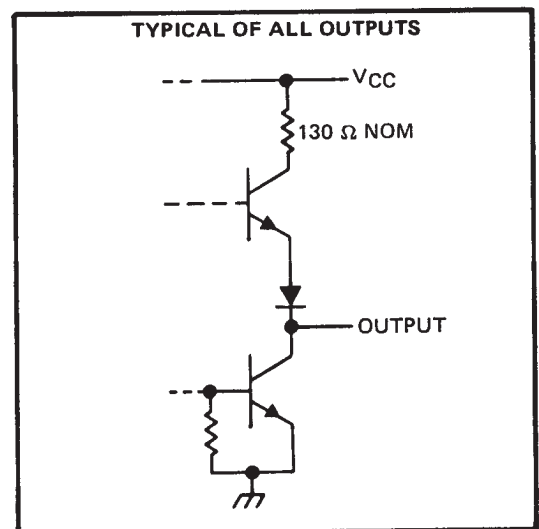


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs

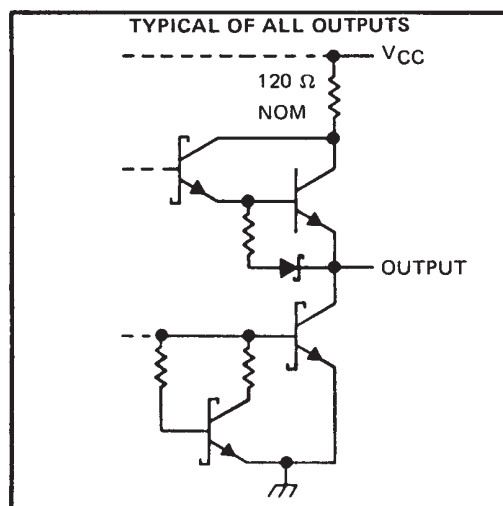


'76



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'LS76A



Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '76	5.5 V
'LS76A	7 V
Operating free-air temperature range: SN54'	–55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5476, SN54LS76A
SN7476, SN74LS76A
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recommended operating conditions

		SN5476			SN7476			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			– 0.4			– 0.4	mA
I _{OL}	Low-level output current			16			16	mA
t _w	Pulse duration		CLK high	20		20		ns
			CLK low	47		47		
			PRE or CLR low	25		25		
t _{su}	Input setup time before CLK ↑	0			0			ns
t _h	Input hold time-data after CLK ↓	0			0			ns
T _A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5476			SN7476			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}		V _{CC} = MIN, I _I = – 12 mA				– 1.5			– 1.5	V
V _{OH}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = – 0.4 mA		2.4	3.4		2.4	3.4		V
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I _I		V _{CC} = MAX, V _I = 5.5 V				1			1	mA
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.4 V				40			40	μA
	All other					80			80	
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V				– 1.6			– 1.6	mA
	All other¶					– 3.2			– 3.2	
I _{OS} §		V _{CC} = MAX		– 20		– 57	– 18		– 57	mA
I _{CC} #		V _{CC} = MAX, See Note 2			10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

¶ Clear is tested with preset high and preset is tested with clear high.

Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 400 Ω, C _L = 15 pF	15	20		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$			16	25	ns
t _{PHL}					25	40	ns
t _{PLH}	CLK	Q or $\overline{\text{Q}}$			16	25	ns
t _{PHL}					25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5476, SN54LS76A SN7476, SN74LS76A DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

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recommended operating conditions

			SN54LS76A			SN74LS76A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.7			0.8			V
I _{OH}	High-level output current		− 0.4			− 0.4			mA
I _{OL}	Low-level output current		4			8			mA
f _{clock}	Clock frequency		0	30		0	30		MHz
t _w	Pulse duration	CLK high	20			20			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	25			25			
t _{su}	Setup time before CLK↓	data high or low	20			20			ns
		$\overline{\text{CLR}}$ inactive	20			20			
		$\overline{\text{PRE}}$ inactive	25			25			
t _h	Hold time-data after CLK↓		0			0			ns
T _A	Operating free-air temperature		− 55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS76A		SN74LS76A		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN,	I _I = − 18 mA	− 1.5		− 1.5		V
V _{OH}		V _{CC} = MIN,	V _{IH} = 2 V, V _{IL} = MAX, I _{OH} = − 0.4 mA	2.5	3.4	2.7	3.4	V
V _{OL}		V _{CC} = MIN,	V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 4 mA	0.25 0.4		0.25 0.4		V
		V _{CC} = MIN,	V _{IL} = MAX, V _{IH} = 2 V, I _{OL} = 8 mA			0.35 0.5		
I _I	J or K	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
	CLR or PRE			0.3		0.3		
	CLK			0.4		0.4		
I _{IH}	J or K	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
	CLR or PRE			60		60		
	CLK			80		80		
I _{IL}	J or K	V _{CC} = MAX, V _I = 0.4 V		− 0.4		− 0.4		mA
	All other			− 0.8		− 0.8		
I _{OS} §		V _{CC} = MAX,	See Note 4	− 20	− 100	− 20	− 100	mA
I _{CC} (Total)		V _{CC} = MAX,	See Note 2	4 6		4 6		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			R _L = 2 kΩ, C _L = 15 pF	30	45		MHz
t _{PLH}	PRE, CLR or CLK	Q or \bar{Q}			15	20	ns
t _{PHL}					15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9557501QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J
5962-9557501QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W
5962-9557501QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W
7601301EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ
7601301EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ
JM38510/00204BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 00204BEA
JM38510/00204BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 00204BEA
SN5476J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5476J
SN5476J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN5476J
SN54LS76AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS76AJ
SN54LS76AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS76AJ
SNJ5476J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J
SNJ5476J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QE A SNJ5476J
SNJ5476W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W
SNJ5476W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9557501QF A SNJ5476W

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS76AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ
SNJ54LS76AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7601301EA SNJ54LS76AJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9557501QFA	W	CFP	16	25	506.98	26.16	6220	NA
SNJ5476W	W	CFP	16	25	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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