SN65LBC172A, SN75LBC172A Quadruple RS-485 Differential Line Drivers

1 Features

- Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 applications
- Signaling Rates† up to 30Mbps
- Propagation delay times <11 ns
- Low standby power consumption 1.5mA max
- Output ESD protection 12 kV
- Driver positive- and negative-current limiting
- Power-up and power-down glitch-free for live insertion applications
- Thermal shutdown protection
- Industry standard pin-out, compatible with SN75172, AM26LS31, DS96172, LTC486, and MAX3045

2 Applications

- Motor drives
- Factory automation and control

3 Description

The SN65LBC172A and SN75LBC172A are quadruple differential line drivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

These devices are optimized for balanced multipoint bus transmission at signaling rates up to 30 million bits per second. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed mulitpoint data transmission applications in noisy environments. These devices are designed using LinBiCMOS, facilitating low power consumption and robustness.

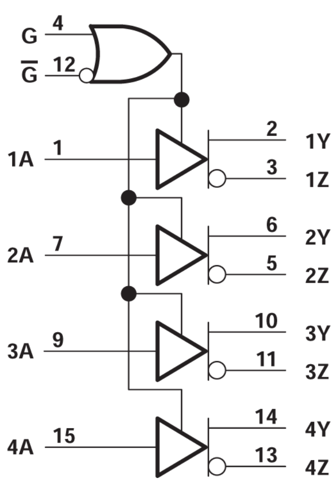
The G and $\overline{G}$ inputs provide driver enable control using either positive or negative logic. When disabled or powered off, the driver outputs present a high-impedance to the bus for reduced system loading.

The SN75LBC172A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC172A is characterized over the temperature range from –40°C to 85°C.

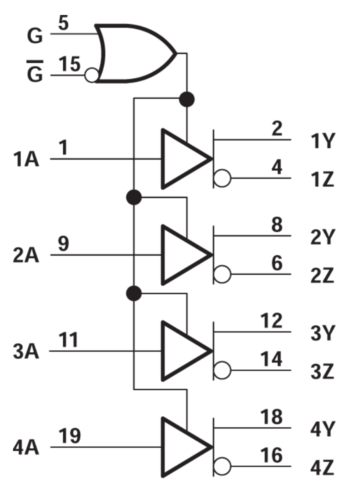
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN65LBC172A SN75LBC172A	SOIC (DW, 16)	10.3mm × 10.3mm
	SOIC (DW, 20)	12.8mm × 10.3mm
	PDIP (N, 16)	19.3mm × 9.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



Logic Diagram (Positive Logic)

† The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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4 Pin Configuration and Functions

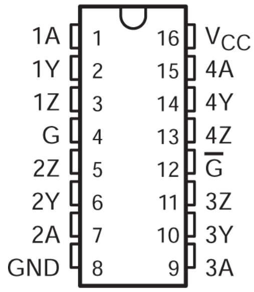


Figure 4-1. N Package (Top View)

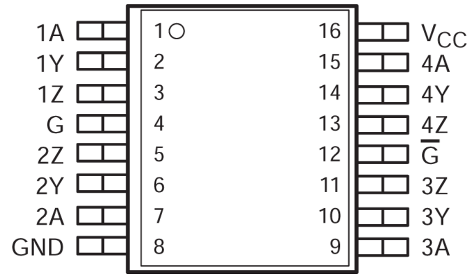


Figure 4-2. 16-DW Package (Top View)

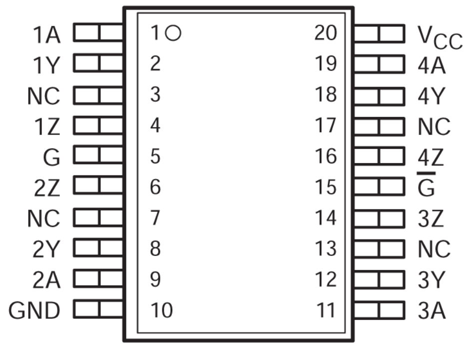


Figure 4-3. 20-DW Package (Top View)

5 Specifications

5.1 Absolute Maximum Ratings

See Note (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.3	6	V
V_O	Output voltage range	at any bus (steady state)	−10	15	V
V_O	Output voltage range	at any bus (transient pulse through 100Ω, see Figure 6-8)	−30	30	V
V_I	Input voltage range	at any A, G, or $\overline{G}$ terminal	−0.5	V_{CC} + 0.5	V
T_{stg}	Storage temperature range		−65	150	°C
P_D	Continuous power dissipation		See Dissipation Rating Table		
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	Y, Z, and GND	±12000	V
			All pins	±5000	
		Charged device model (CDM), per AEC Q100-011(2)	All pins	±1000	

(1) Tested in accordance with JEDEC standard 22, Test Method A114−A.
(2) Tested in accordance with JEDEC standard 22, Test Method C101.

5.3 Dissipation Rating Table

PACKAGE	JEDEC BOARD MODEL	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
16-PIN DW	Low K	1200mW	9.6mW/°C	769mW	625mW
	High K	2240mW	17.9mW/°C	1434mW	1165mW
20-PIN DW	Low K	1483mW	11.86mW/°C	949mW	771mW
	High K	2753mW	22mW/°C	1762mW	1432mW
16-PIN N	Low K	1150mW	9.2mW/°C	736mW	598mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.

5.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	−7		12	V
High-level input voltage, V_{IH}	A, G, $\overline{G}$	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Output current		−60		60	mA
Operating free-air temperature, T_A	SN75LBC172A	0		70	°C
	SN65LBC172A	−40		85	

5.5 Thermal Information

THERMAL METRIC[1]		N (PDIP) 16 PINS	DW (SOIC) 16 PINS	DW (SOIC) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	71.1	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	37.4	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	36.8	39.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.5	13.3	8.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.3	36.4	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −18mA		−1.5	−0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude[2]	No load (open circuit)		3		V_{CC}	V
		R_L = 54Ω, see Figure 6-1		1	1.6	2.5	
		With common-mode loading, see Figure 6-2		1	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See Figure 6-1		−0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 6-3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 6-3		−0.02		0.02	V
I_I	Input current	A, G, $\overline{G}$		−50		50	µA
I_{OS}	Short-circuit output current	V_{TEST} = −7V to 12V, See Figure 6-7	V_I = 0V	−200		200	mA
			V_I = V_{CC}				
I_{OZ}	High-impedance-state output current		G at 0V, $\overline{G}$ at V_{CC}	−50		50	µA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0V	−10		10	
I_{CC}	Supply current	V_I = 0V or V_{CC}, No load	All drivers enabled			23	mA
			All drivers disabled			1.5	

(1) All typical values are at V_{CC} = 5V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly of lower output signal into account in determining the maximum signal transmission distance.

5.7 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 54Ω, C_L = 50pF, see Figure 6-4	5.5	8	11	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.5	8	11	ns
t_r	Differential output voltage rise time		2	7.5	11	ns
t_f	Differential output voltage fall time		2	7.5	11	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} – t_{PHL} \rvert$			0.6	2	ns
$t_{sk(o)}$	Output skew(1)				2	ns
$t_{sk(pp)}$	Part-to-part skew(2)				3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 6-5			25	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance				25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 6-6			30	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.8 Typical Characteristics

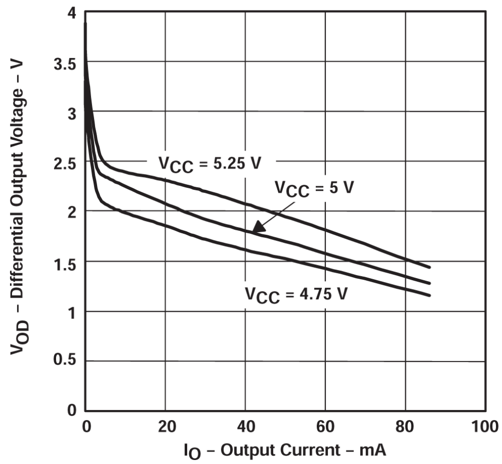


Figure 5-1. Differential Output Voltage vs Output Current

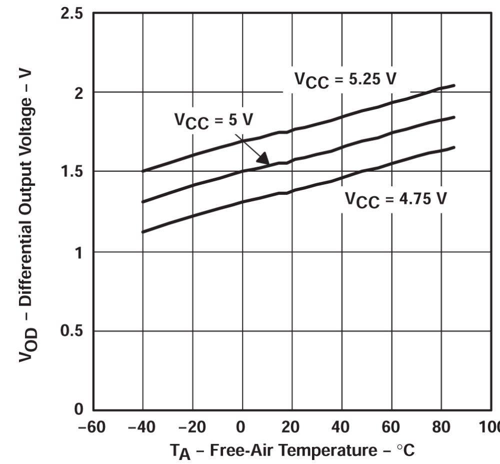


Figure 5-2. Differential Output Voltage vs Free-air Temperature

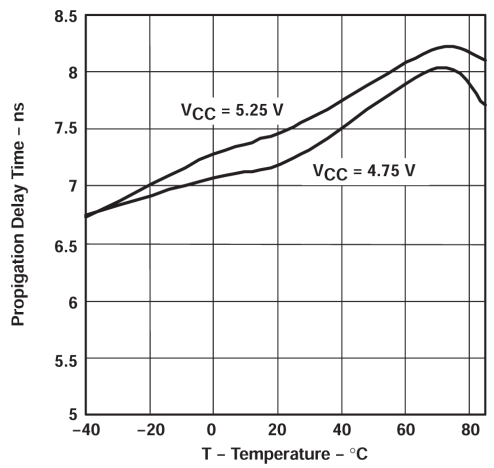


Figure 5-3. Propagation Delay Time vs Temperature

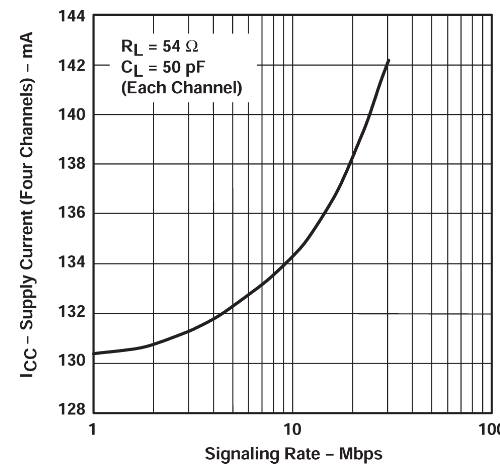


Figure 5-4. Supply Current (Four Channels) vs Signaling Rate

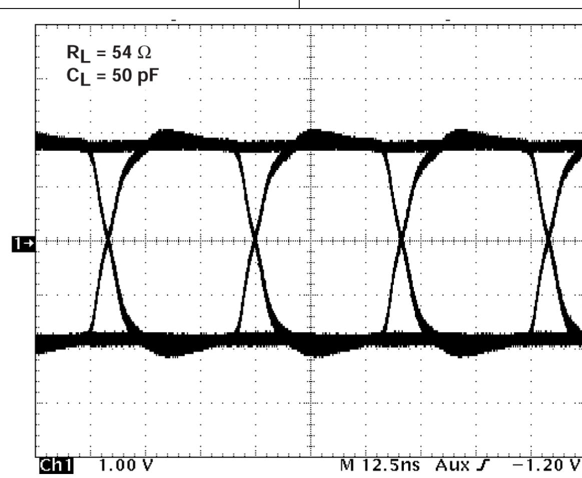


Figure 5-5. Eye Pattern, Pseudorandom Data at 30Mbps

6 Parameter Measurement Information

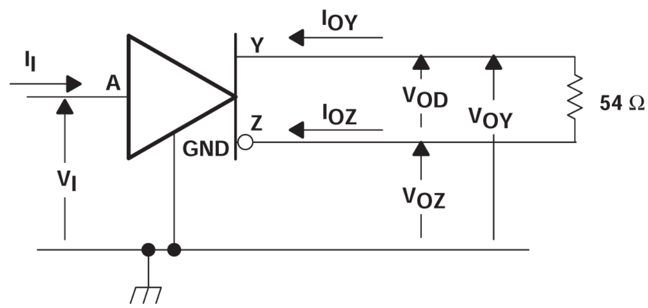


Figure 6-1. Test Circuit, V_{OD} Without Common-Mode Loading

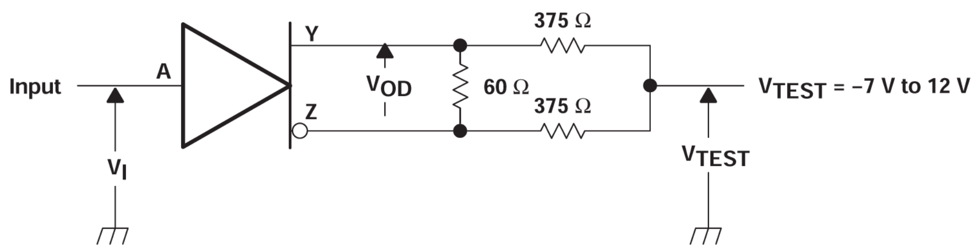


Figure 6-2. Test Circuit, V_{OD} With Common-Mode Loading

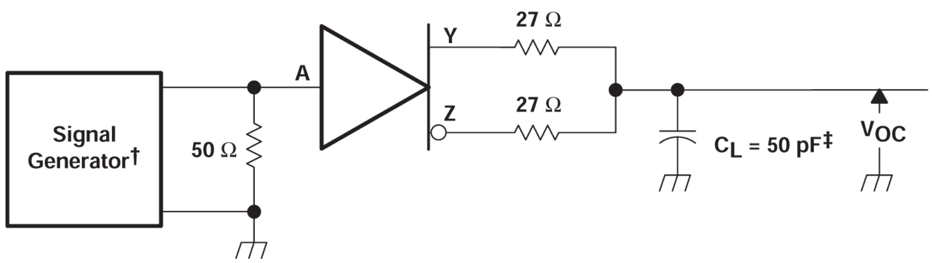
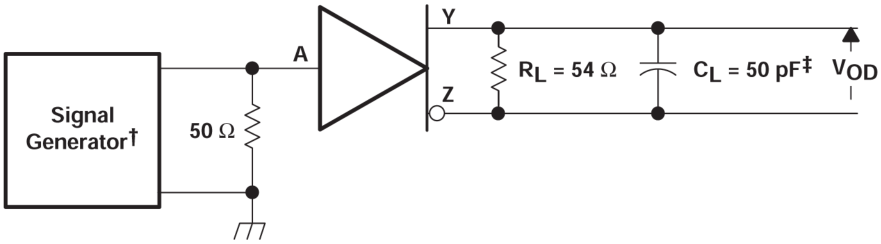


Figure 6-3. V_{OC} Test Circuit



† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

‡ Includes probe and jig capacitance

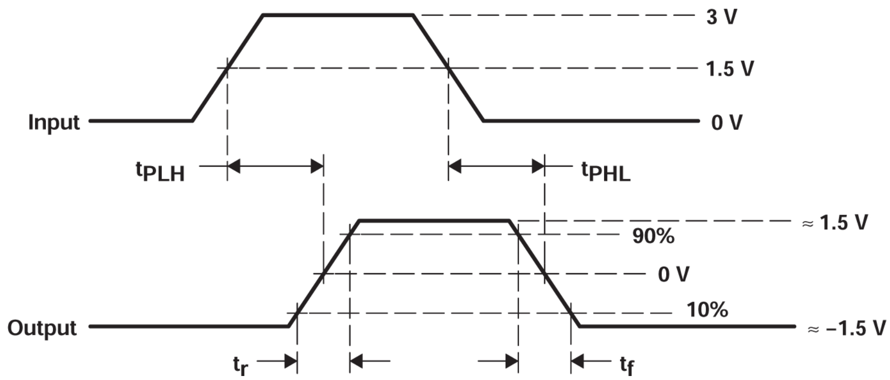
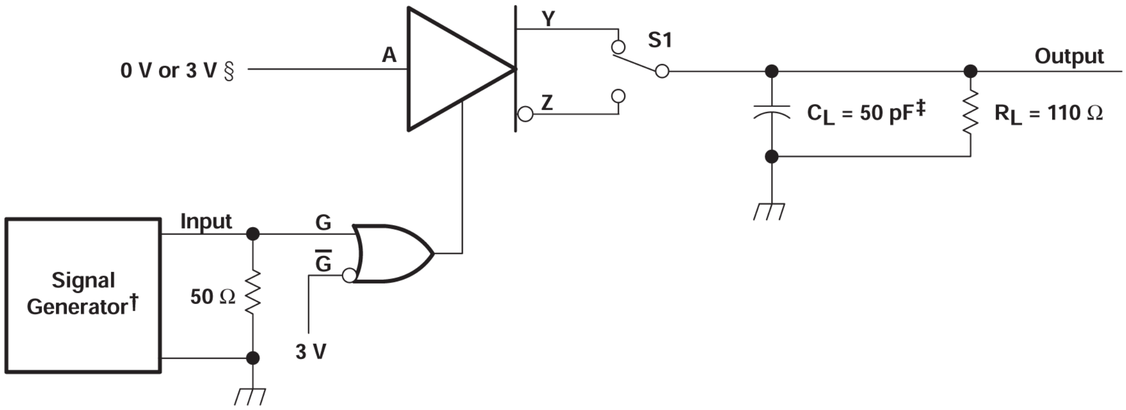


Figure 6-4. Output Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3-V if testing Y output, 0 V if testing Z output

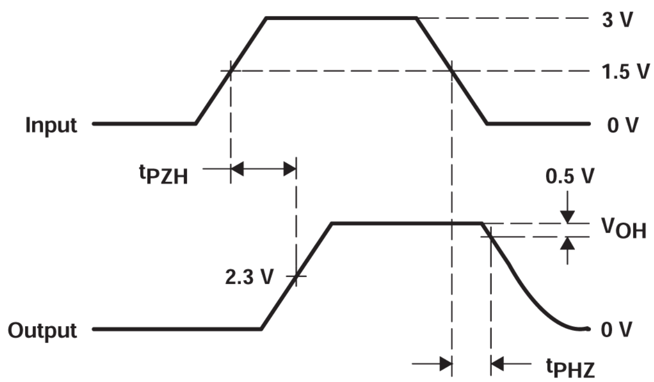
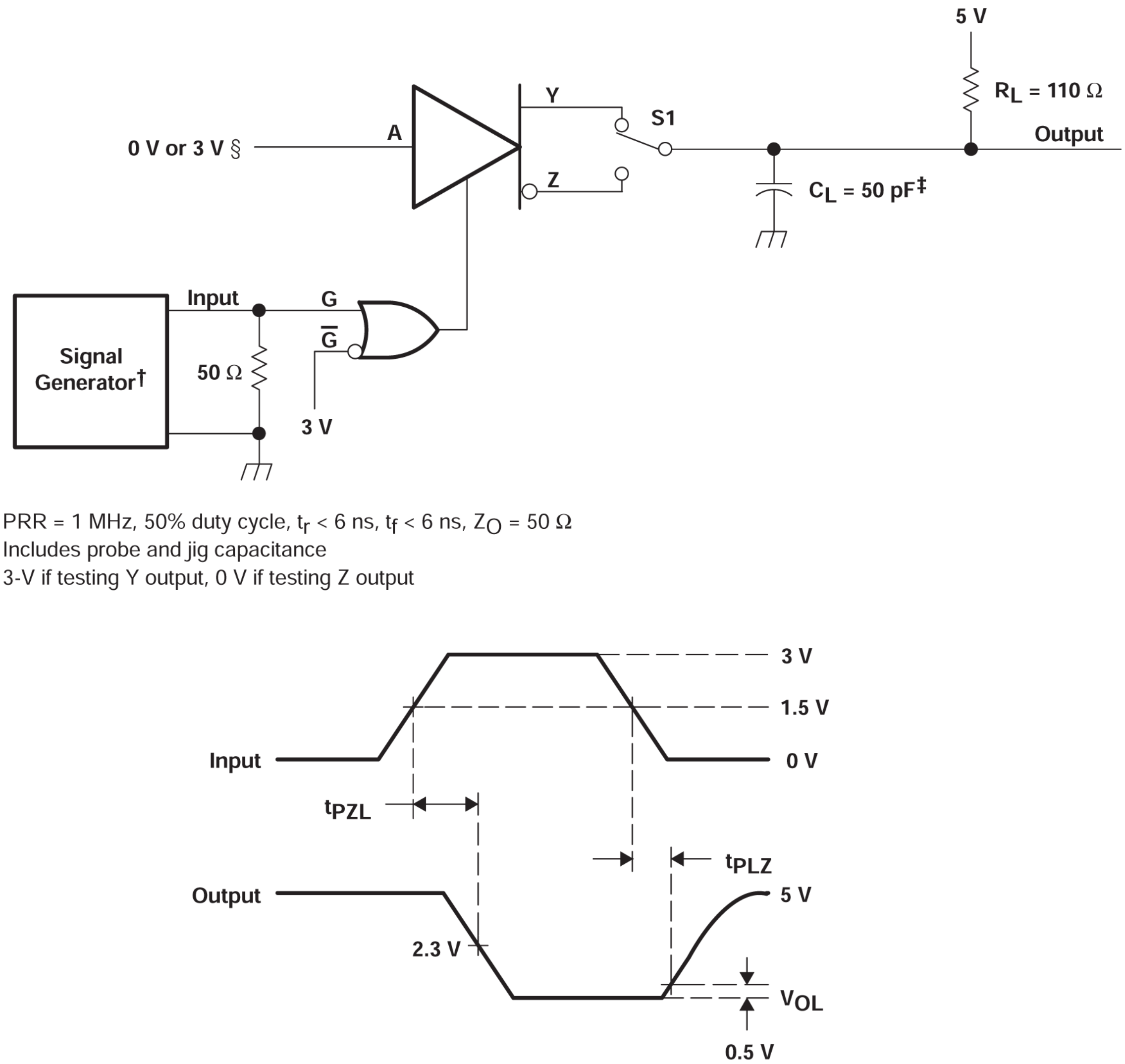


Figure 6-5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}



† PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3-V if testing Y output, 0 V if testing Z output

Figure 6-6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

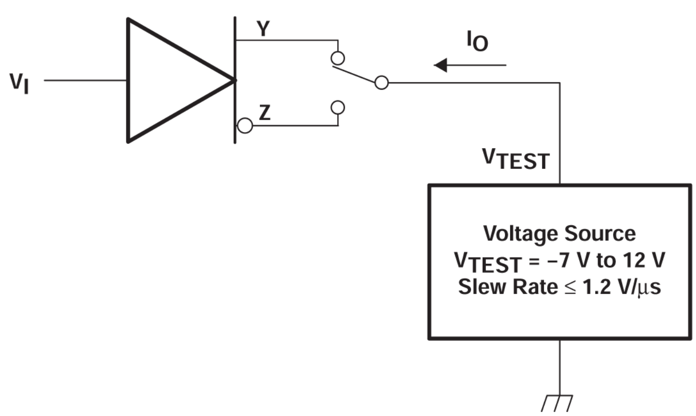


Figure 6-7. Test Circuit, Short-Circuit Output Current

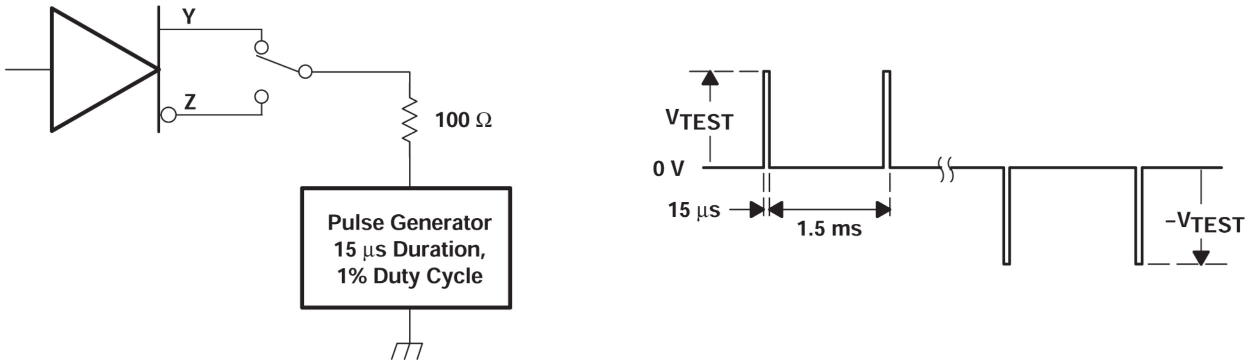


Figure 6-8. Test Circuit and Waveform, Transient Over-Voltage

7 Detailed Description

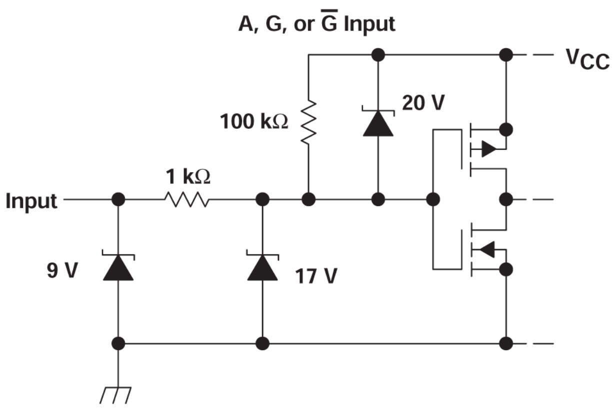
7.1 Device Functional Modes

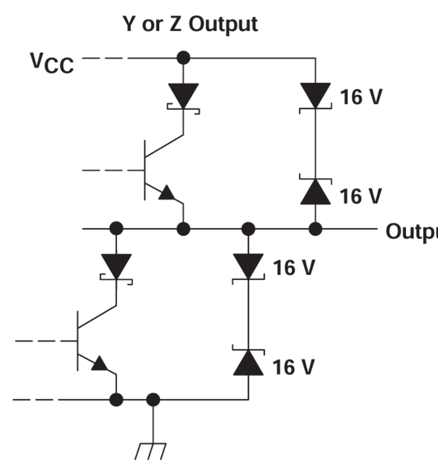
7.1.1 Function Table

Table 7-1. (Each Driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
L	H	X	L	H
L	X	L	L	H
H	H	X	H	L
H	X	L	H	L
OPEN	H	X	H	L
OPEN	X	L	H	L
H	OPEN	X	H	L
L	OPEN	X	L	H
X	L	H	Z	Z
X	L	OPEN	Z	Z

7.1.2 Equivalent Input and Output Schematic Diagrams





8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

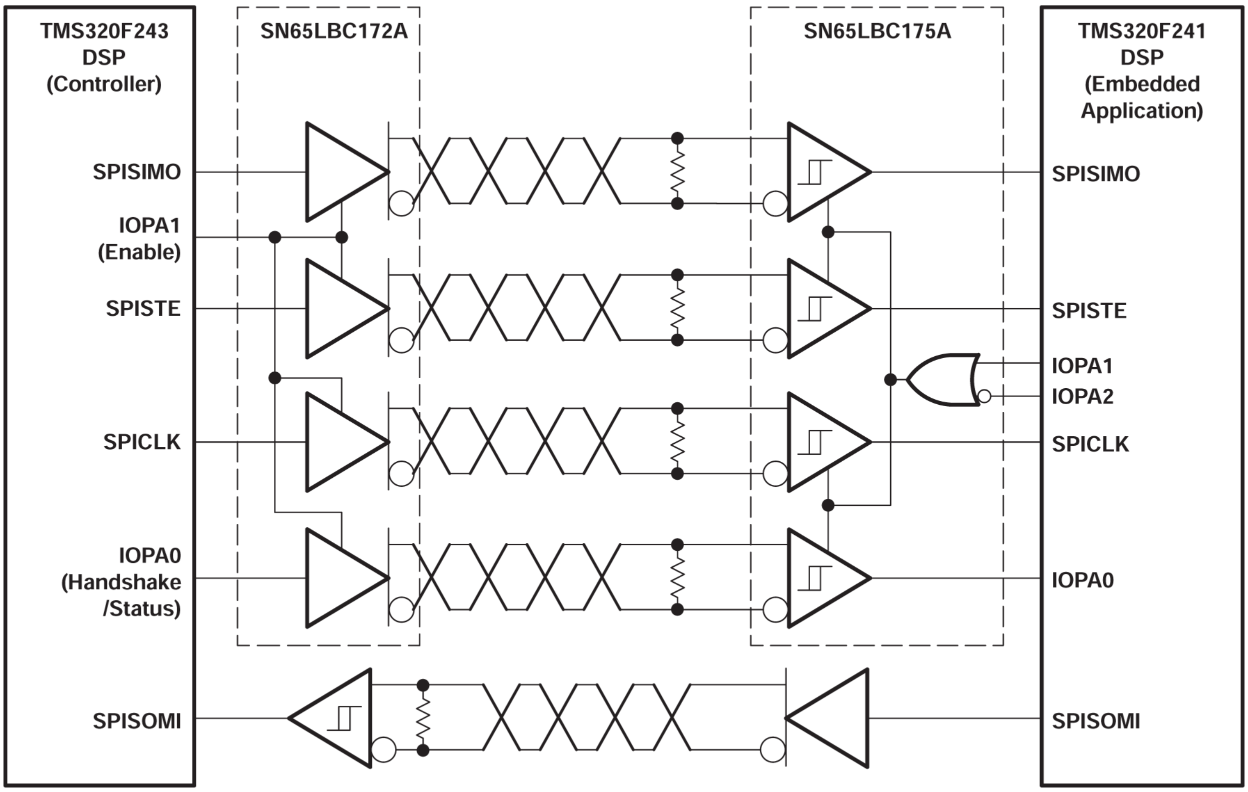


Figure 8-1. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2008) to Revision D (April 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Thermal Information* table	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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