

SN54ALS574B, SN54AS574, SN54AS575 SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS575A and 'AS575 Have Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J, JT) 300-mil DIPs, and Ceramic Flat (W) Packages

description

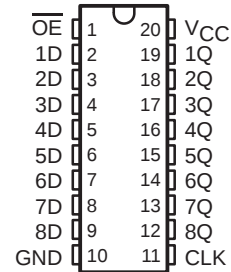
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN74ALS575A, SN54AS575, and SN74AS575 may be synchronously cleared by taking the clear (CLR) input low.

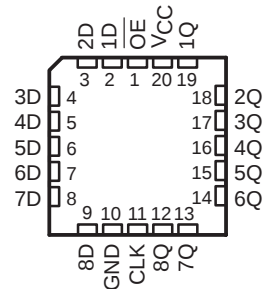
The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS574B, SN54AS574, and SN54AS575 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS574B, SN74ALS575A, SN74AS574, and SN74AS575 are characterized for operation from 0°C to 70°C .

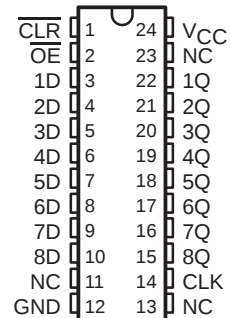
SN54ALS574B, SN54AS574 . . . J OR W PACKAGE
SN74ALS574B, SN74AS574 . . . DW OR N PACKAGE
(TOP VIEW)



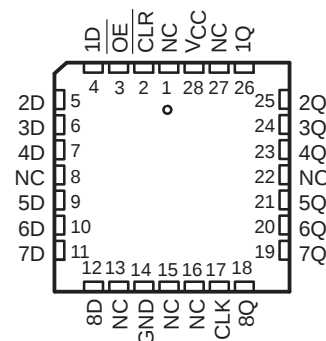
SN54ALS574B, SN54AS574 . . . FK PACKAGE
(TOP VIEW)



SN54AS575 . . . JT OR W PACKAGE
SN74ALS575A, SN74AS575 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS575 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54ALS574B, SN54AS574, SN54AS575 SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

Function Tables

SN54ALS574B, SN74ALS574B, SN54AS574, SN74AS574
(each flip-flop)

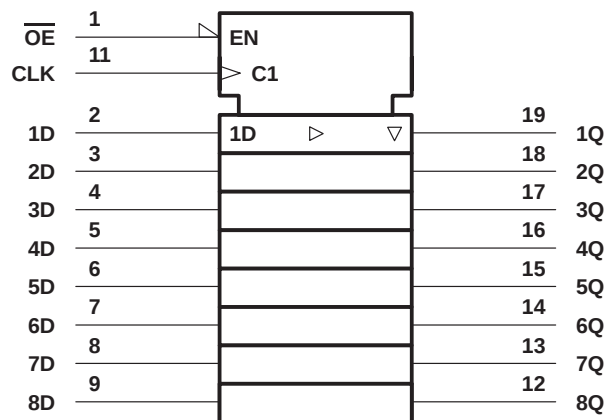
INPUTS			OUTPUT Q
$\overline{\text{OE}}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

SN74ALS575A, SN54AS575, SN74AS575
(each flip-flop)

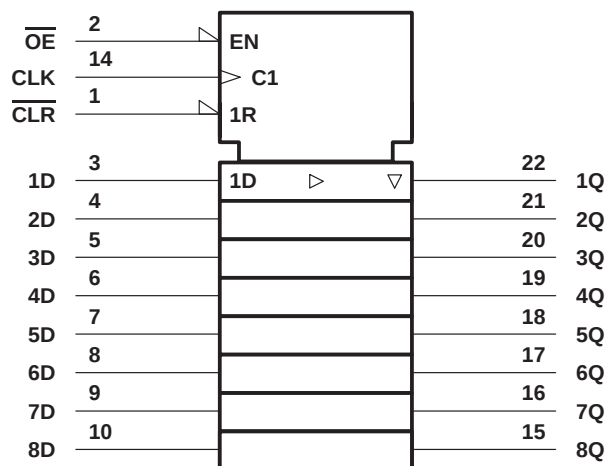
INPUTS				OUTPUT Q
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	CLK	D	
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q ₀
H	X	H	X	Z

logic symbols†

SN54ALS574B, SN74ALS574B,
SN54AS574, SN74AS574



SN74ALS575A, SN54AS575,
SN74AS575

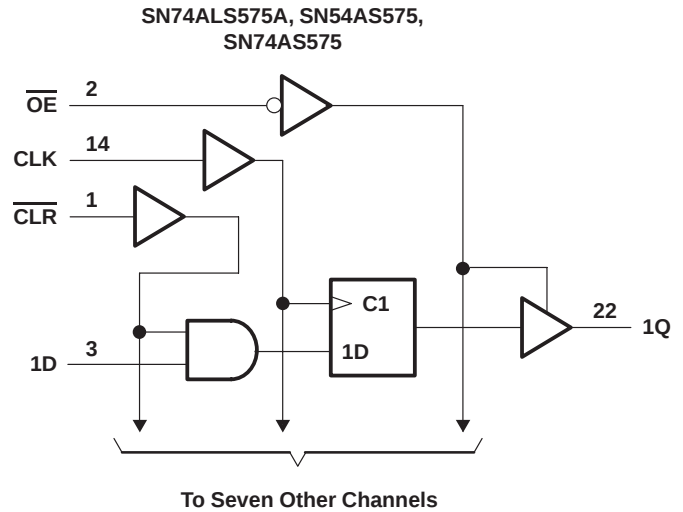
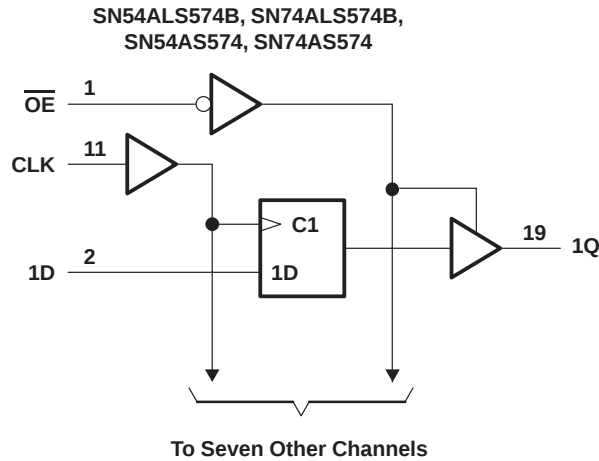


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, J, JT, N, and NT packages.

**SN54ALS574B, SN54AS574, SN54AS575
SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

SDAS165B – JUNE 1982 – REVISED JULY 1995

logic diagrams (positive logic)



Pin numbers shown are for the DW, J, JT, N, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS574B	–55°C to 125°C
SN74ALS574B, SN74ALS575A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
f_{clock}	Clock frequency	'ALS574B						MHz
		0		28	0		35	
t_w	Pulse duration	SN74ALS575A						ns
		16.5			14			
t_{su}	Setup time before CLK $\uparrow$	SN74ALS575A, CLK high or low						ns
		15			16.5			
t_h	Hold time after CLK $\uparrow$	Data						ns
		4			15			
T_A	Operating free-air temperature	SN74ALS575A, CLR						°C
		–55		125	0		70	



SN54ALS574B, SN54AS574, SN54AS575
SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS574B			SN74ALS574B SN74ALS575A			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -1\text{ mA}$	2.4	3.3					
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -2.6\text{ mA}$				2.4	3.2		
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$		0.25	0.4		0.25	0.4	V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 24\text{ mA}$					0.35	0.5	
I_{OZH}		$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$			20			20	μA
I_{OZL}		$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$			-20			-20	μA
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA
I_{IH}		$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA
I_{IL}		$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.2			-0.2	mA
$I_O^{\ddagger}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-20		-112	-30		-112	mA
I_{CC}	'ALS574B	$V_{CC} = 5.5\text{ V}$	Outputs high		11	18	11	18	mA
			Outputs low		17	27	17	27	
			Outputs disabled		17	28	17	28	
	SN74ALS575A	$V_{CC} = 5.5\text{ V}$	Outputs high		10	17	10	17	
			Outputs low		15	24	15	24	
			Outputs disabled		16	30	16	30	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX§						UNIT
			SN54ALS574B		SN74ALS574B		SN74ALS575A		
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			28		35		30		MHz
t _{PLH}	CLK	Q	4	22	3	14	4	14	ns
t _{PHL}			4	17	4	14	4	14	
t _{PZH}	OE	Q	4	21	3	18	4	18	ns
t _{PZL}			4	26	4	18	4	18	
t _{PHZ}	OE	Q	2	16	1	10	2	10	ns
t _{PLZ}			2	25	2	12	3	13	

^{\S} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS574B, SN54AS574, SN54AS575
SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54AS574, SN54AS575	–55°C to 125°C
SN74AS574, SN74AS575	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−12			−15			mA
I _{OL}	Low-level output current		32			48			mA
f _{clock} *	Clock frequency		0	100		0	90		MHz
t _w *	Pulse duration	CLK high	5			5.5			ns
		CLK low	4			5.5			
t _{su} *	Setup time before CLK↑	Data	3			5.5			ns
		‘AS575, $\overline{\text{CLR}}$ high or low	6.5			6.5			
t _h *	Hold time after CLK↑	Data	3			3			ns
		‘AS575, $\overline{\text{CLR}}$	0			0			
T _A	Operating free-air temperature		−55	125		0	70		°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS574B, SN54AS574, SN54AS575
SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS574 SN54AS575			SN74AS574 SN74AS575			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = –2 mA		V _{CC} – 2			V _{CC} – 2			V
		V _{CC} = 4.5 V	I _{OH} = –12 mA	2.4	3.2					
			I _{OH} = –15 mA				2.4	3.3		
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 32 mA	0.29 0.5					V	
			I _{OL} = 48 mA			0.34 0.5				
I _{OZH}		V _{CC} = 5.5 V, V _O = 2.7 V		50			50			μA
I _{OZL}		V _{CC} = 5.5 V, V _O = 0.4 V		–50			–50			μA
I _I		V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}		V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	$\overline{\text{OE}}$, CLK, $\overline{\text{CLR}}$	V _{CC} = 5.5 V, V _I = 0.4 V		–0.5			–0.5			mA
	D			–3			–2			
I _O †		V _{CC} = 5.5 V, V _O = 2.25 V		–30	–112	–30	–112	mA		
I _{CC}	‘AS574	V _{CC} = 5.5 V	Outputs high	73	116	73	116	mA		
			Outputs low	85	134	85	134			
			Outputs disabled	84	134	84	134			
	‘AS575	V _{CC} = 5.5 V	Outputs high	78	126	78	126			
			Outputs low	89	142	89	142			
			Outputs disabled	88	142	88	142			

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS574 SN54AS575		SN74AS574 SN74AS575		
			MIN	MAX	MIN	MAX	
f _{max} *			100		90		MHz
t _{PLH}	CLK	Any Q	3	11	3	8	ns
t _{PHL}			4	11	4	9	
t _{PZH}	$\overline{\text{OE}}$	Any Q	2	7	2	6	ns
t _{PZL}			3	11	3	10	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	2	7	2	6	ns
t _{PLZ}			2	7	2	6	

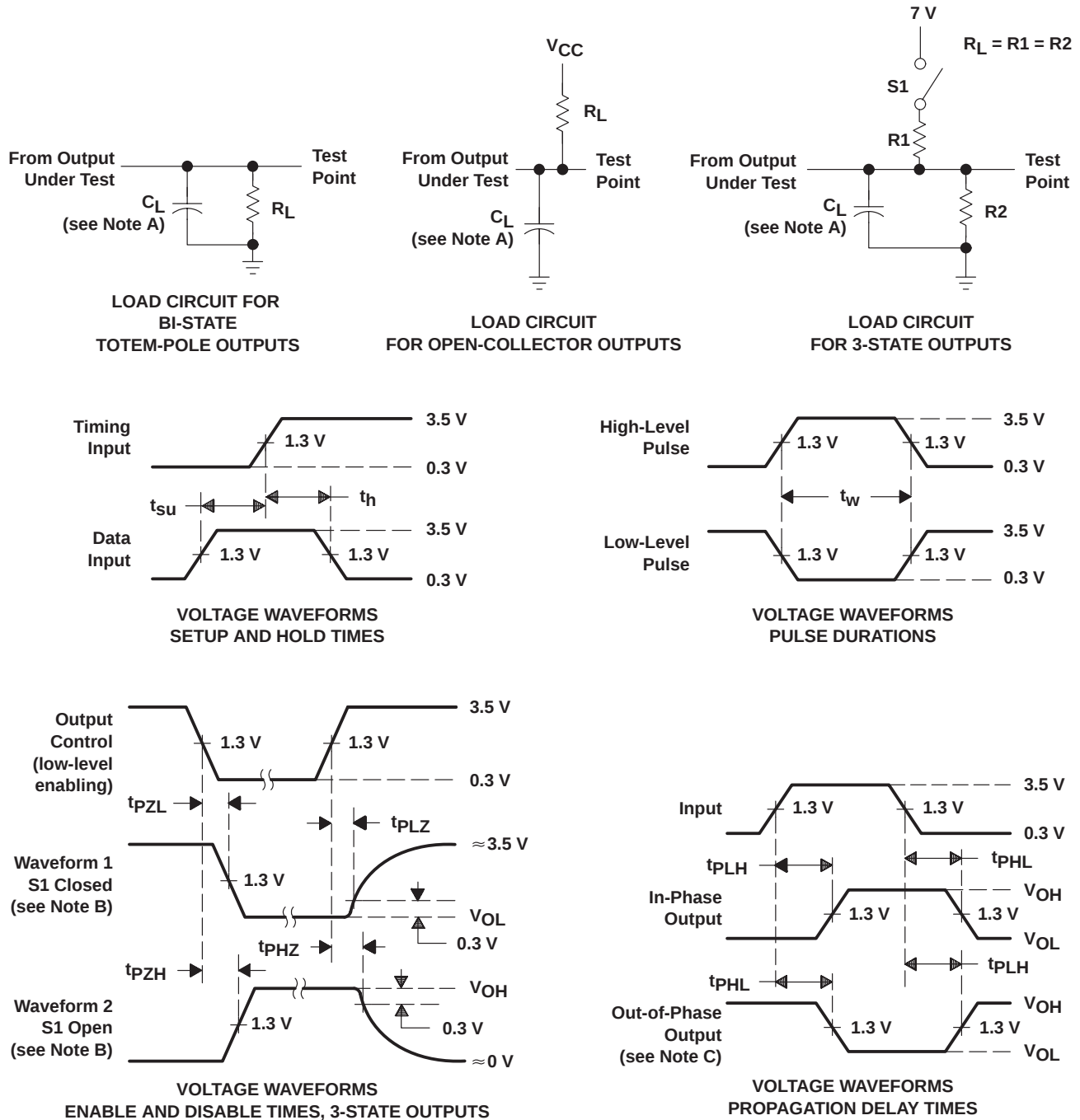
^{*} On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

[§] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS574B, SN54AS574, SN54AS575
SN74ALS574B, SN74ALS575A, SN74AS574, SN74AS575
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS165B – JUNE 1982 – REVISED JULY 1995

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84001012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84001012A SNJ54ALS 574BFBK
8400101RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400101RA SNJ54ALS574BJ
8400101SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400101SA SNJ54ALS574BW
JM38510/37104B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37104B2A
JM38510/37104BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37104BRA
SN54ALS574BJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS574BJ
SN54AS574J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS574J
SN74ALS574BDW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	ALS574B
SN74ALS574BDWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS574B
SN74ALS574BN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS574BN
SN74ALS574BNSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS574B
SN74ALS575ADW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS575A
SN74AS574DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	AS574
SN74AS574DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS574
SN74AS574N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS574N
SNJ54ALS574BFBK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84001012A SNJ54ALS 574BFBK
SNJ54ALS574BJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400101RA SNJ54ALS574BJ
SNJ54ALS574BW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400101SA SNJ54ALS574BW
SNJ54AS574J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54AS574J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS574B, SN54AS574, SN74ALS574B, SN74AS574 :

- Catalog : [SN74ALS574B](#), [SN74AS574](#)
- Military : [SN54ALS574B](#), [SN54AS574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS574BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS574BNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AS574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS574BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS574BNSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AS574DWR	SOIC	DW	20	2000	367.0	367.0	45.0

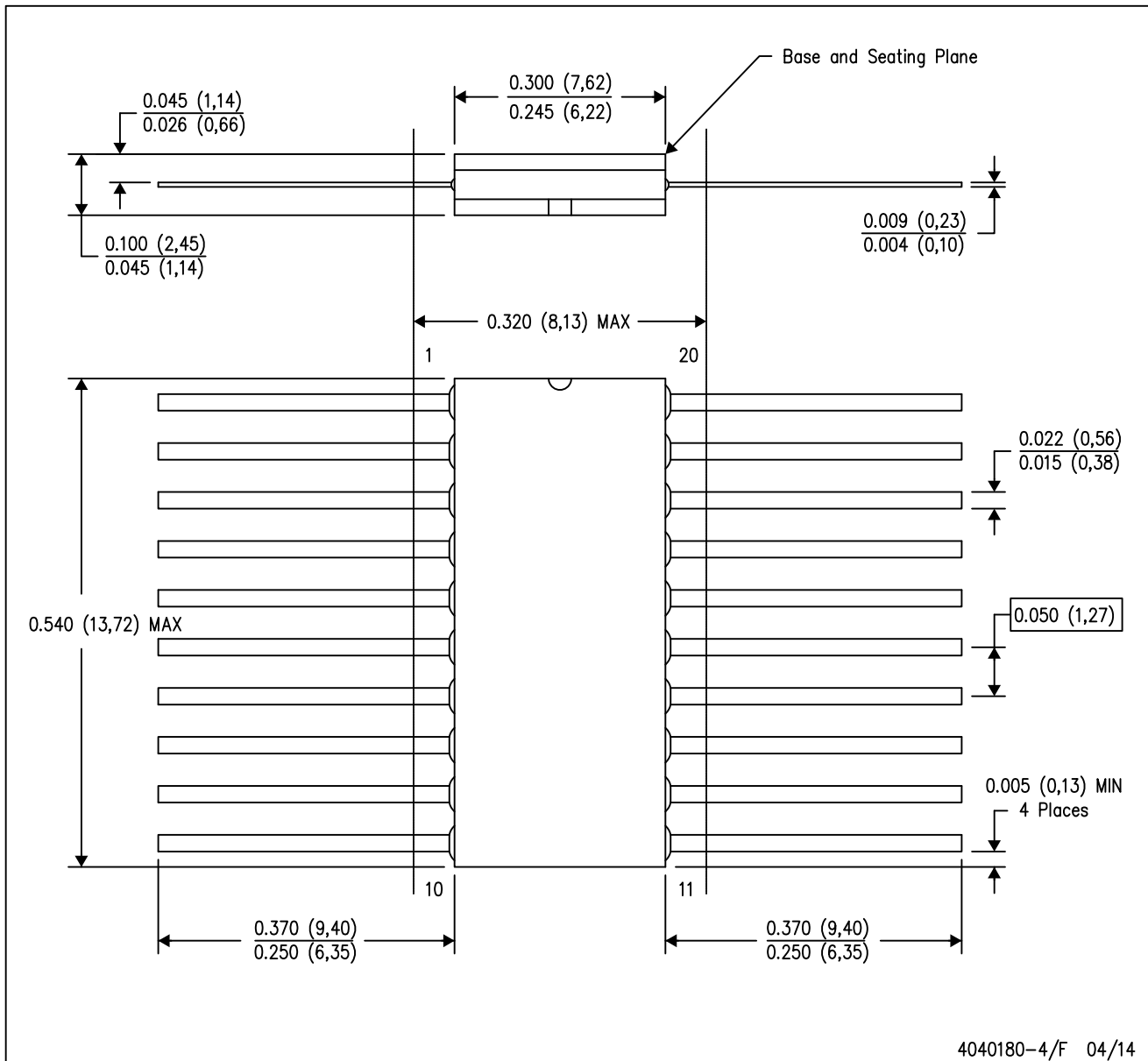
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84001012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8400101SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/37104B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37104B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS574BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS574BNE4	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS575ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74AS574N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS574BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS574BW	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

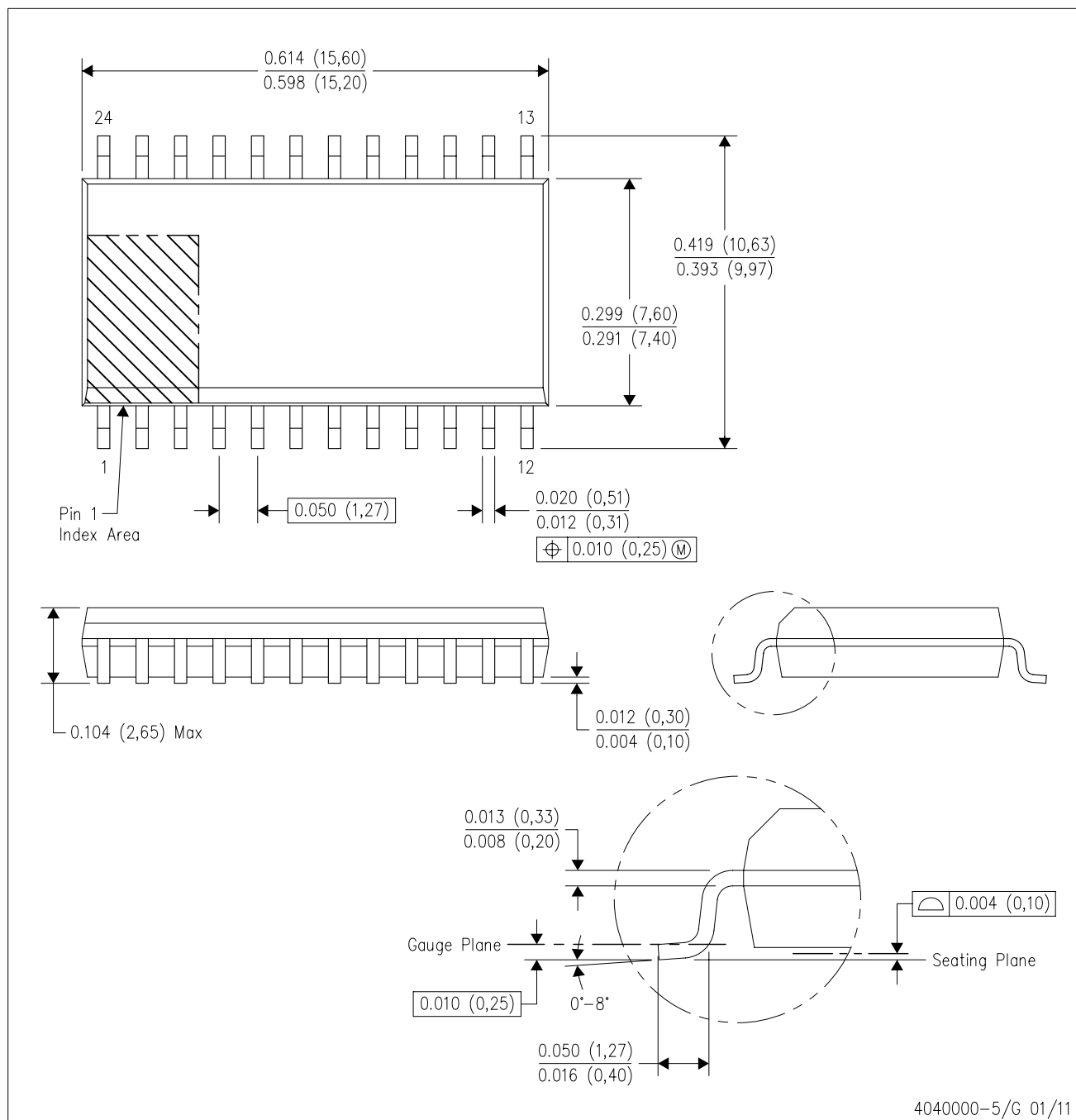


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

GENERIC PACKAGE VIEW

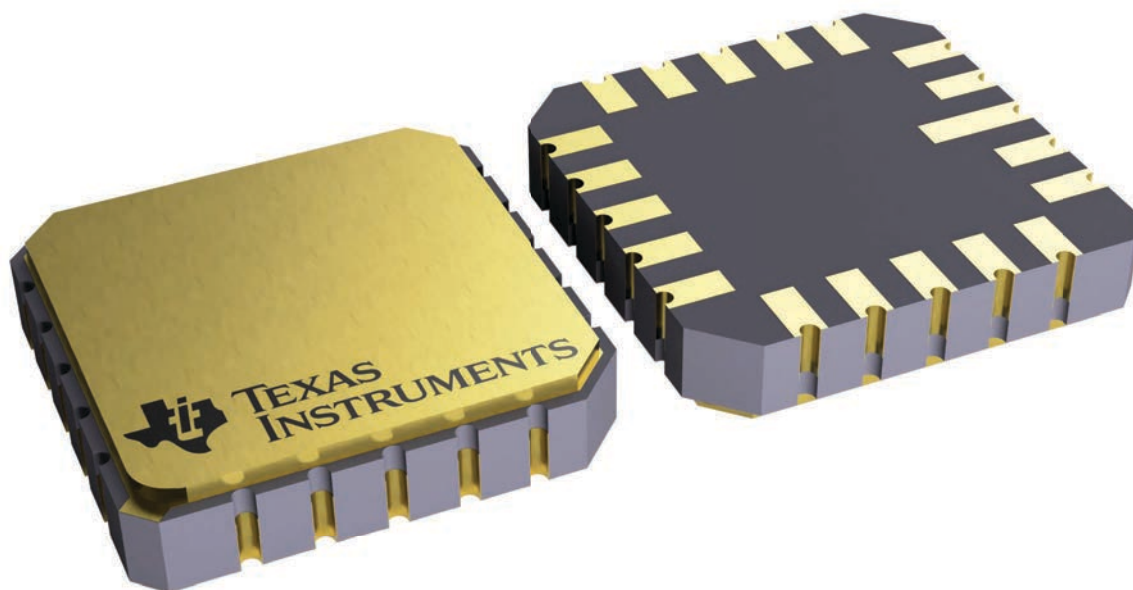
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



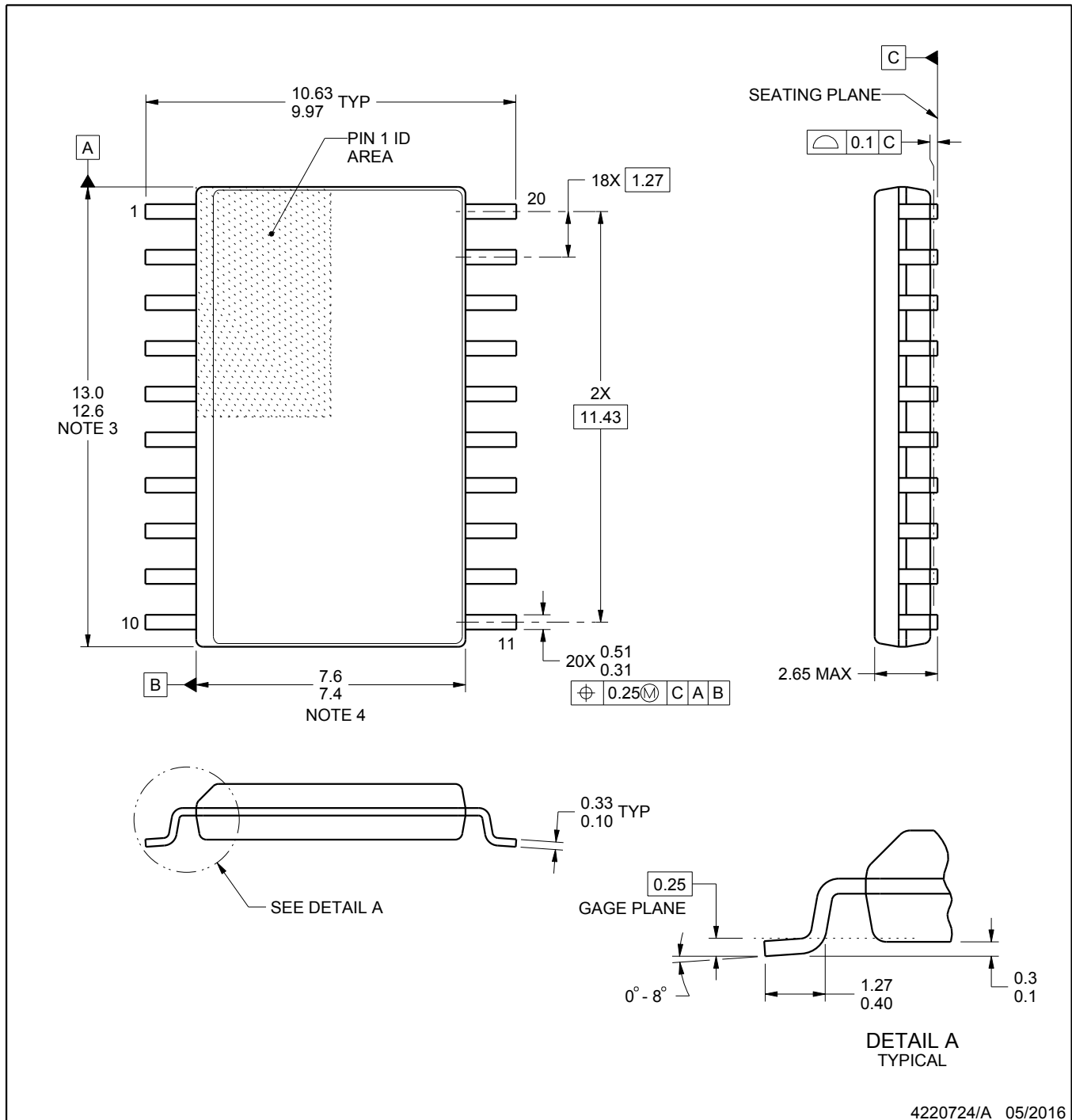
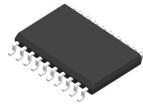
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

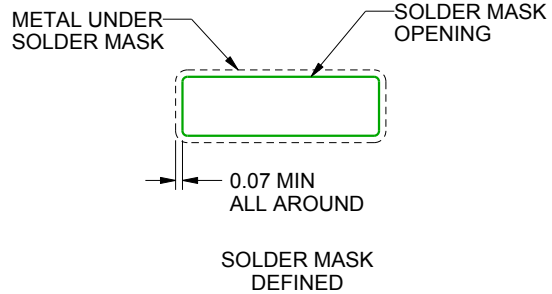
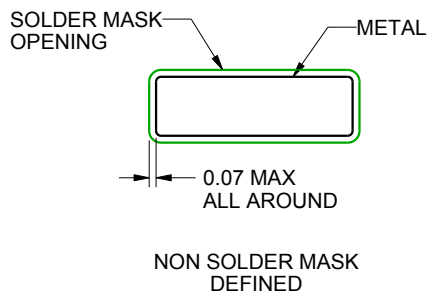
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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