SN74LS07 Hex Buffers and Drivers With Open-Collector High-Voltage Outputs

1 Features

- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays

2 Applications

- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid-State Drives (SSD): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description

These hex buffers and drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs. The SN74LS07 devices have a rated output voltage of 30 V. The maximum sink current is 40 mA.

These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW, and average propagation delay time is 12 ns.

Device Information[(1)]

PART NUMBER	PACKAGE (PINS)	BODY SIZE (NOM)
SN74LS07D	SOIC (14)	8.65 mm × 3.90 mm
SN74LS07DB	SSOP (14)	6.20 mm × 5.30 mm
SN74LS07N	PDIP (14)	19.30 mm × 6.35 mm
SN74LS07NS	SO (14)	10.30 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

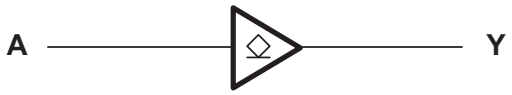


Table of Contents

4 Revision History

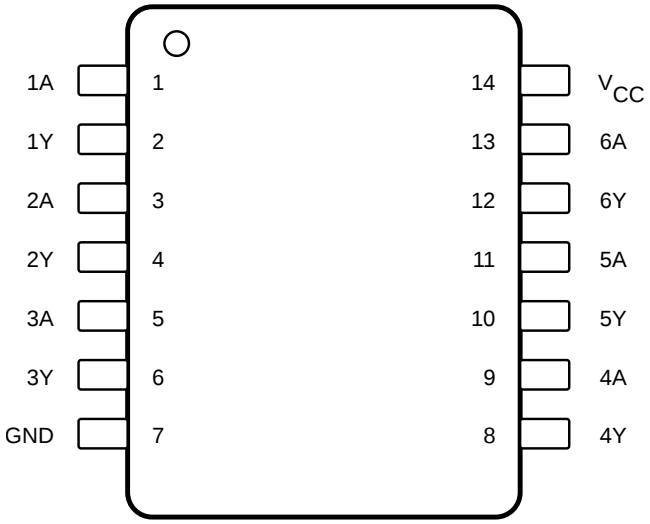
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2004) to Revision D **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted SN54LS07 and SN74LS17 from the data sheet because they are obsolete and no longer supplied ... 1
- Deleted *Ordering Information* table. ... 1

5 Pin Configuration and Functions

D, DB, N, or NS Packages
14-Pin SOIC, SSOP, PDIP, SO
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Input 1
2	1Y	O	Output 1
3	2A	I	Input 2
4	2Y	O	Output 2
5	3A	I	Input 3
6	3Y	O	Output 3
7	GND	—	Ground pin
8	4Y	O	Output 4
9	4A	I	Input 4
10	5Y	O	Output 5
11	5A	I	Input 5
12	6Y	O	Output 6
13	6A	I	Input 6
14	V_{CC}	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
V_I	Input voltage(2)		7	V
V_O	Output voltage(2)(3)		30	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) This is the maximum voltage that should be applied to any output when it is in the off state.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			30	V
I_{OL}	Low-level output current			40	mA
T_A	Operating free-air temperature	0		70	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LS07				UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.2	97.4	50.2	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	49.8	37.5	40.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	44.5	30	41.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	16.5	22.3	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39.4	44	29.9	41.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5	V
I_{OH}	V_{CC} = MIN, V_{IH} = 2 V	V_{OH} = 30 V			0.25	mA
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V	I_{OL} = 16 mA			0.4	V
		I_{OL} = MAX[2]			0.7	
I_I	V_{CC} = MAX, V_I = 7 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				–0.2	mA
I_{CCH}	V_{CC} = MAX				14	mA
I_{CCL}	V_{CC} = MAX				45	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) I_{OL} = 40 mA

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 110 Ω, C_L = 15 pF		6	10	ns
t_{PHL}					19	30	

6.7 Typical Characteristics

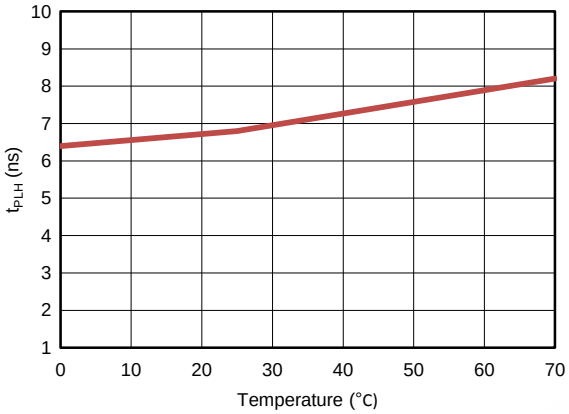
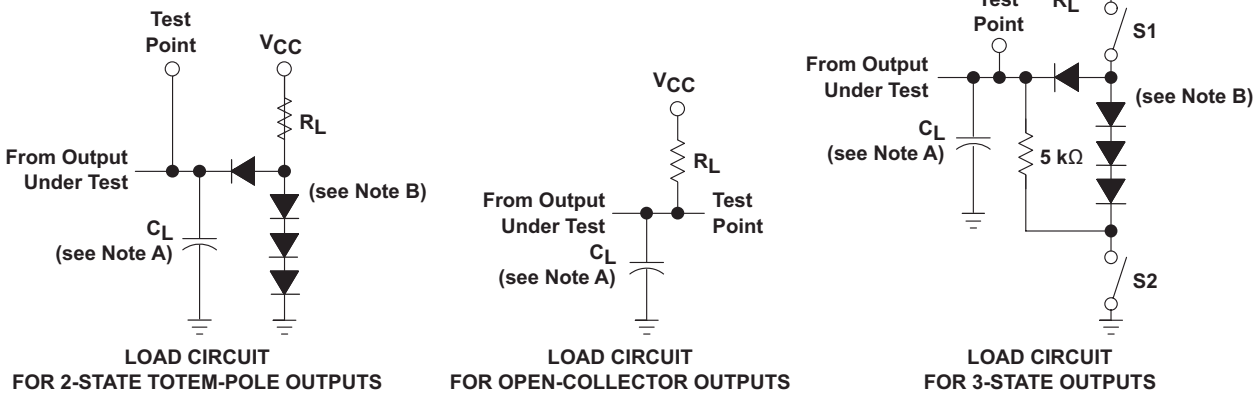
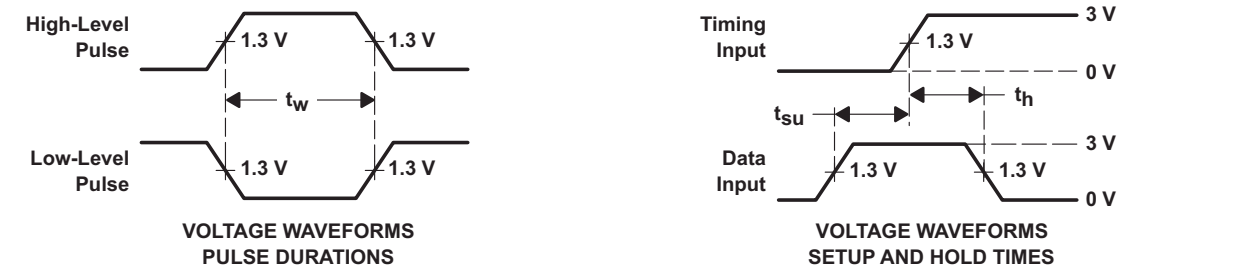
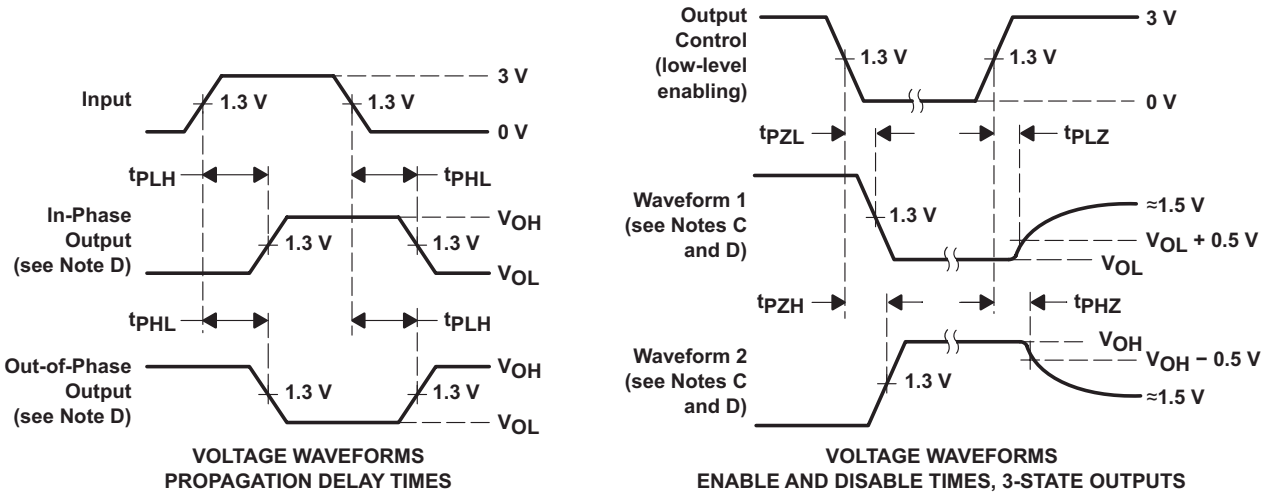


Figure 1. t_{PLH} vs. Temperature

7 Parameter Measurement Information







A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω, t_r ≤ 1.5 ns, t_f ≤ 2.6 ns.

G. The outputs are measured one at a time, with one input transition per measurement.

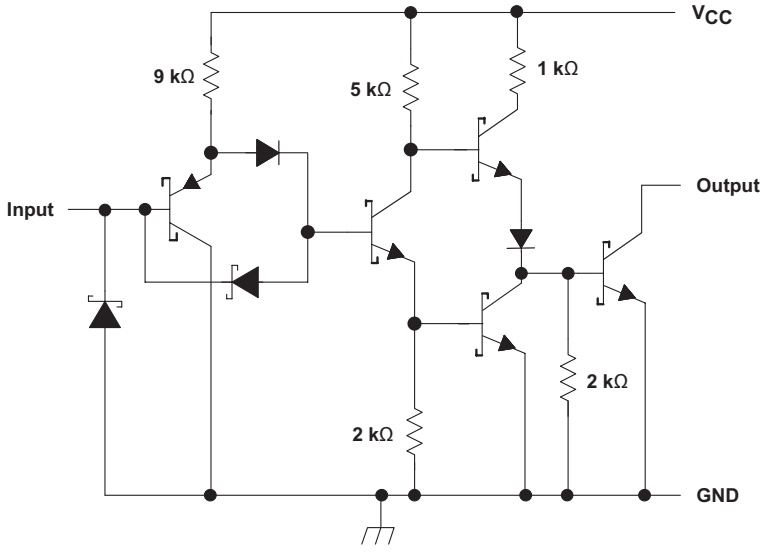
Figure 2. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The outputs of the SN74LS07 device are open-collector and can be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current for the SN74LS07 is 40 mA.

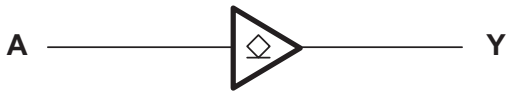
Inputs can be driven from 2.5-V, 3.3-V (LVTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.



Resistor values shown are nominal.

Figure 3. Schematic (Gate)

8.2 Functional Block Diagram



8.3 Feature Description

- Allows for up translation
  - Inputs accept voltages to 5.25 V
  - Outputs accept voltages to 30 V
- High Sink-Current Capability
  - Up to 40 mA

8.4 Device Functional Modes

Table 1 lists the functions of this device.

Table 1. Function Table

INPUT A	OUTPUT Y
H	Hi-Z
L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LS07 device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 40 mA of drive current at 5 V. Therefore, this device is ideal for driving multiple inputs. The inputs are 5.25-V tolerant and outputs are 30-V tolerant.

9.2 Typical Application

Multiple channels of the SN74LS07 device can be used to create a positive AND logic function, as shown in Figure 4. Additionally, the SN74LS07 device can be used to drive an LED by sinking up to 40 mA, which may be more than the previous stage can sink.

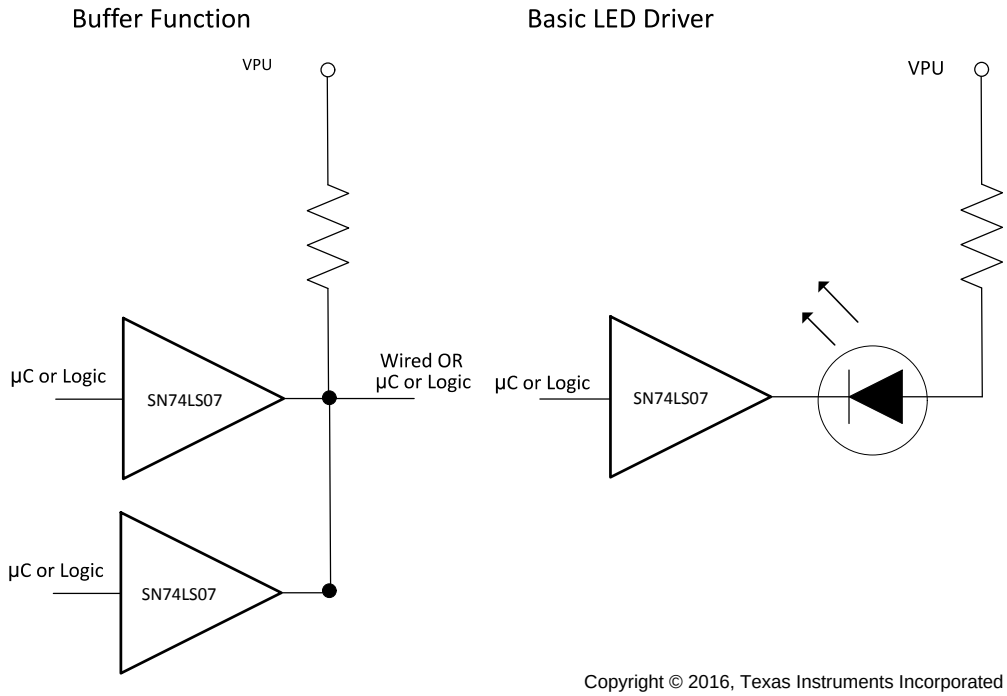


Figure 4. Typical Application Diagram

9.2.1 Design Requirements

Ensure that the inputs are in a known state as defined by V_{IH} and V_{IL} noted in *Recommended Operating Conditions*, or else the outputs may be in an unknown state.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - For specified high and low level, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.25 V.
2. Recommend Output Conditions
   - Load currents must not exceed 40 mA per output.
   - Outputs must not be pulled above 30 V.

Typical Application (continued)

9.2.3 Application Curve

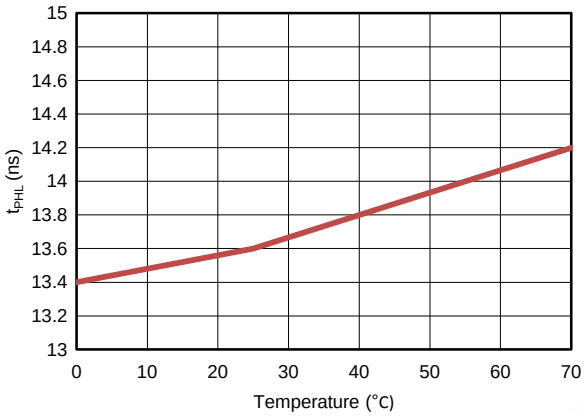


Figure 5. t_{PHL} vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating indicated in *Recommended Operating Conditions*.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} pins, then TI recommends either a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and a 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

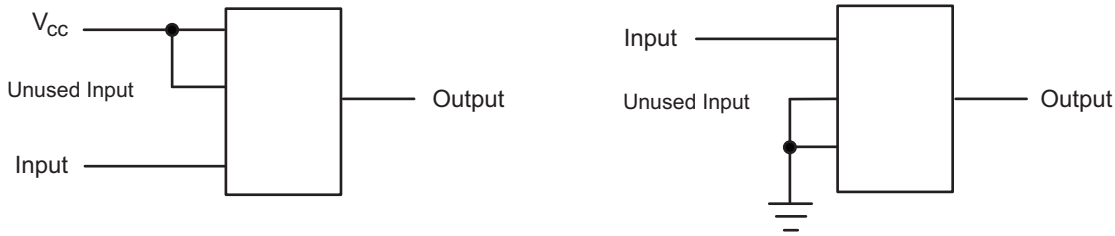


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the followign:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS07D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07
SN74LS07DBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07
SN74LS07DBRG4	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07
SN74LS07DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07
SN74LS07DRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS07
SN74LS07N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS07N
SN74LS07NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS07
SN74LS07NSRG4	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS07

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

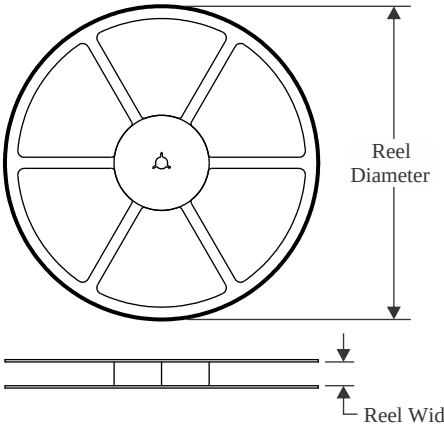
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

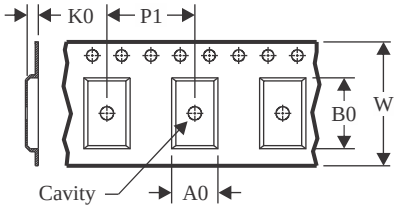
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

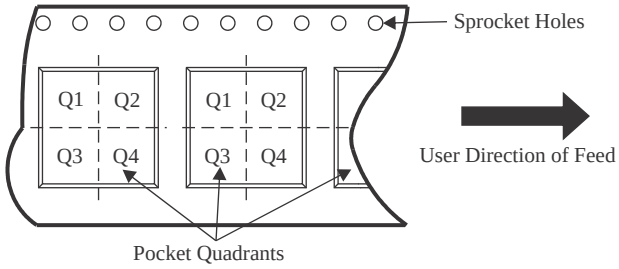


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

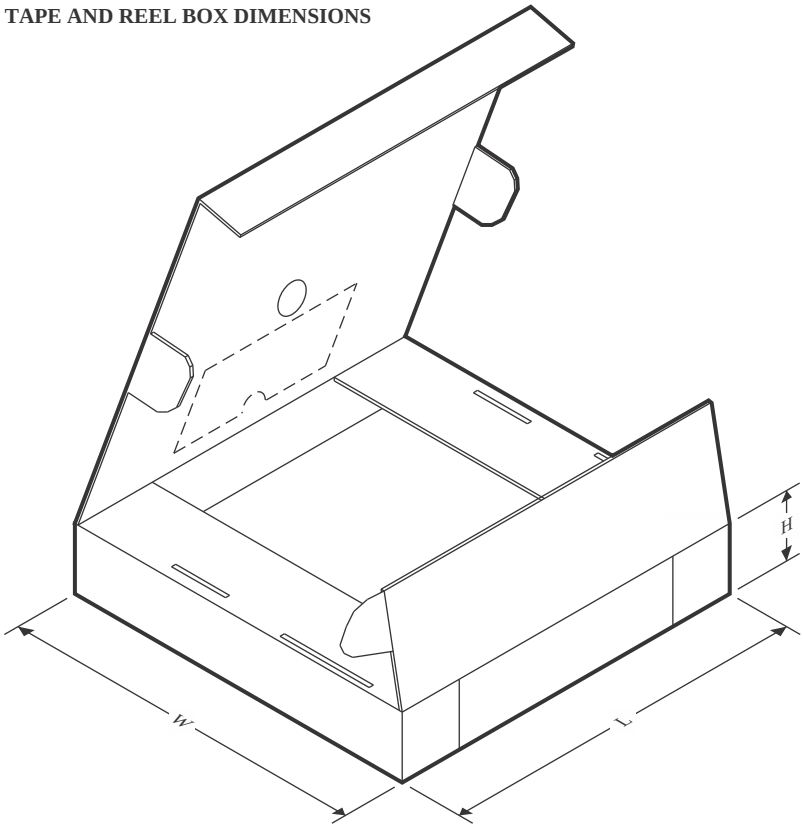
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS07DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS07DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LS07DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS07DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS07NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS07NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

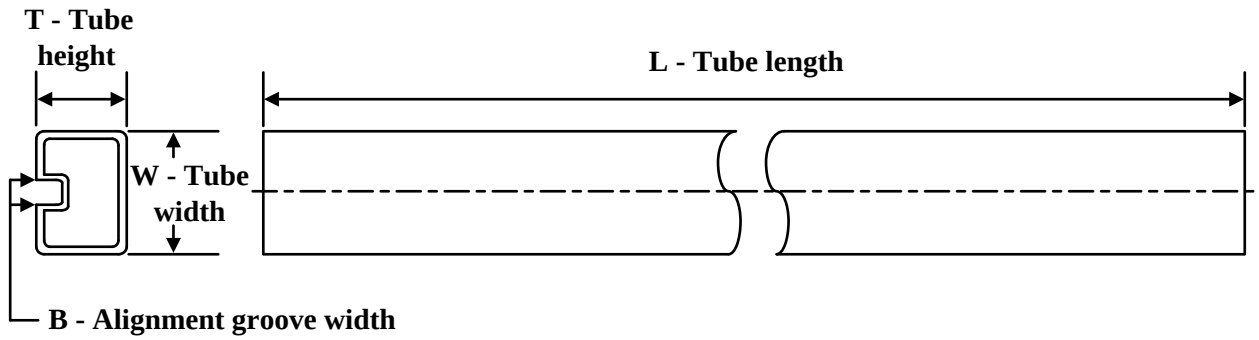
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

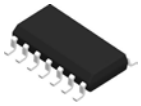
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS07DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LS07DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LS07DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS07DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LS07NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LS07NSR	SOP	NS	14	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS07D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS07N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS07N	N	PDIP	14	25	506	13.97	11230	4.32

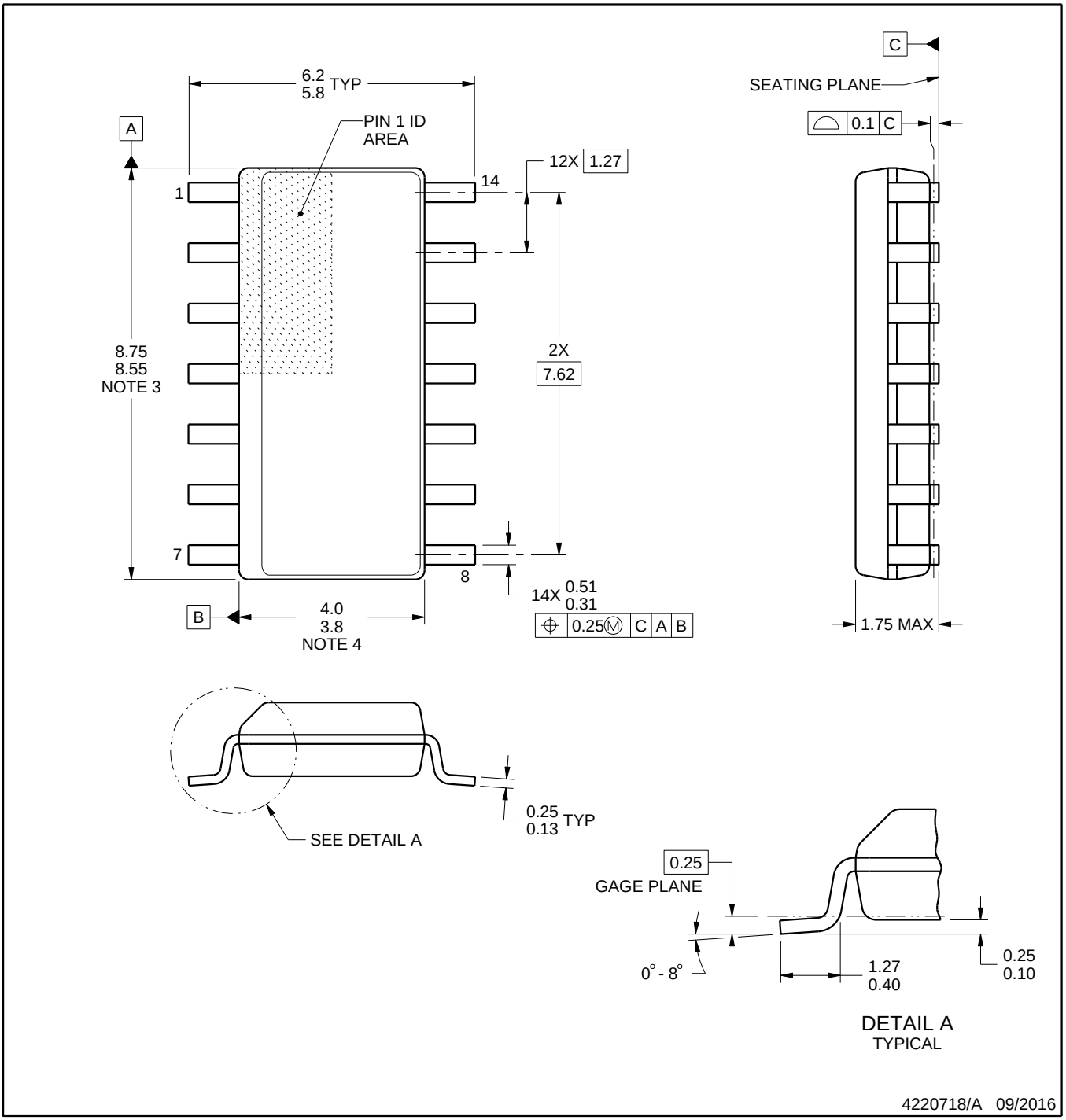


PACKAGE OUTLINE

D0014A

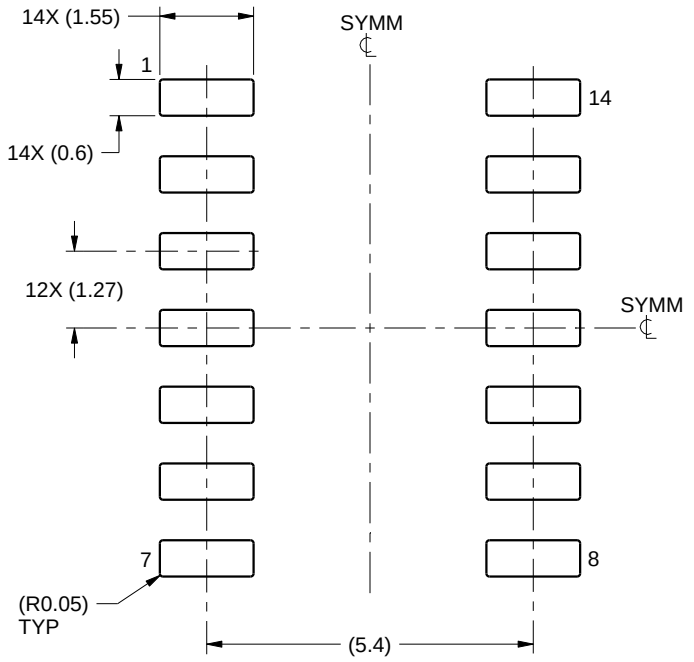
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

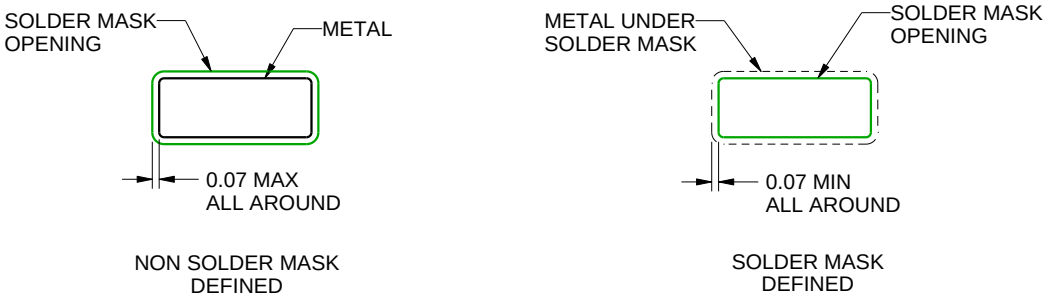


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

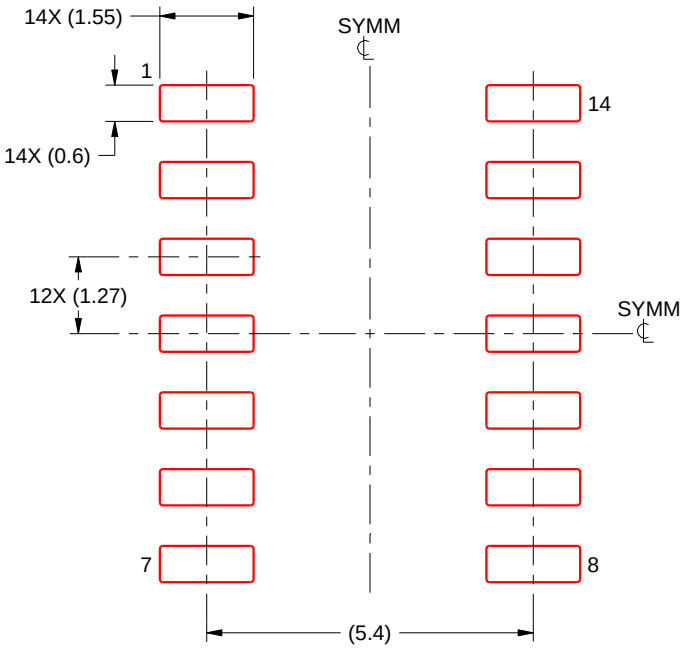
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

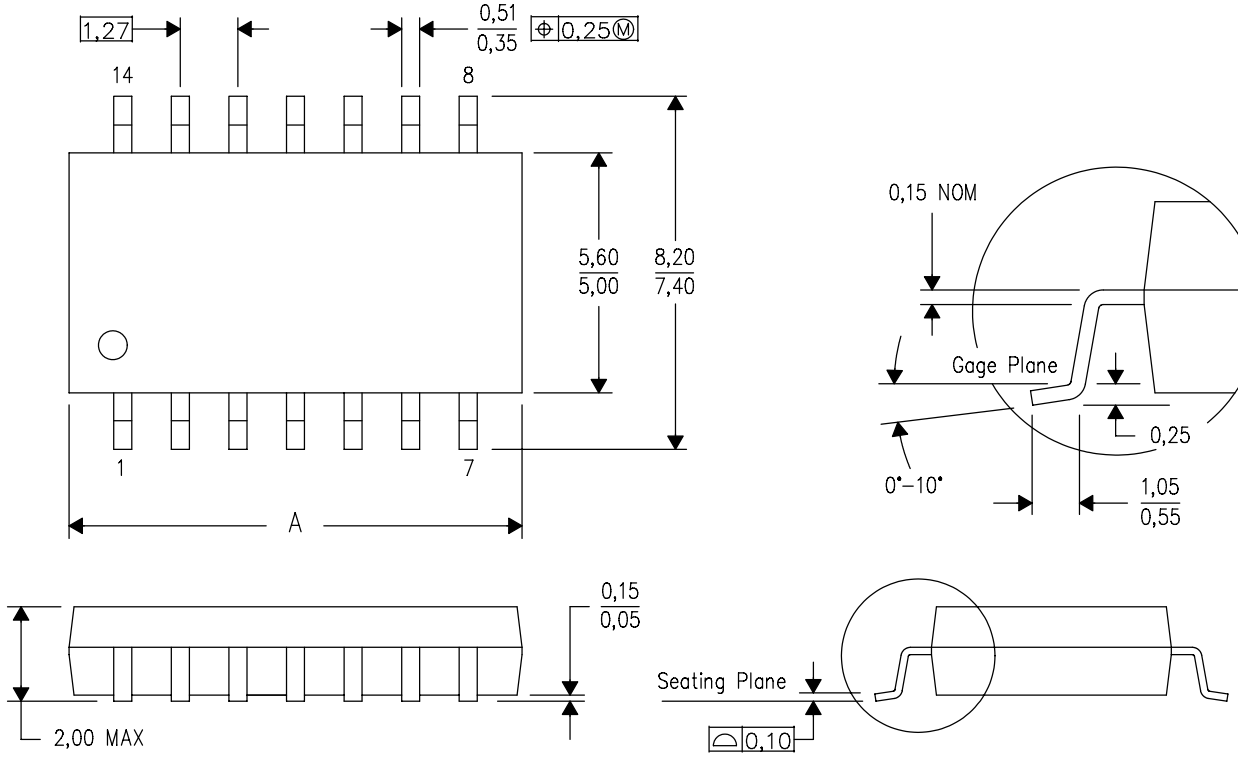
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

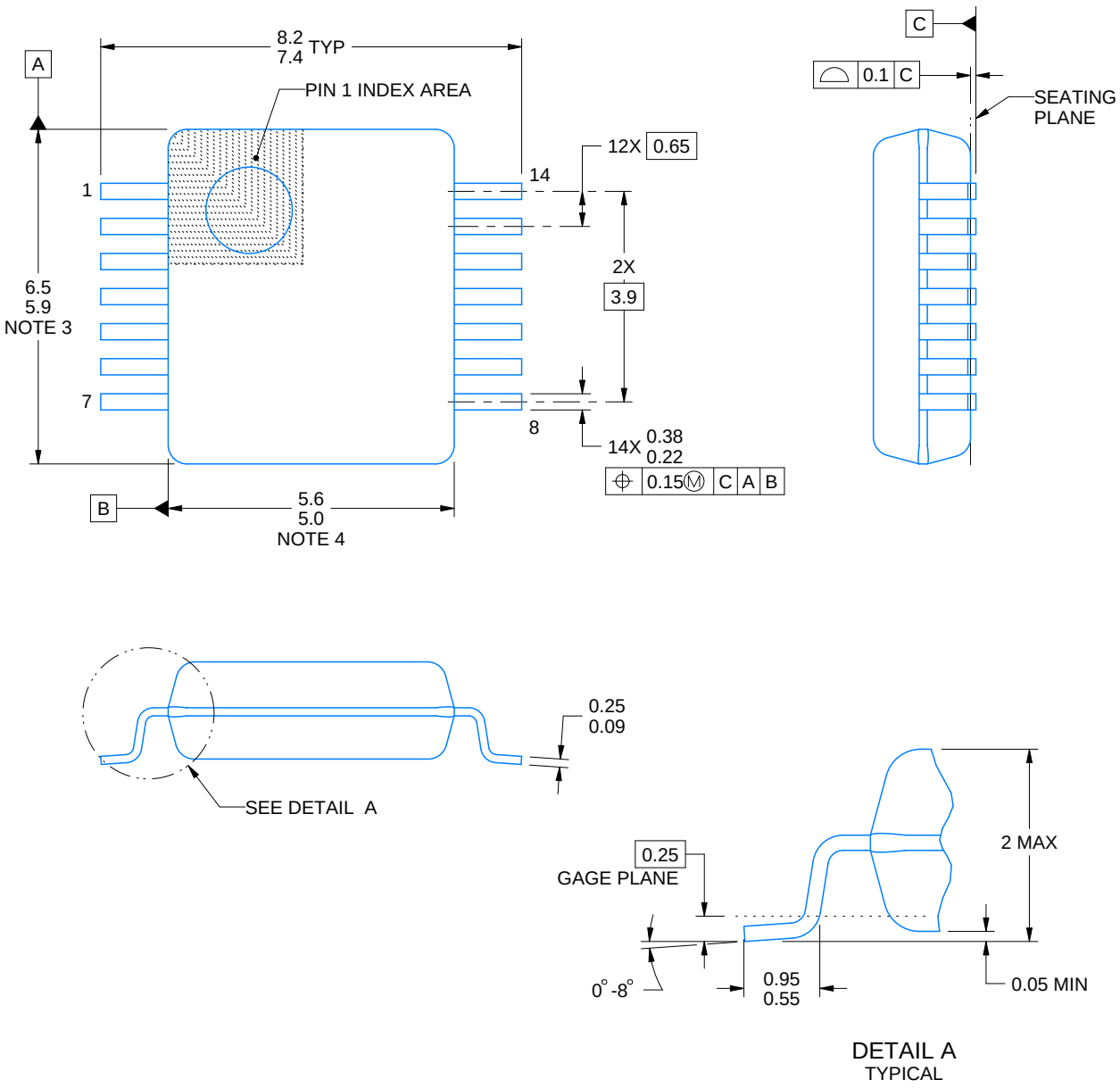
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

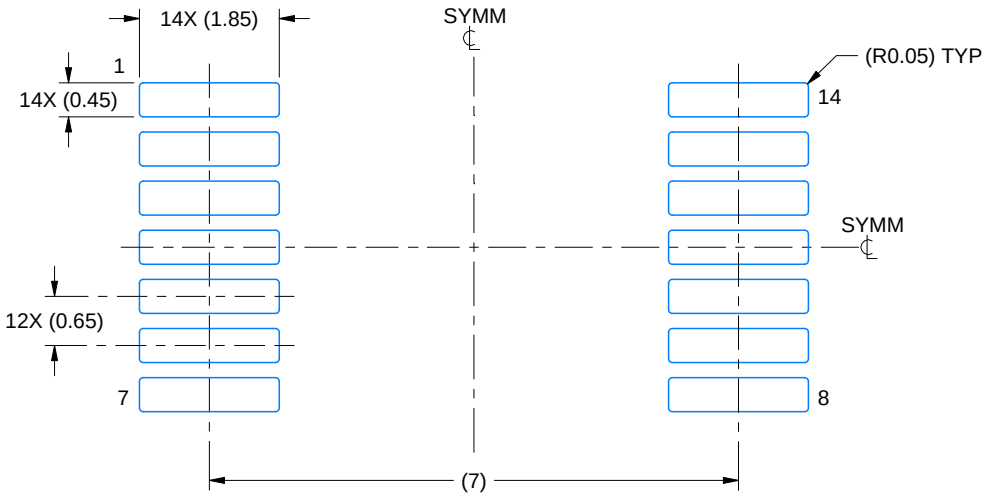
SMALL OUTLINE PACKAGE



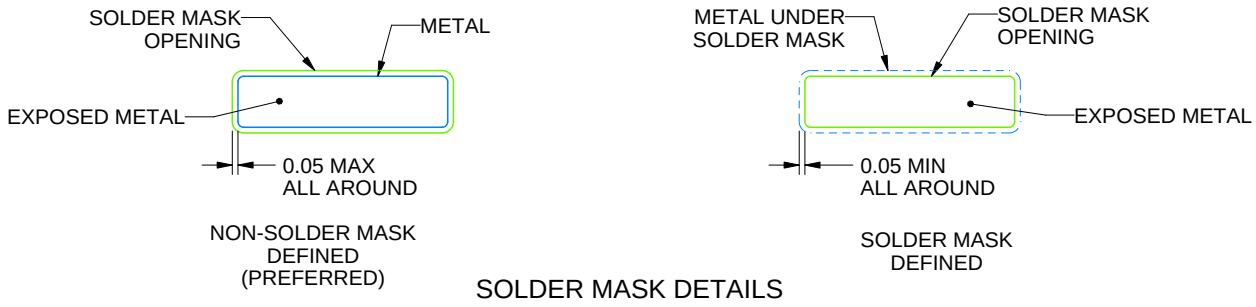
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

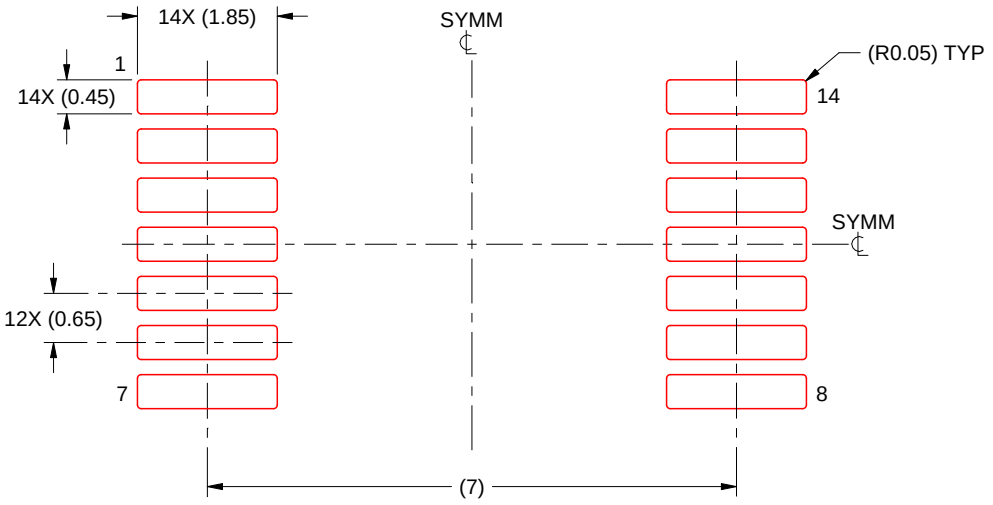


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

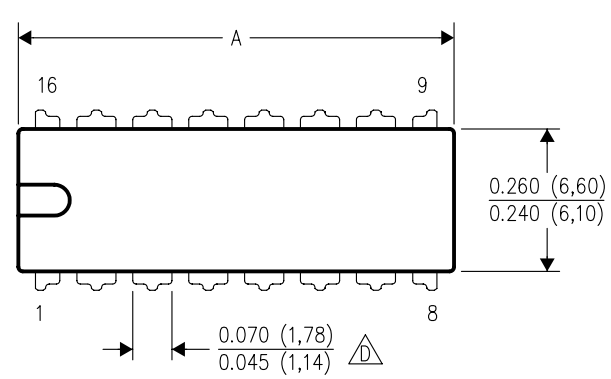
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

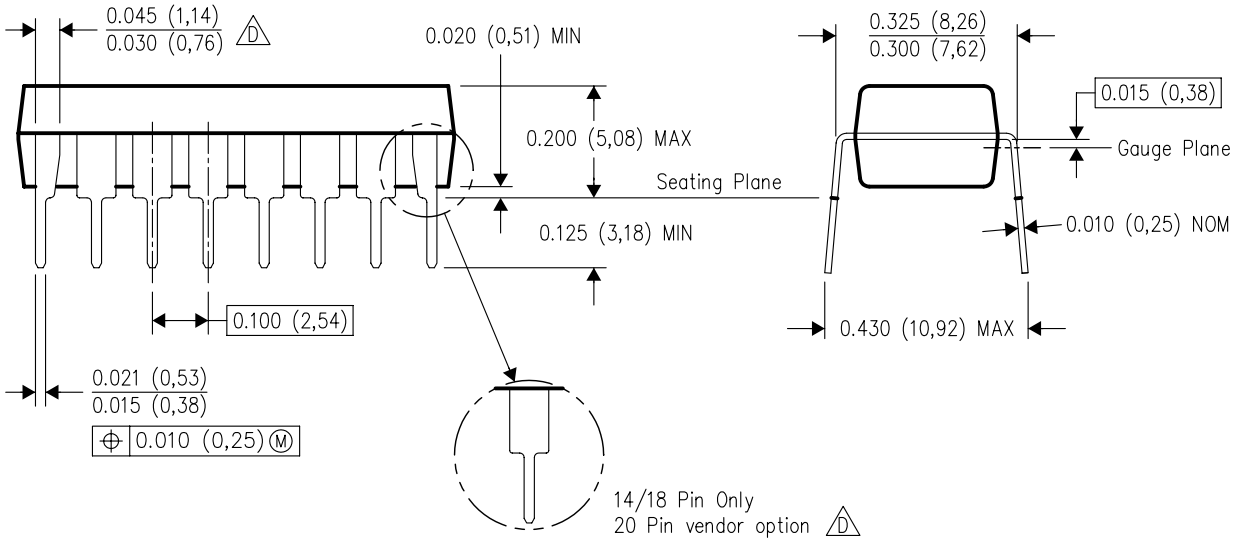
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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