

SN54LS620, SN54LS621, SN74LS620, SN74LS621, SN74LS623 OCTAL BUS TRANSCEIVERS

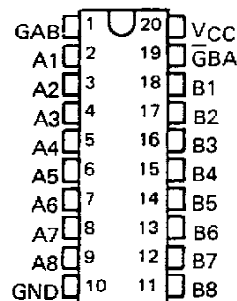
SDLS185

D2537, AUGUST 1979—REVISED MARCH 1988

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS623	3-State	True

SN54LS620, SN54LS621,
SN54LS622 . . . J PACKAGE
SN74LS620, SN74LS621,
SN74LS623 . . . DW OR N PACKAGE
(TOP VIEW)



description

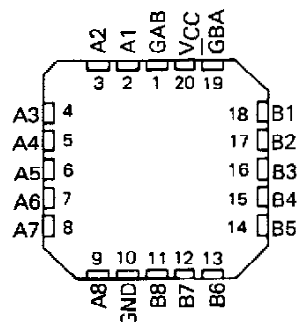
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{\text{GBA}}$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620, 'LS621, and 'LS623 the capability to store data by simultaneous enabling of $\overline{\text{GBA}}$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620.

SN54LS620, SN54LS621,
SN54LS622 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{\text{GBA}}$	GAB	'LS620	'LS621, 'LS623
L	L	B data to A bus	B data to A bus
H	H	A data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	B data to A bus, A data to B bus	B data to A bus, A data to B bus

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	-55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

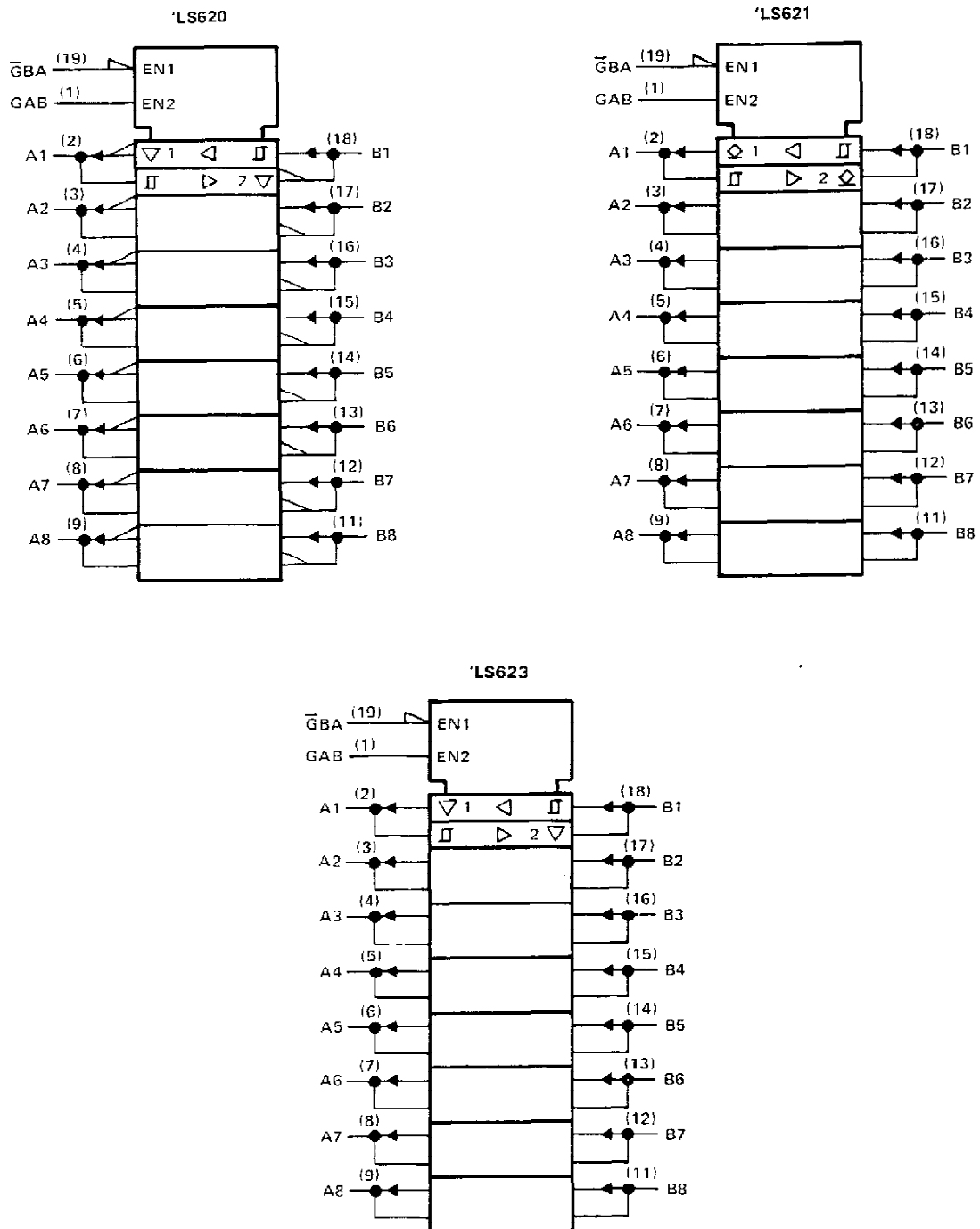
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN54LS620, SN54LS621, SN74LS620, SN74LS621, SN74LS623 OCTAL BUS TRANSCEIVERS

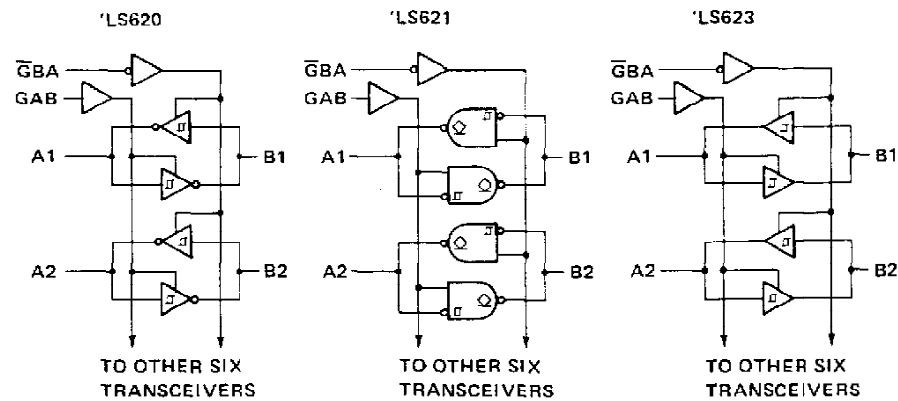
logic symbols†



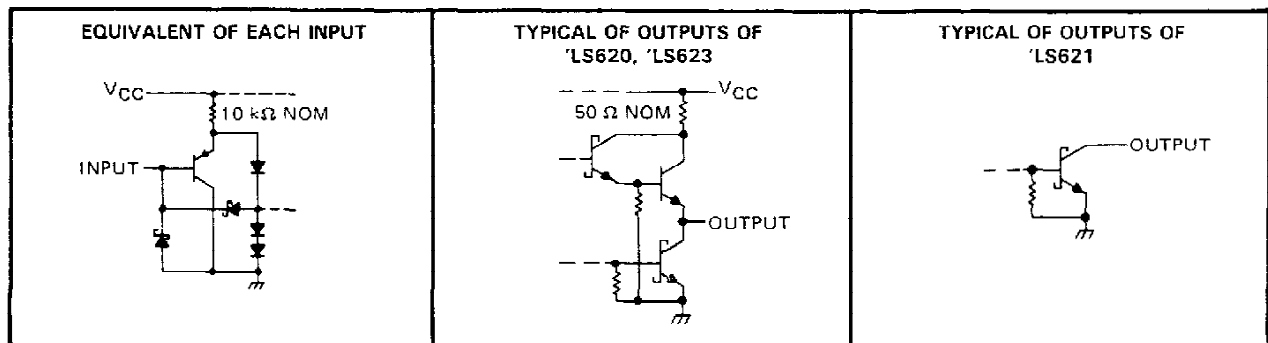
† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, and N packages.

**SN54LS620, SN54LS621,
SN74LS620, SN74LS621, SN74LS623
OCTAL BUS TRANSCEIVERS**

logic diagrams (positive logic)



schematics of inputs and outputs



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SN54LS620, SN74LS620, SN74LS623

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

recommended operating conditions

PARAMETER	SN54LS620			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-12			-15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS620			SN74LS620 SN74LS623			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.5			0.6	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -3 \text{ mA}$	2.4	3.4		2.4	3.4		V
	$I_{OH} = \text{MAX}$	2			2			
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$I_{OL} = 24 \text{ mA}$				0.35	0.5		
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7 \text{ V}, \bar{G} \text{ at } 2 \text{ V}$			20			20	µA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.4 \text{ V}, \bar{G} \text{ at } 2 \text{ V}$			-400			-400	µA
I_I Input current at maximum input voltage	A or B			0.1			0.1	mA
	GBA or GAB			0.1			0.1	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-40		-225	-40		-225	mA
I_{CC} Total supply current	Outputs high			48			48	mA
	Outputs low			62			62	
	Outputs at Hi-Z			64			64	

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			SN74LS623			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	A	B	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$	6	10		8	15		ns
	B	A		6	10		8	15		
t_{PHL} Propagation delay time, high-to-low-level output	A	B		8	15		11	15		ns
	B	A		8	15		11	15		
t_{PZL} Output enable time to low level	$\bar{G}BA$	A	See Note 2	31	40		31	40		ns
	GAB	B		31	40		31	40		
t_{PZH} Output enable time to high level	$\bar{G}BA$	A		23	40		26	40		ns
	GAB	B		23	40		26	40		
t_{PLZ} Output disable time from low level	$\bar{G}BA$	A	$C_L = 5 \text{ pF}, R_L = 667 \Omega,$	15	25		15	25		ns
	GAB	B		15	25		15	25		
t_{PHZ} Output disable time from high level	$\bar{G}BA$	A		15	25		15	25		ns
	GAB	B		15	25		15	25		

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = Output enable time to high level

t_{PZL} = Output enable time to low level

t_{PHZ} = Output disable time from high level

t_{PLZ} = Output disable time from low level

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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SN54LS621, SN74LS621

OCTAL BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

recommended operating conditions

PARAMETER	SN54LS621			SN74LS621			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS621			SN74LS621			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.5			0.6	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input	$V_{CC} = \text{MIN}$	0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$			100			100	µA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 24 \text{ mA}$				0.35	0.5		
I_I	Input current at maximum input voltage	A or B			5.5 V			0.1	mA
		GAB or $\overline{\text{GBA}}$			$V_I = 7 \text{ V}$			0.1	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{CC}	Total supply current	Outputs high	48	70		48	70		mA
		Outputs low	62	90		62	90		

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			UNIT
				MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	$C_L = 45 \text{ pF}, R_L = 667 \Omega,$ See Note 2		17	25	ns
		B			17	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A			16	25	ns
		B			16	25	
t_{PLH}	Output disable time from low level	$\overline{\text{GBA}}$			23	40	ns
		GAB			25	40	
t_{PHL}	Output enable time from high level	$\overline{\text{GBA}}$			34	50	ns
		GAB			37	50	

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



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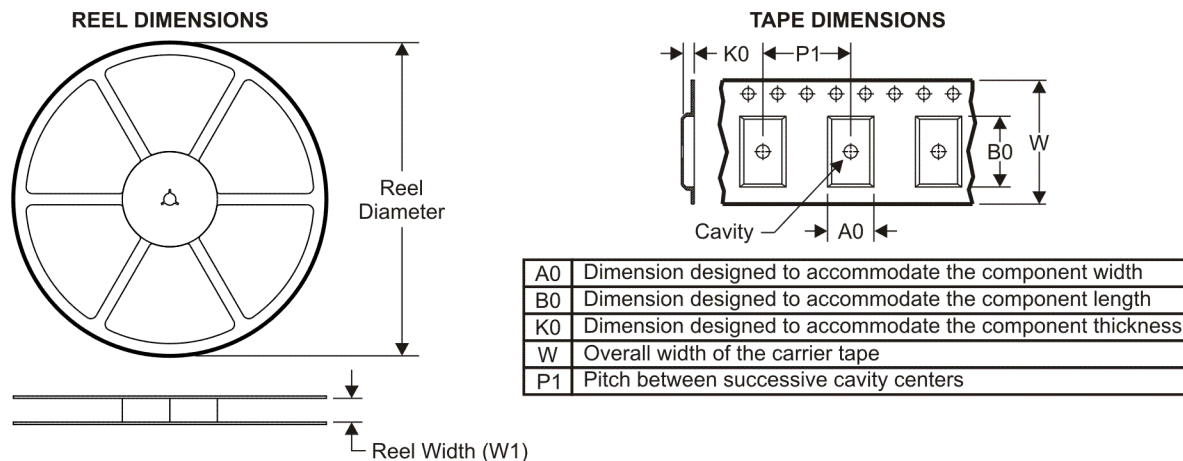
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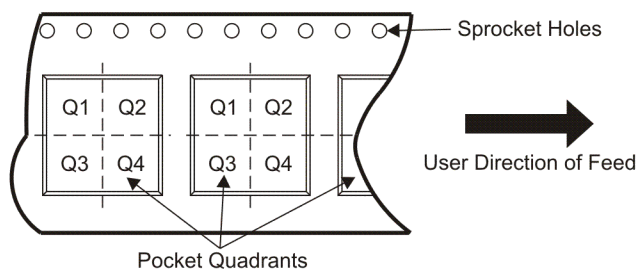
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TAPE AND REEL INFORMATION



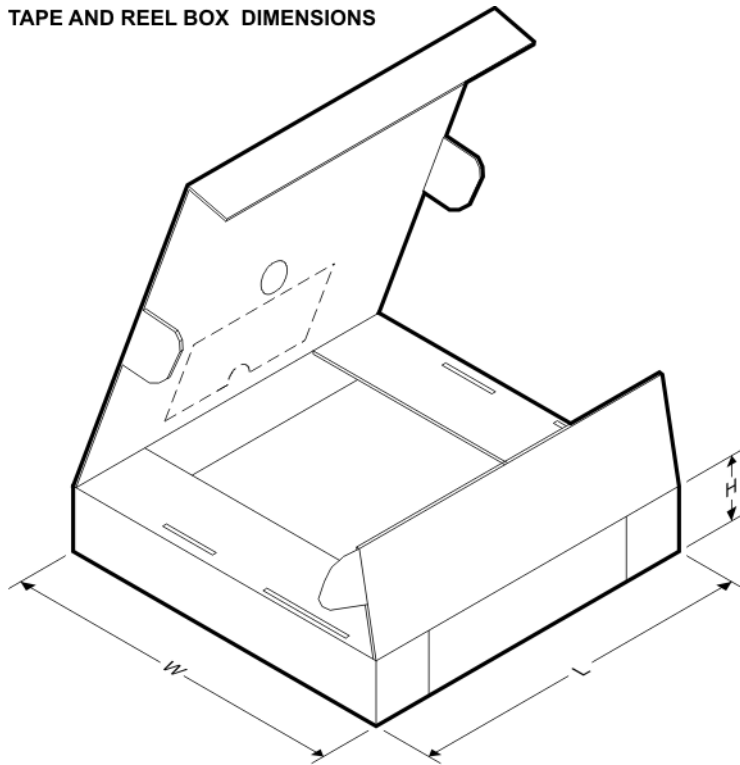
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS623DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LS623NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS623DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN74LS623NSR	SO	NS	20	2000	346.0	346.0	41.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS623N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS623N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



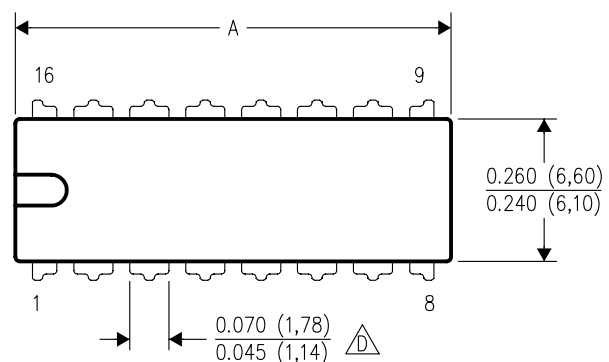
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS623N	N	PDIP	20	20	506	13.97	11230	4.32

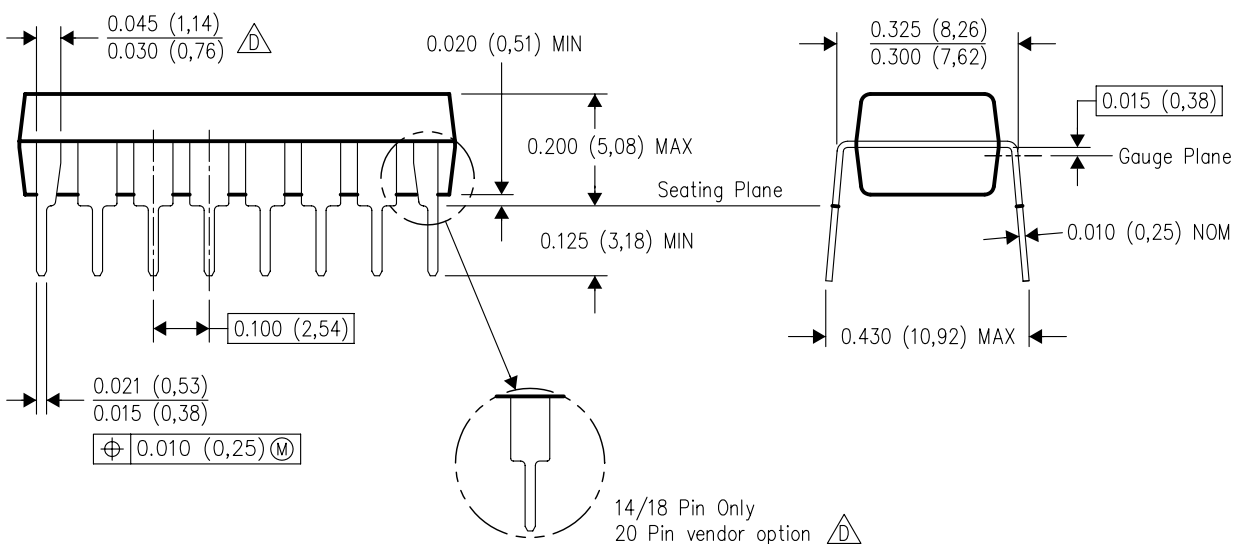
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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