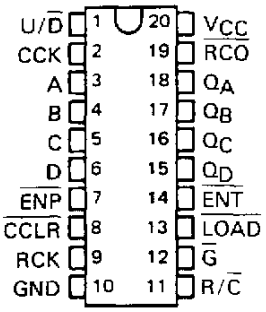
SN54LS696, SN54LS697, SN54LS699, SN74LS696, SN74LS697, SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

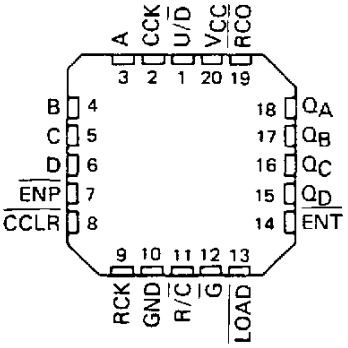
SDLS199 D2424, JANUARY 1981 – REVISED MARCH 1988

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . Decade Counter, Direct Clear
  'LS697 . . Binary Counter, Direct Clear
  'LS699 . . Binary Counter, Synchronous Clear

SN54LS696, SN54LS697, SN54LS699 . . . J OR W PACKAGE
SN74LS696, SN74LS697, SN74LS699 . . . DW OR N PACKAGE
(TOP VIEW)



SN54LS696, SN54LS697, SN54LS699 . . . FK PACKAGE
(TOP VIEW)



description

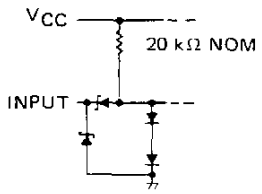
These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable $\overline{P}$ and enable $\overline{T}$ and a ripple-carry output for easy expansion. The register/counter select input R/$\overline{C}$, selects the counter when low and the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

Both the counter CCK and register clock RCK are positive-edge triggered. The counter clear $\overline{CCLR}$ is active low and is asynchronous on the 'LS696 and 'LS697, synchronous on the 'LS699. Loading of the counter is accomplished when $\overline{LOAD}$ is taken low and a positive transition occurs on the counter clock CCK.

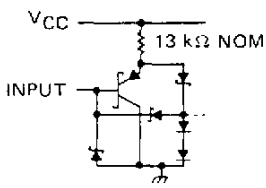
Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to $\overline{ENT}$ of the second stage, etc. All $\overline{ENP}$ inputs can be tied common and used as a master enable or disable control.

schematics of inputs and outputs

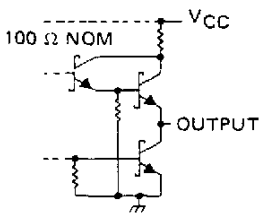
EQUIVALENT OF A, B, C, D INPUTS



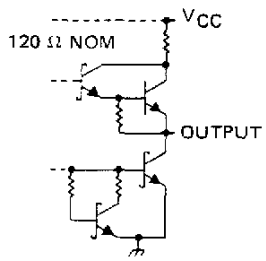
EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF ALL Q OUTPUTS

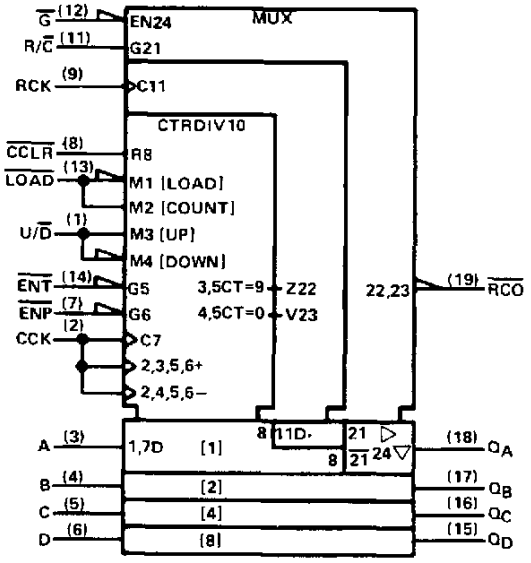


RCO OUTPUT

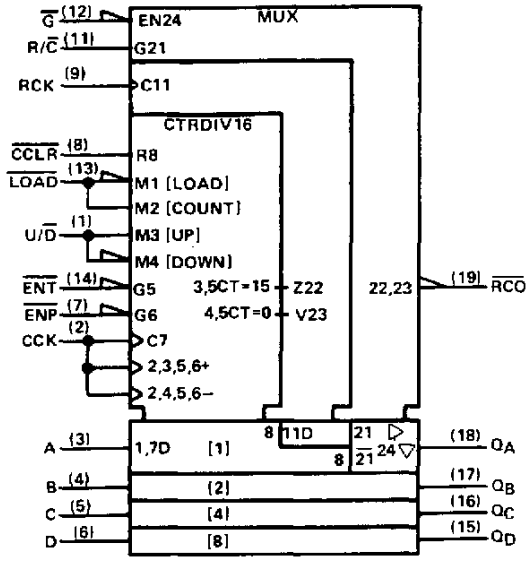


logic symbols†

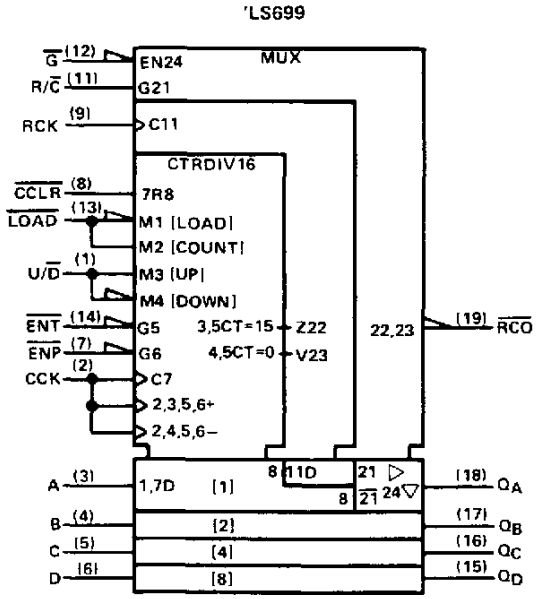
'LS696



'LS697

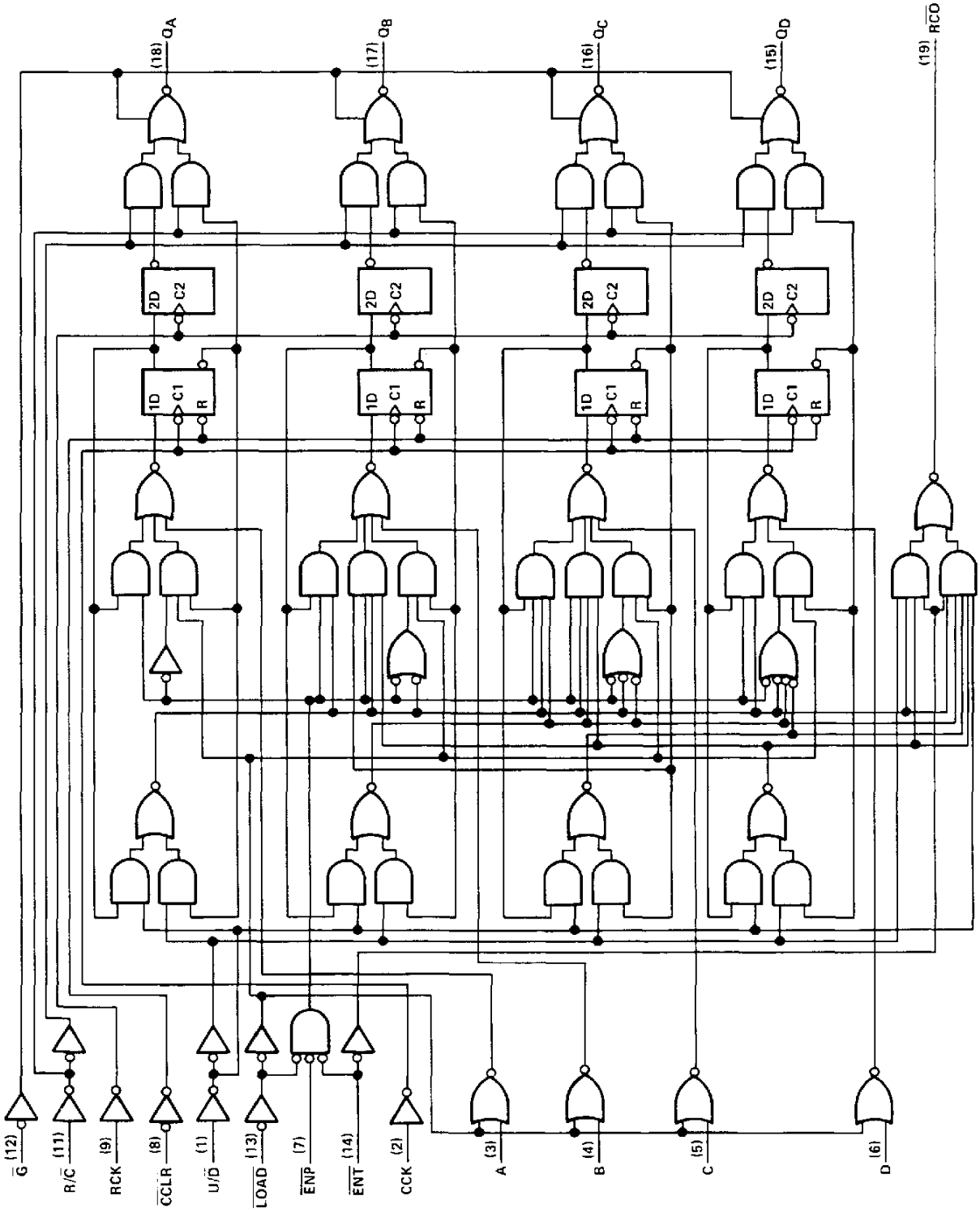


'LS699

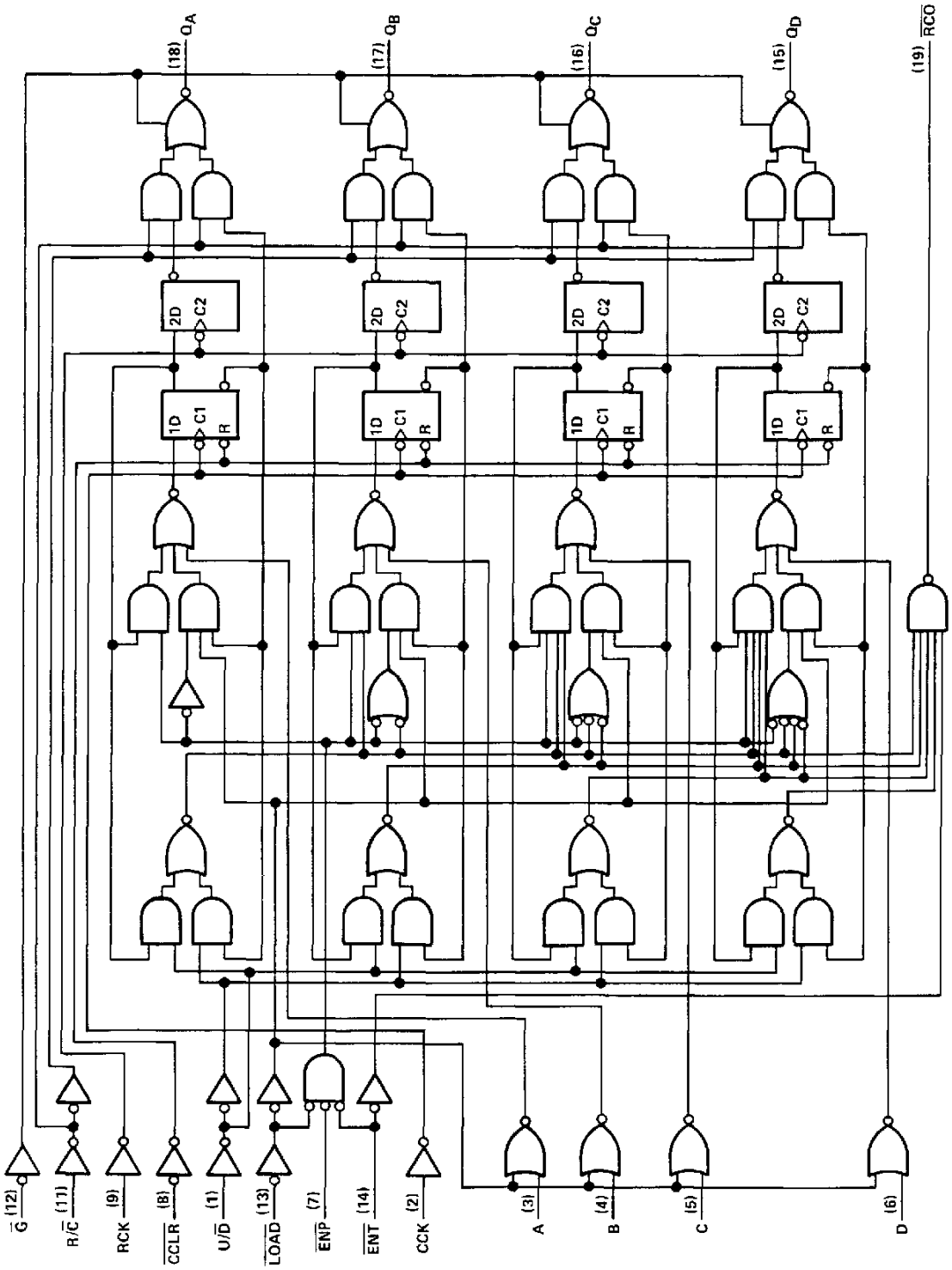


†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

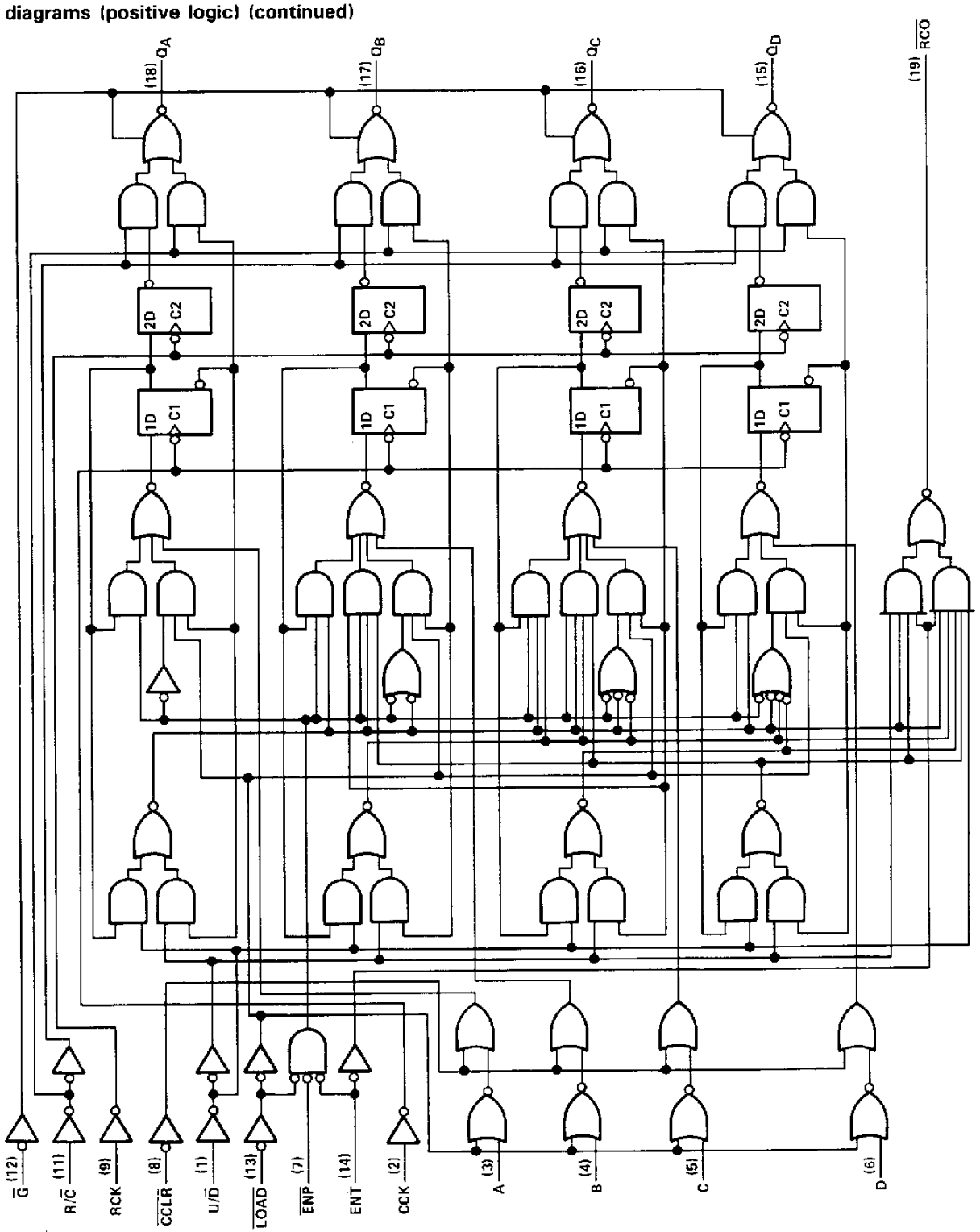
logic diagrams (positive logic)



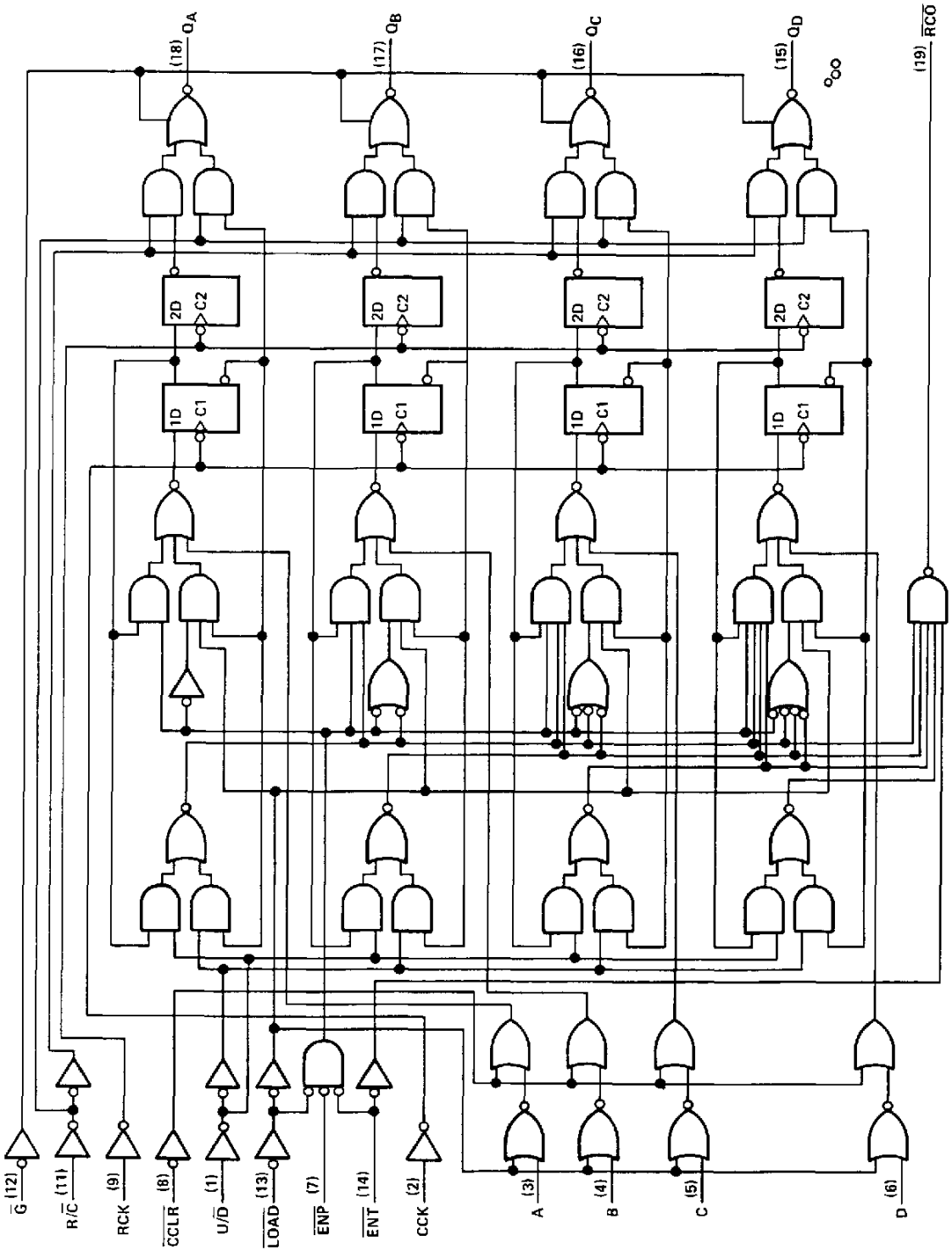
logic diagrams (positive logic) (continued)



logic diagrams (positive logic) (continued)



logic diagrams (positive logic) (continued)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS696, SN54LS697, SN54LS699 . . . −55°C to 125°C
SN74LS696, SN74LS697, SN74LS699 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		$\overline{RCO}$			−0.4			−0.4	
I_{OL}	Low-level output current	Q			12			24	mA
		$\overline{RCO}$			4			8	
f_{clock}	Clock frequency	CCK	0		20	0		20	MHz
		RCK	0		20	0		20	
t_w	Pulse duration	CCK high or low	25			25			ns
		RCK high or low	25			25			
		'LS696, 'LS697 $\overline{CCLR}$ low	20			20			
t_{su}	Setup time before CCK ↑	A thru D	30			30			ns
		$\overline{ENP}$ or $\overline{ENT}$	30			30			
		$\overline{LOAD}$	30			30			
		U/$\overline{D}$	35			35			
		'LS696, 'LS697, $\overline{CCLR}$ inactive	25			25			
		'LS699, $\overline{CCLR}$	30			30			
t_{su}	Setup time CCK ↑ before RCK ↑ (see Note 2)		30			30			ns
t_h	Hold time		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		$\overline{RCO}$		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V,	V_O=2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V,	V_O=0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 3		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 4		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 5		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.

4. I_{CCL} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I_{CCZ} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

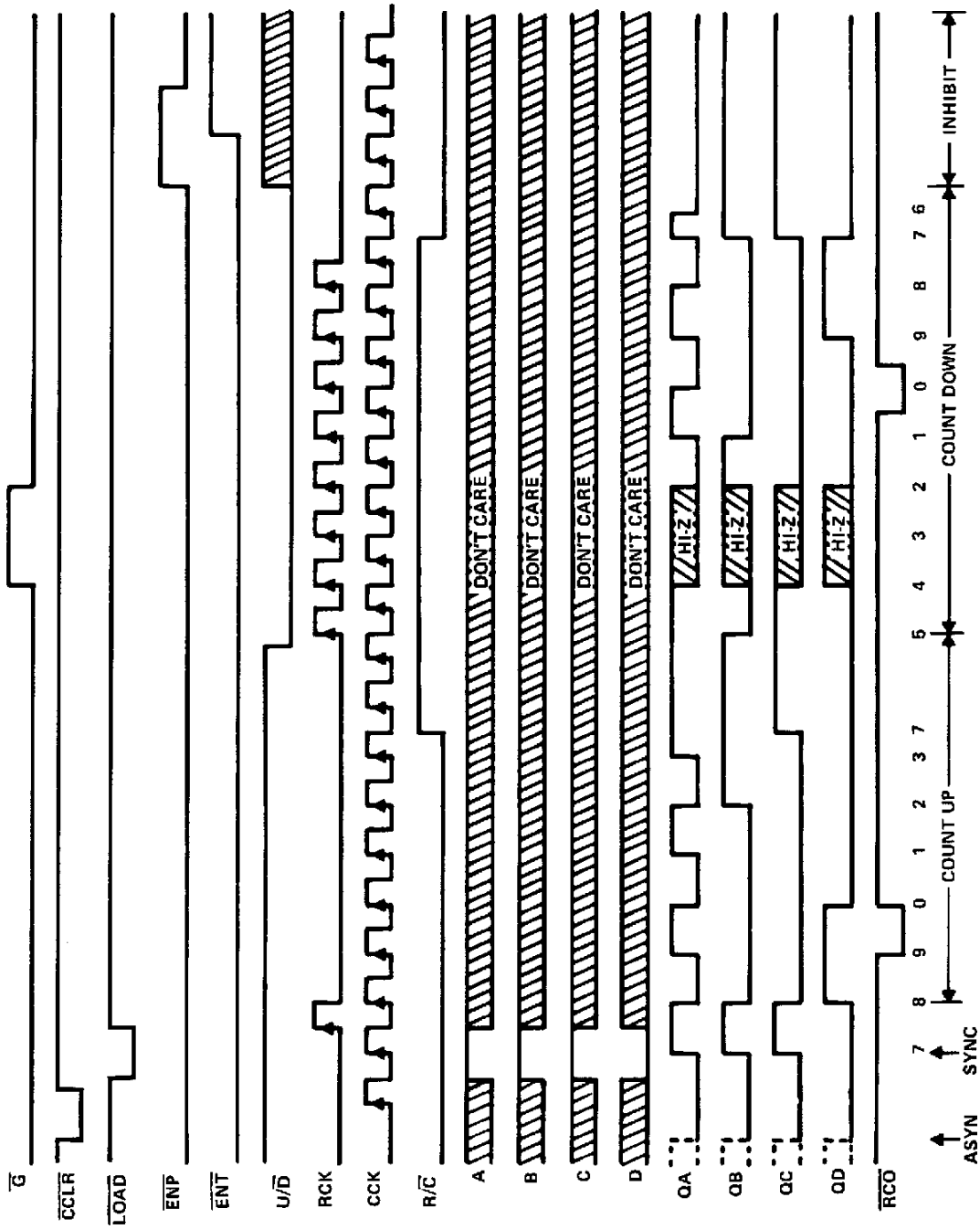
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697 MIN	'LS696, 'LS697 TYP	'LS696, 'LS697 MAX	'LS699 MIN	'LS699 TYP	'LS699 MAX	UNIT
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	ns
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			13	20		13	20	ns
t_{PHL}					13	20		13	20	ns
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	ns
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	ns

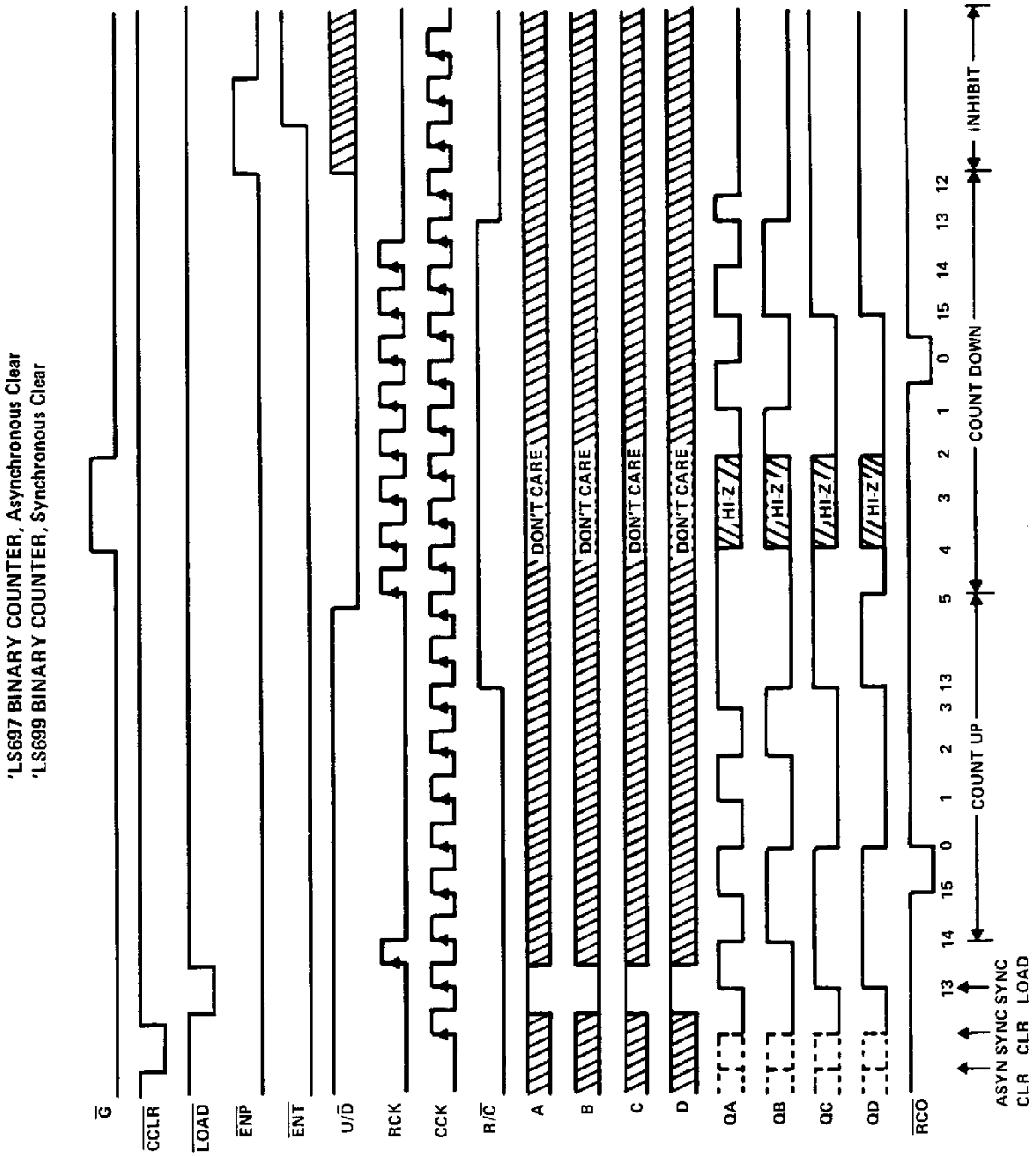
NOTE 6: Load circuits and voltage waveforms are shown in Section 1.

typical operating sequences

'LS696 DECADE COUNTER, Asynchronous Clear

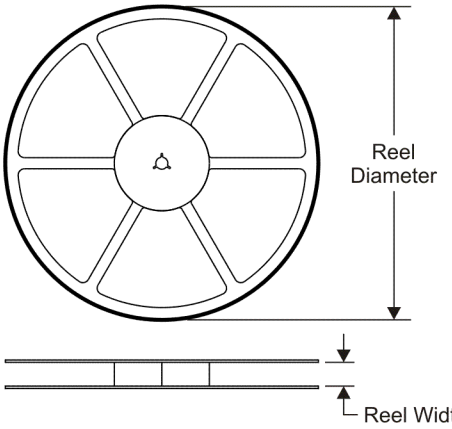


typical operating sequences (continued)

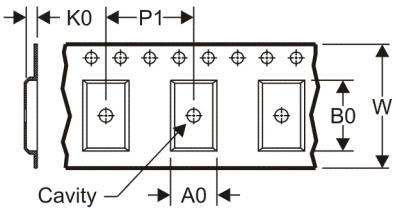


TAPE AND REEL INFORMATION

REEL DIMENSIONS

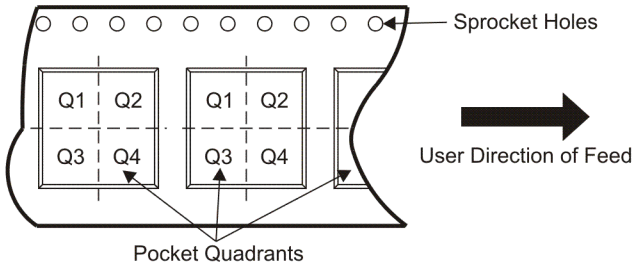


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

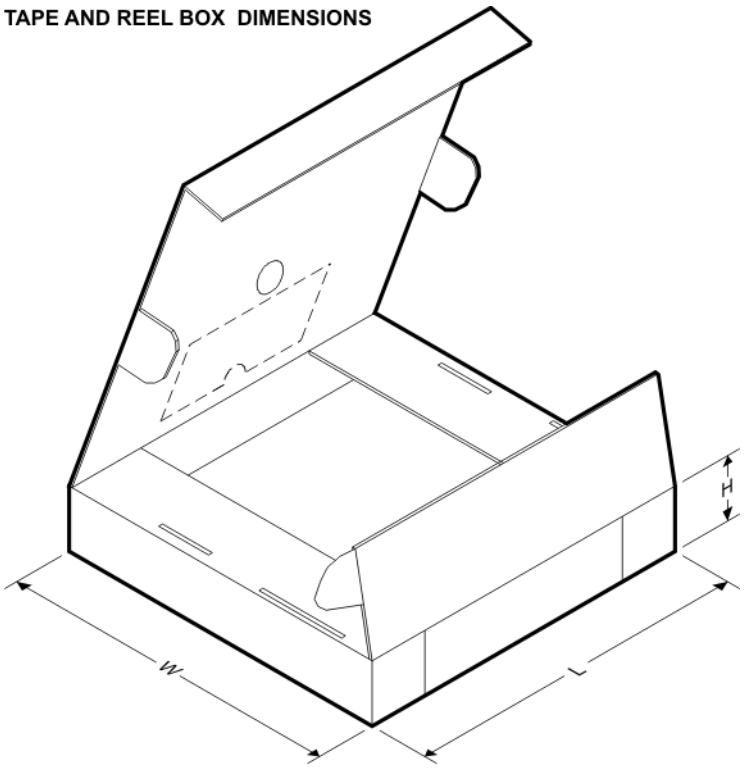
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS697NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS697NSR	SO	NS	20	2000	346.0	346.0	41.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS697DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS697
SN74LS697N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS697N
SNJ54LS697J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS697J

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54LS697, SN74LS697 :

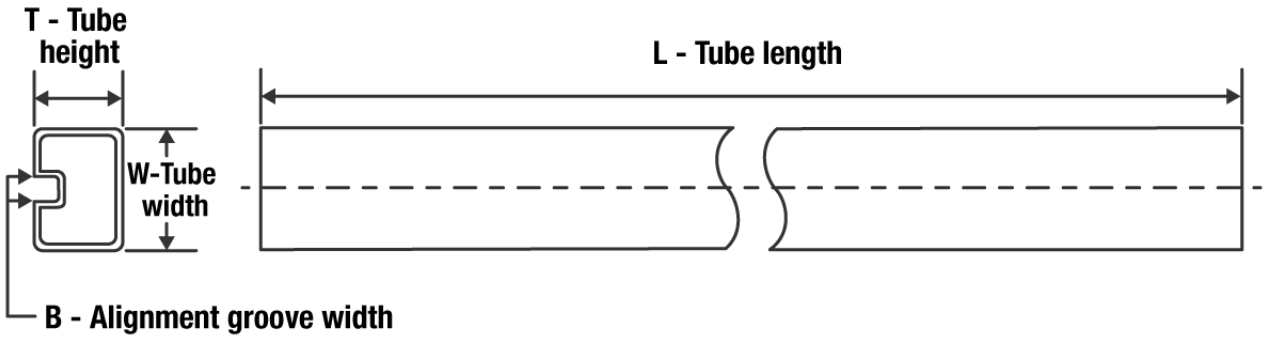
- Catalog : SN74LS697

- Military : SN54LS697

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



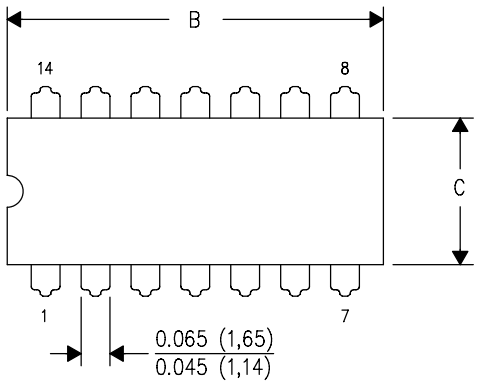
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LS697DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS697N	N	PDIP	20	20	506	13.97	11230	4.32

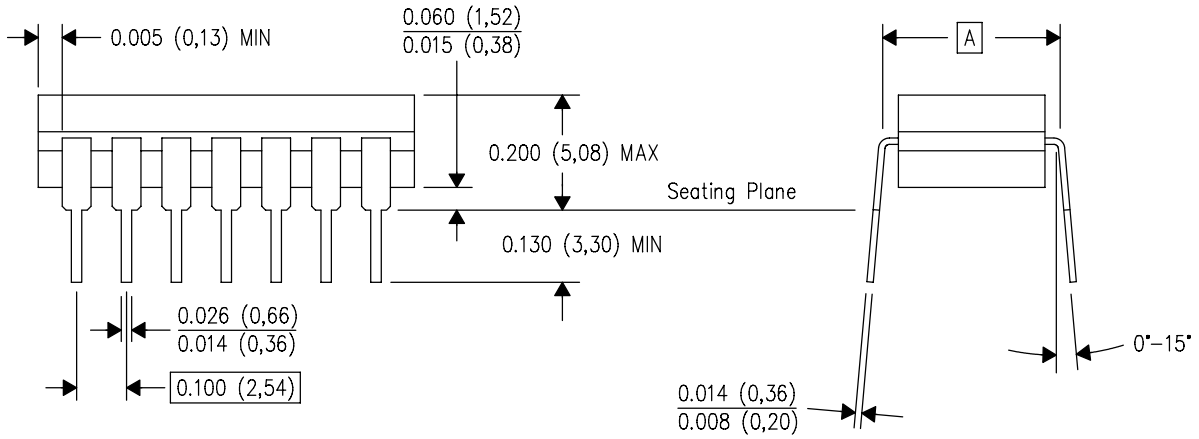
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



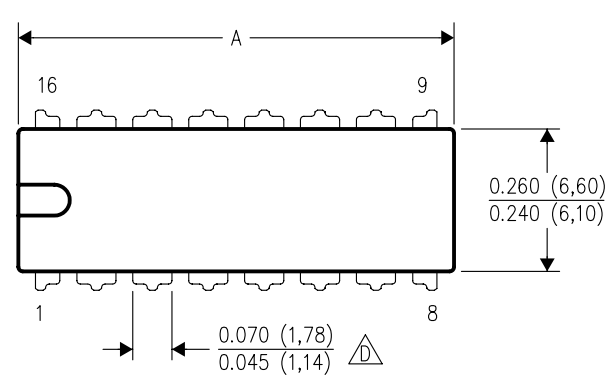
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

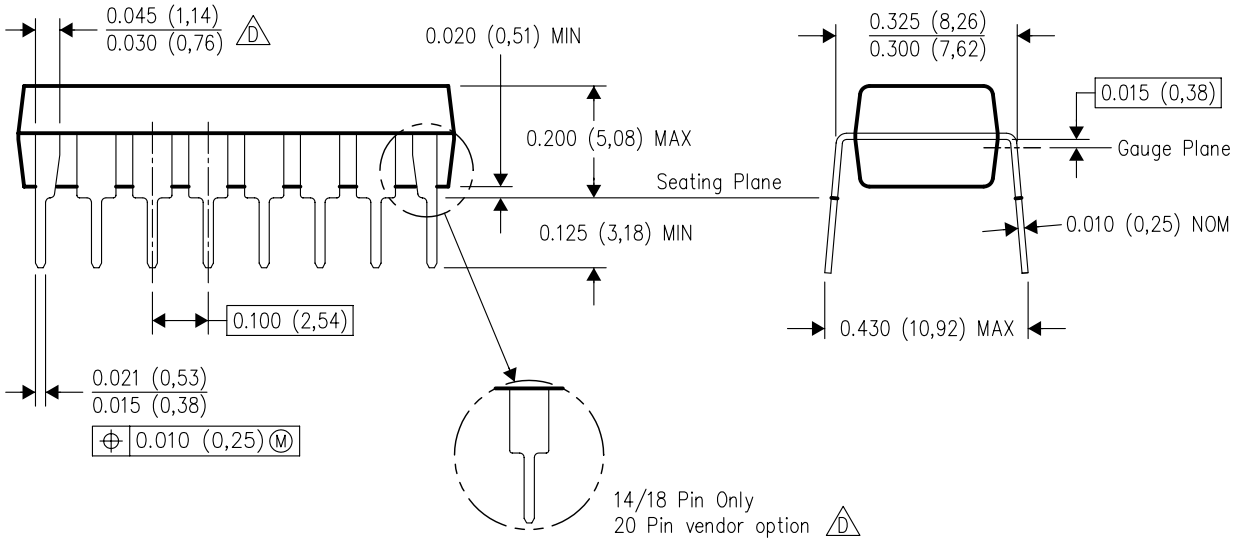
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

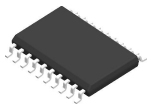


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

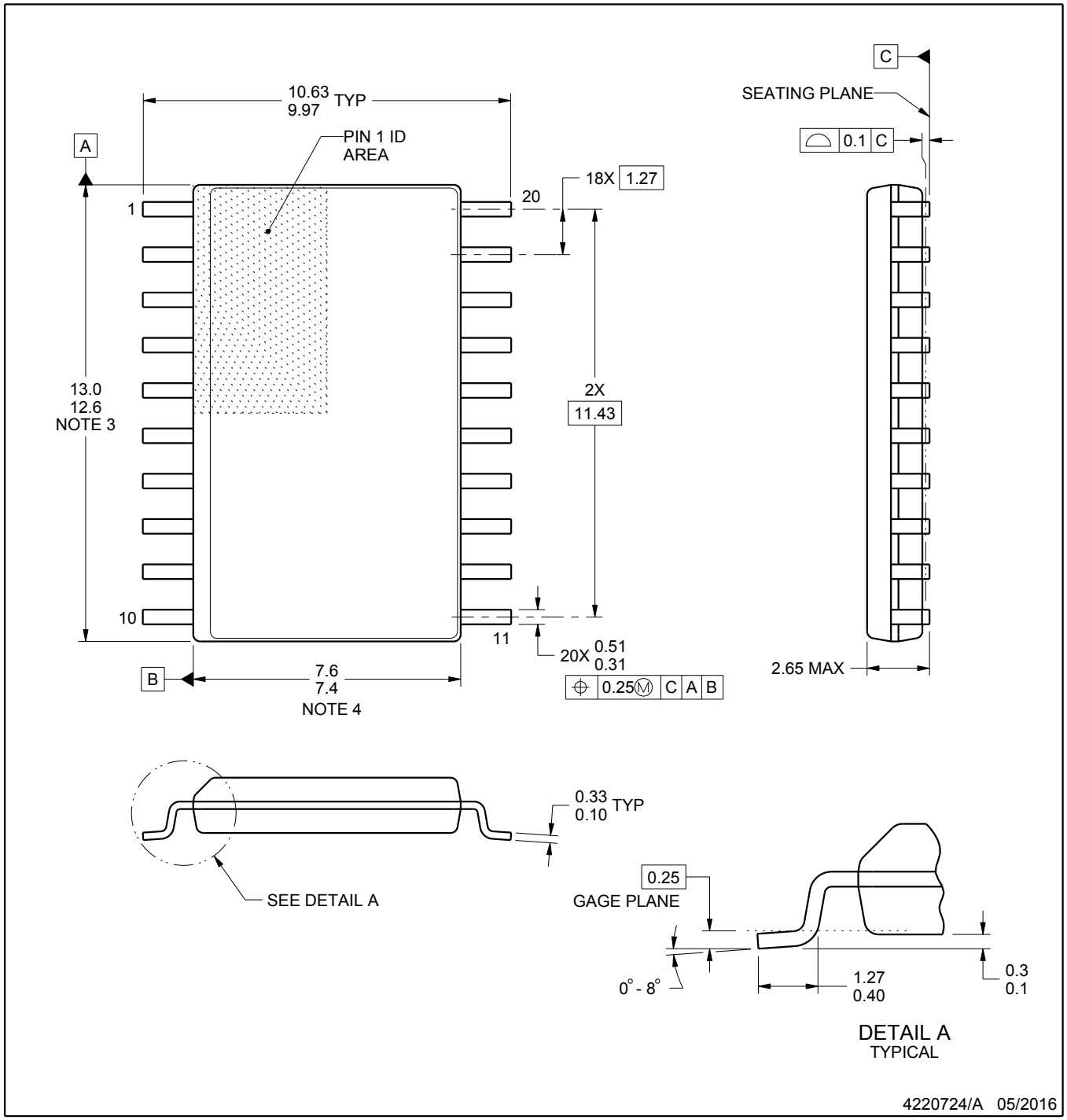


PACKAGE OUTLINE

DW0020A

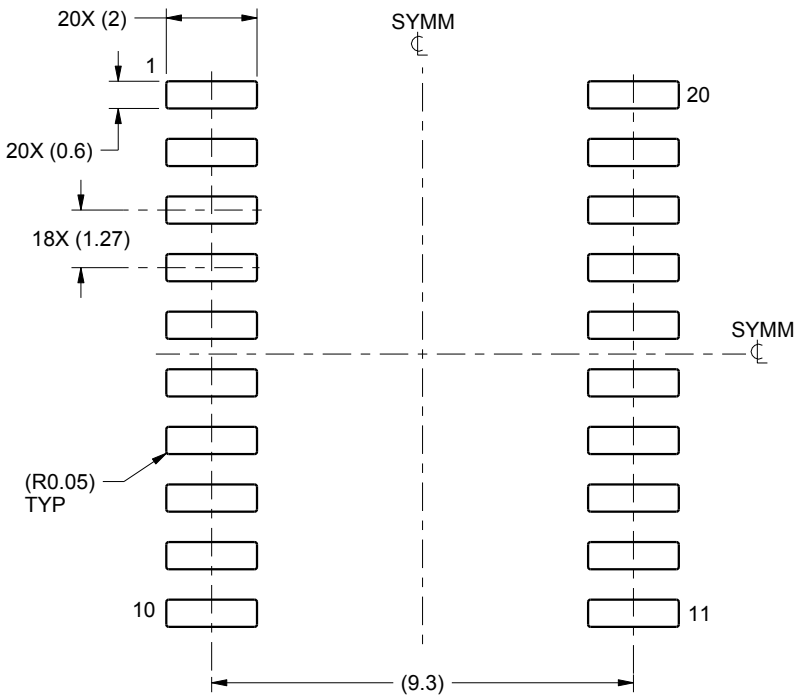
SOIC - 2.65 mm max height

SOIC

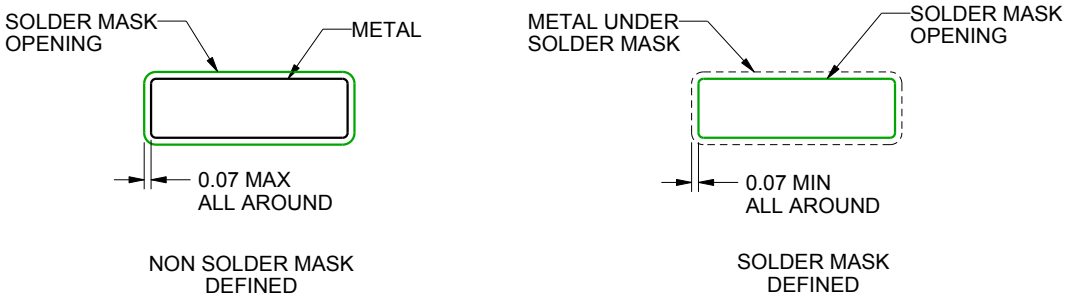


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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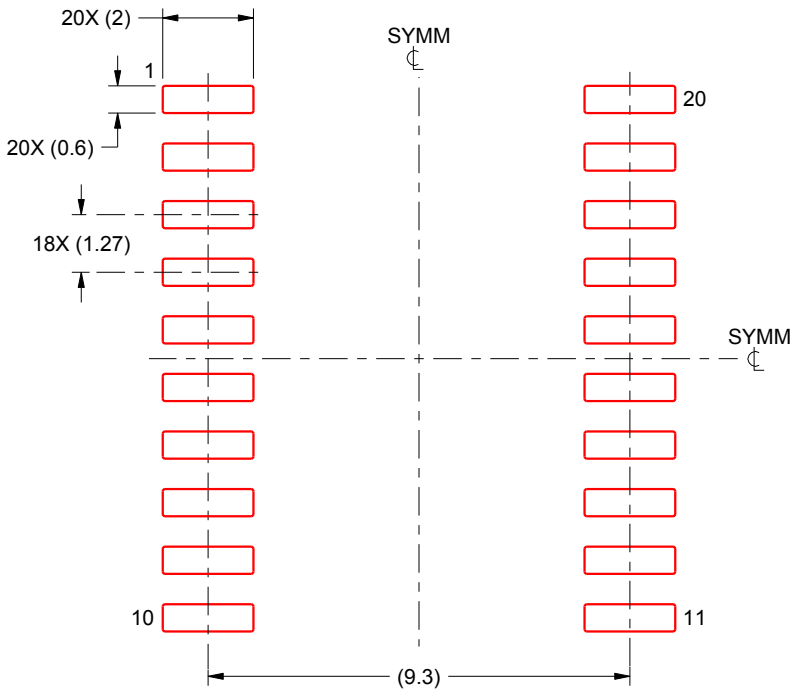
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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