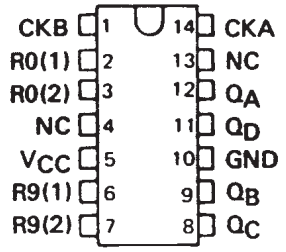
'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

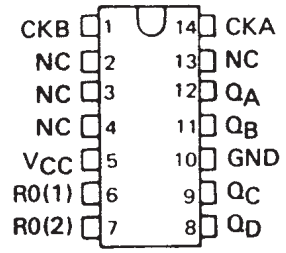
'93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

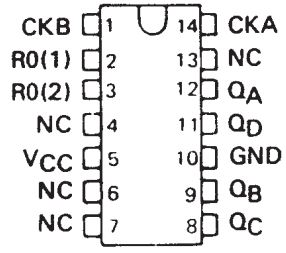
SN5490A, SN54LS90 . . . J OR W PACKAGE
SN7490A . . . N PACKAGE
SN74LS90 . . . D OR N PACKAGE
(TOP VIEW)



SN5492A, SN54LS92 . . . J OR W PACKAGE
SN7492A . . . N PACKAGE
SN74LS92 . . . D OR N PACKAGE
(TOP VIEW)



SN5493A, SN54LS93 . . . J OR W PACKAGE
SN7493 . . . N PACKAGE
SN74LS93 . . . D OR N PACKAGE
(TOP VIEW)



description

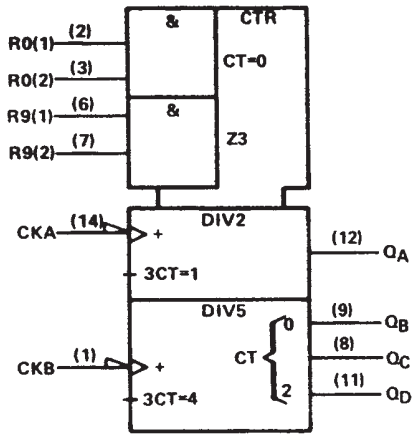
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

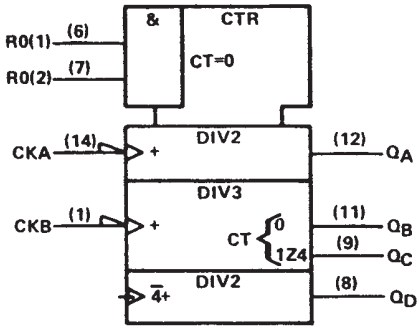
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A.

logic symbols†

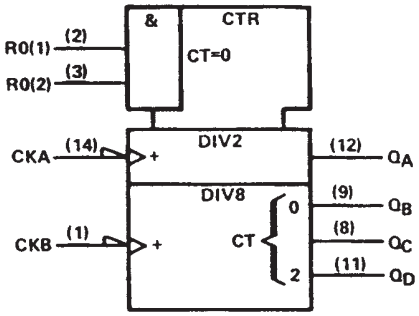
'90



'92



'93A, 'LS93



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

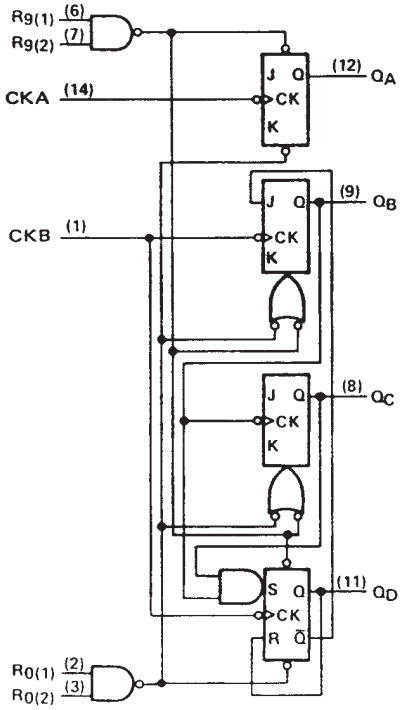
'93A, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

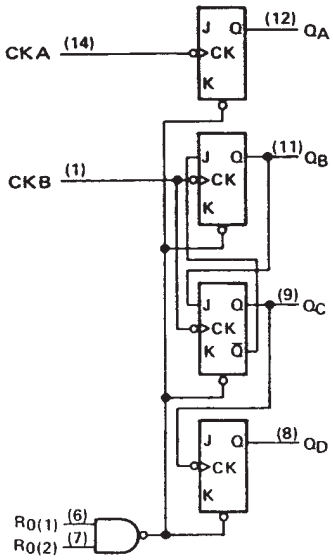
NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

logic diagrams (positive logic)

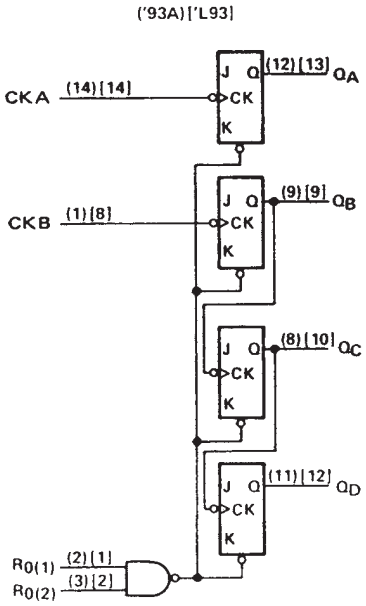
'90A, 'LS90



'92A, 'LS92



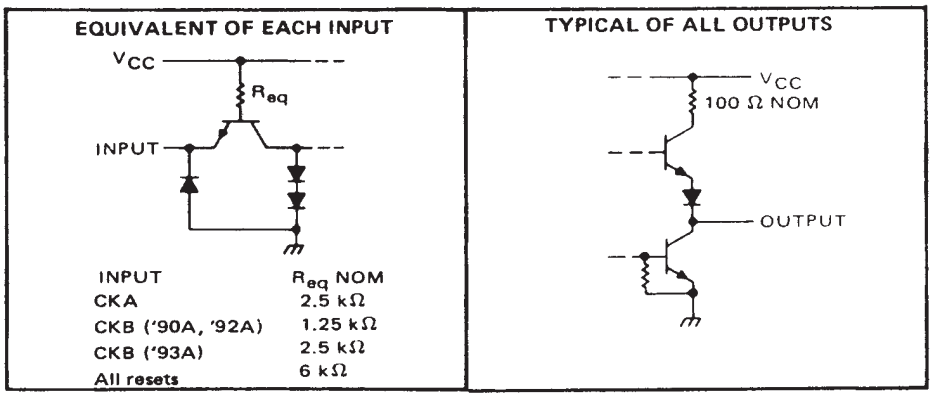
'93A, 'LS93



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in ( ) are for the 'LS93 and '93A and pin numbers shown in [ ] are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A

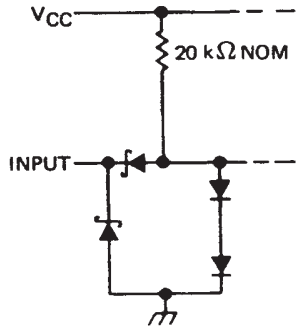


INPUT	R_{eq} NOM
CKA	2.5 kΩ
CKB ('90A, '92A)	1.25 kΩ
CKB ('93A)	2.5 kΩ
All resets	6 kΩ

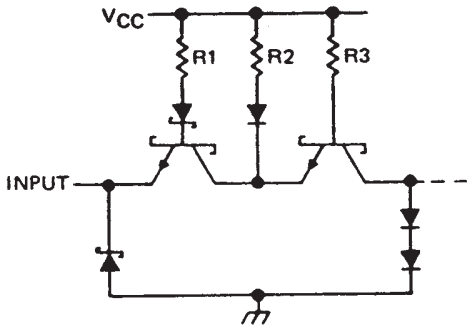
schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93

EQUIVALENT OF EACH RESET INPUT

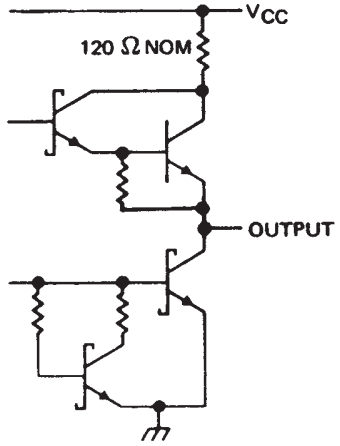


EQUIVALENT OF A AND B INPUTS



INPUT	NOMINAL VALUES R1	R2	R3
CKA	10 kΩ	10 kΩ	10 kΩ
CKB ('LS90, 'LS92)	6.7 kΩ	6.7 kΩ	5 kΩ
CKB ('LS93)	15 kΩ	15 kΩ	10 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ¶		TEST CONDITIONS†		'90A MIN	'90A TYP‡	'90A MAX	'92A MIN	'92A TYP‡	'92A MAX	'93A MIN	'93A TYP‡	'93A MAX	UNIT
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Any reset			40			40			40	μA
			CKA			80			80			80	
			CKB			120			120			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Any reset			−1.6			−1.6			−1.6	mA
			CKA			−3.2			−3.2			−3.2	
			CKB			−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
			SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CKA	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	CKA	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	CKB	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	CKB	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	CKB	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

† f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: R inputs . . . . . 7 V
A and B inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		CKA	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
		CKB						0.4			0.4	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		CKA						40			40	
		CKB						80			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		CKA						−2.4			−2.4	
		CKB						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3	'LS90		9	15		9	15	mA
					'LS92		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS93			SN74LS93			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		CKA or CKB	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		CKA or CKB						40			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		CKA						−2.4			−2.4	
		CKB						−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			9	15		9	15	mA

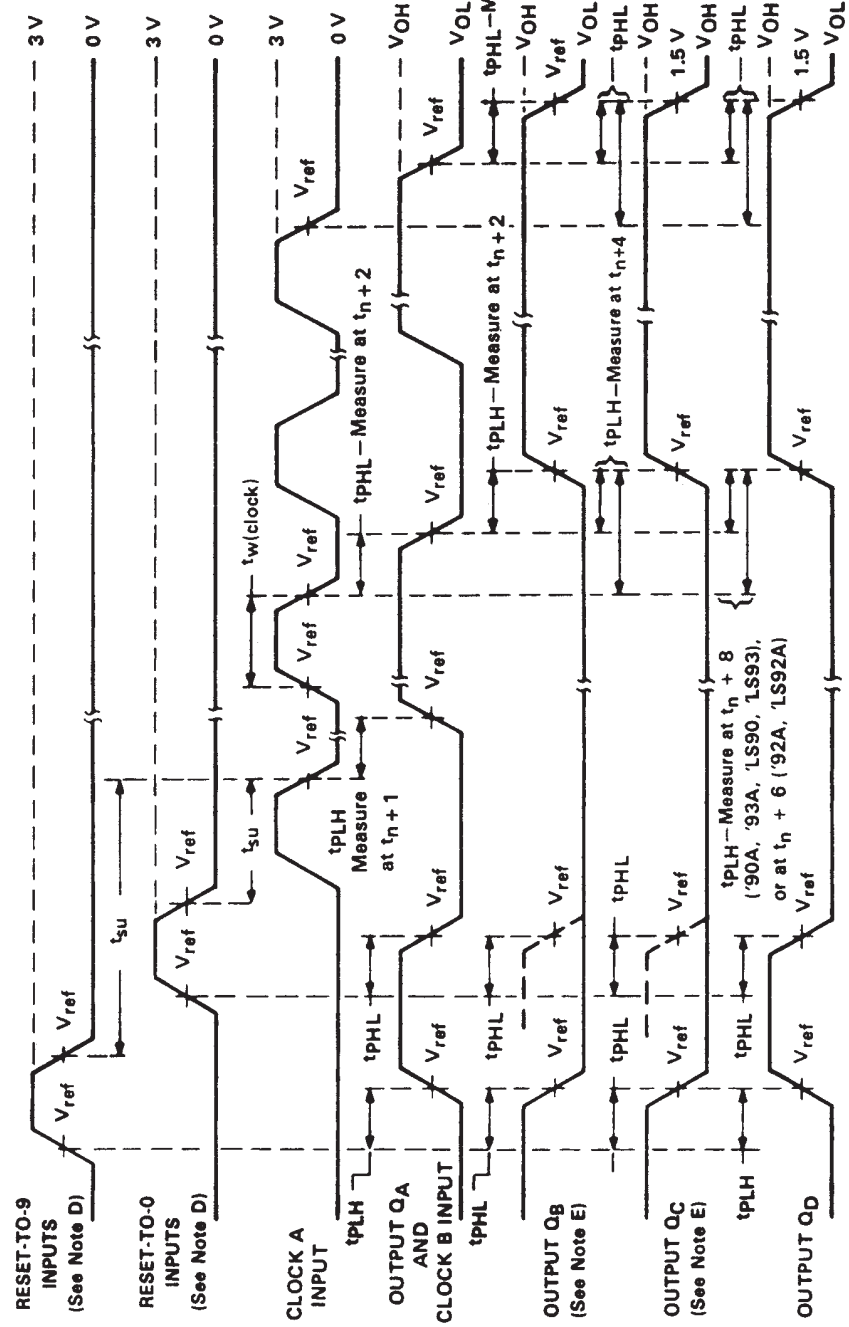
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CKA	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	CKA	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	CKB	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	CKB	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	CKB	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

#f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

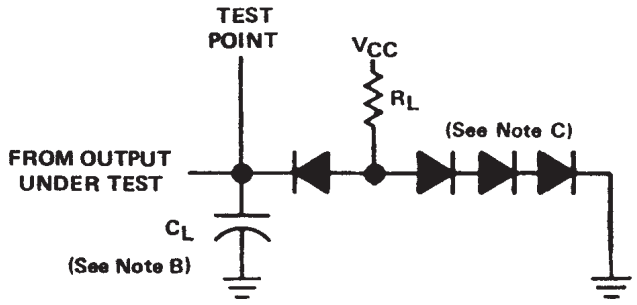
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \le 5$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \le 15$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'LS90, 'LS92, and 'LS93; V_{ref} = 1.3 V.

FIGURE 1A

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'LS90, 'LS92, and 'LS93; V_{ref} = 1.3 V.

FIGURE 1B

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7603201CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J
7700101CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J
7700101DA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W
JM38510/31501BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31501BCA
JM38510/31502BCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BCA
JM38510/31502BDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 31502BDA
SN54LS90J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS90J
SN54LS93J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS93J
SN74LS90D	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LS90
SN74LS90DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS90
SN74LS90N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS90N
SN74LS92D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS92
SN74LS92N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS92N
SN74LS92NSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS92
SN74LS93D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS93
SN74LS93N	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS93N
SNJ54LS90J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7603201CA SNJ54LS90J
SNJ54LS93J	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101CA SNJ54LS93J
SNJ54LS93W	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700101DA SNJ54LS93W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS90, SN54LS93, SN74LS90, SN74LS93 :

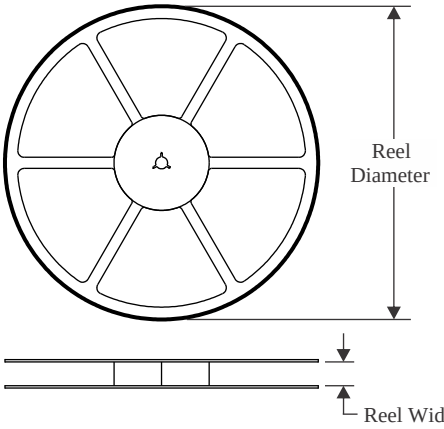
- Catalog : SN74LS90, SN74LS93
- Military : SN54LS90, SN54LS93

NOTE: Qualified Version Definitions:

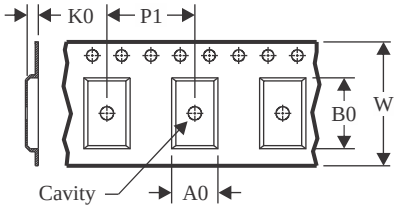
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

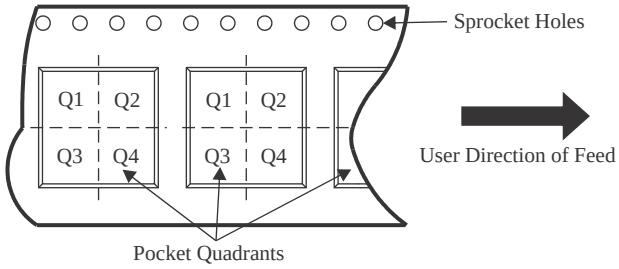


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

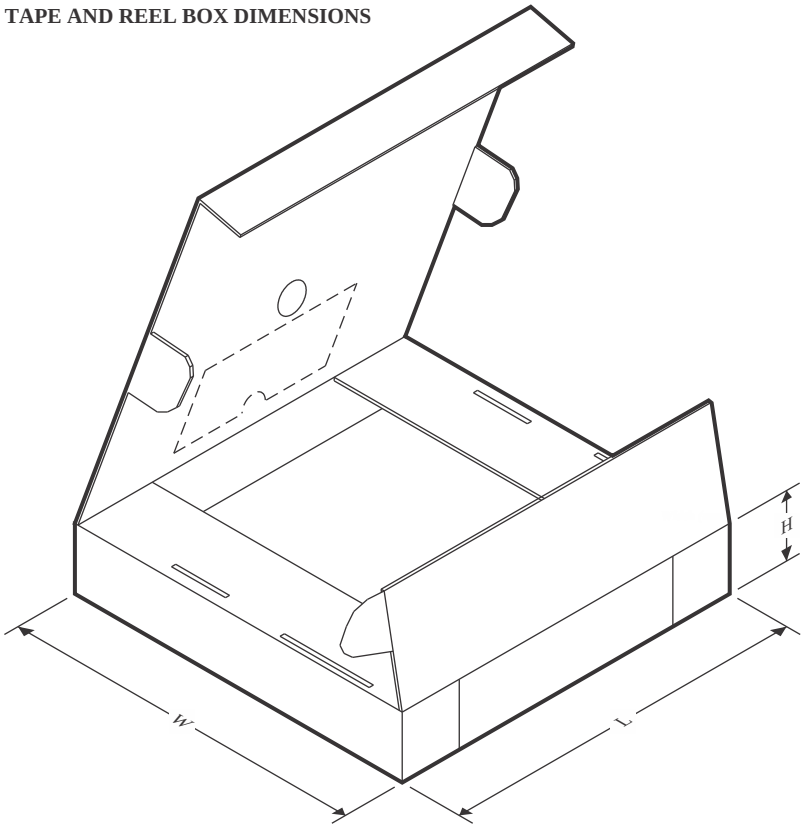
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS90DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS92NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

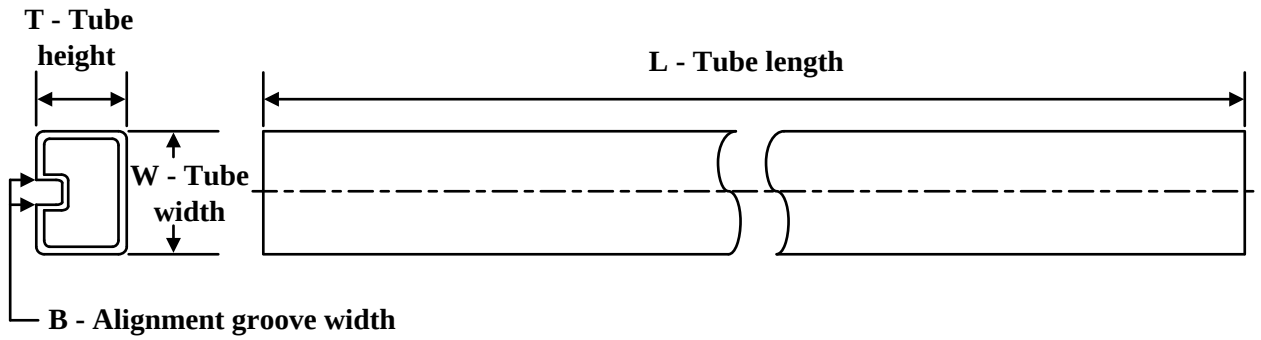
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

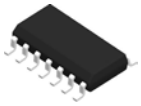
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS90DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LS92NSR	SOP	NS	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
7700101DA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
M38510/31502BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS90NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS92N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93D	D	SOIC	14	50	506.6	8	3940	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SN74LS93N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54LS93W	W	CFP	14	25	506.98	26.16	6220	NA

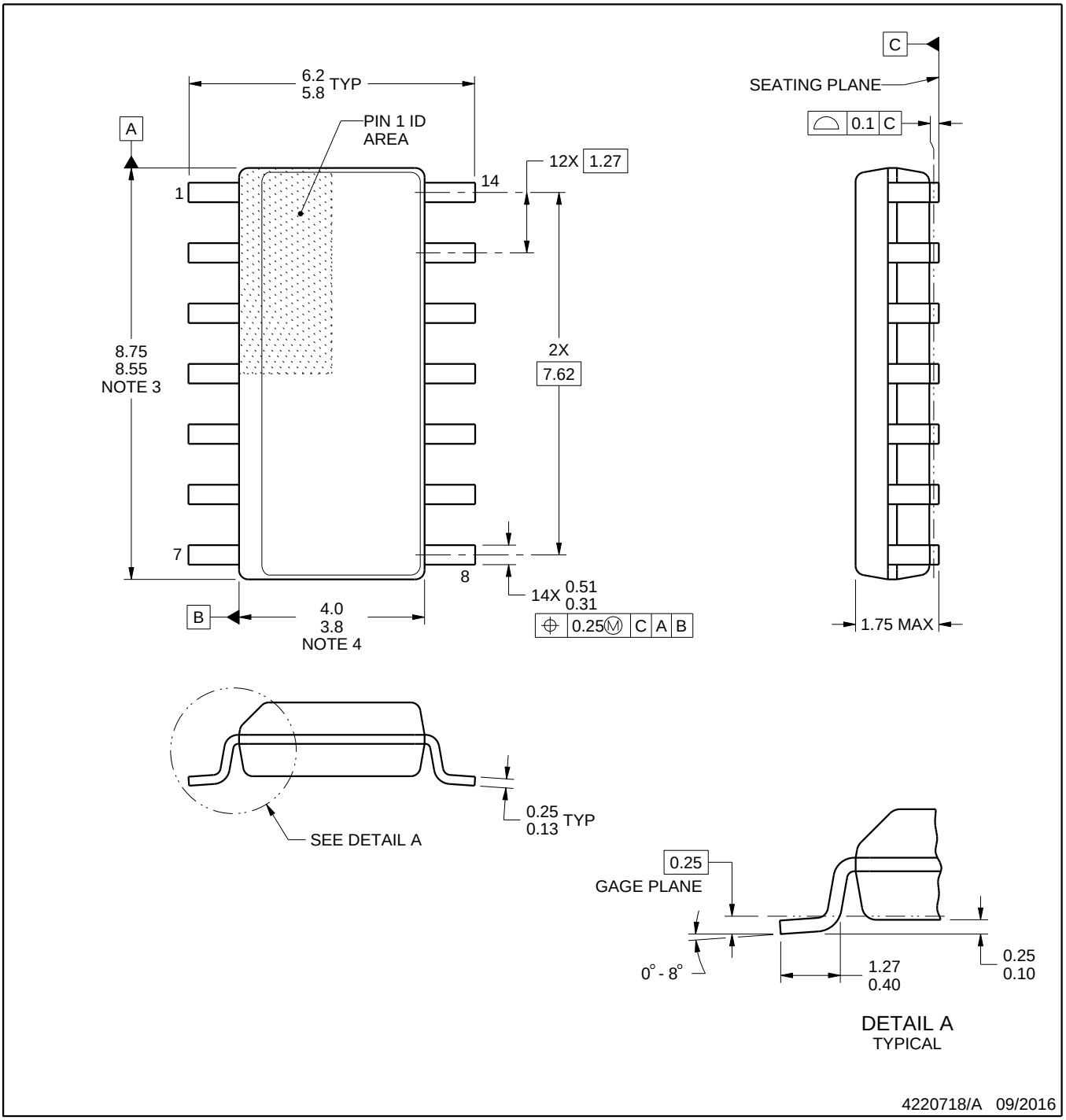


PACKAGE OUTLINE

D0014A

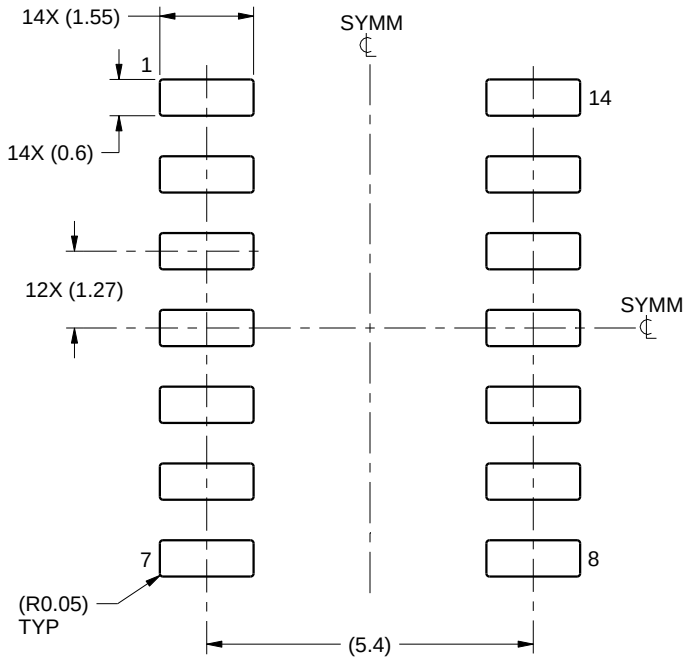
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

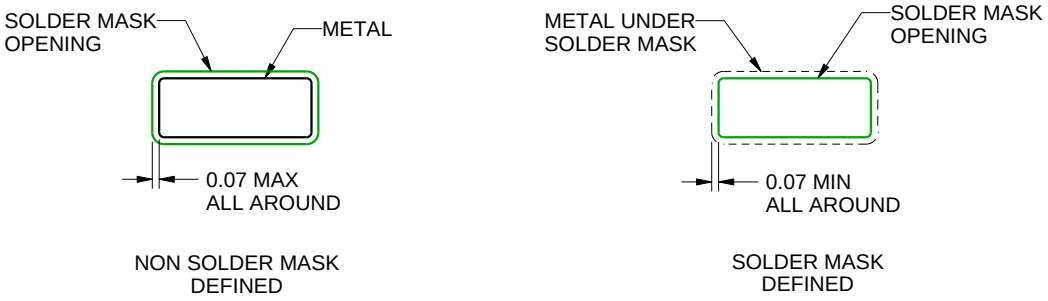


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

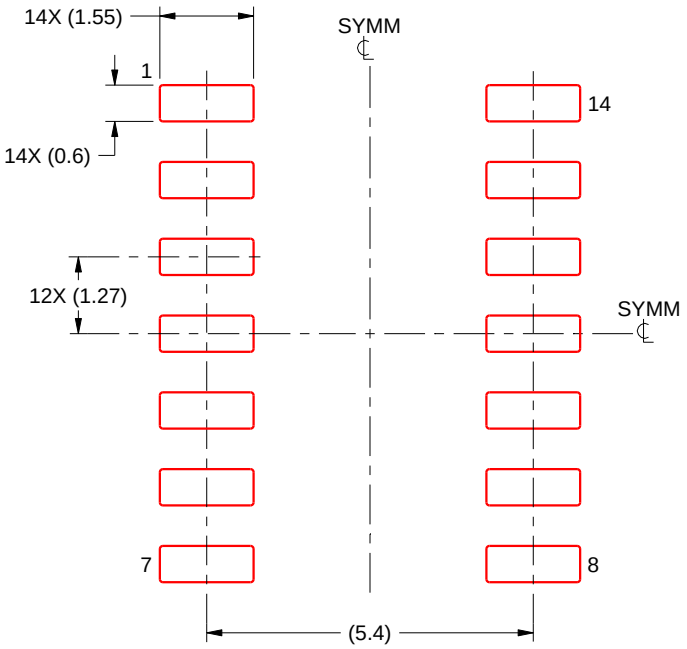
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

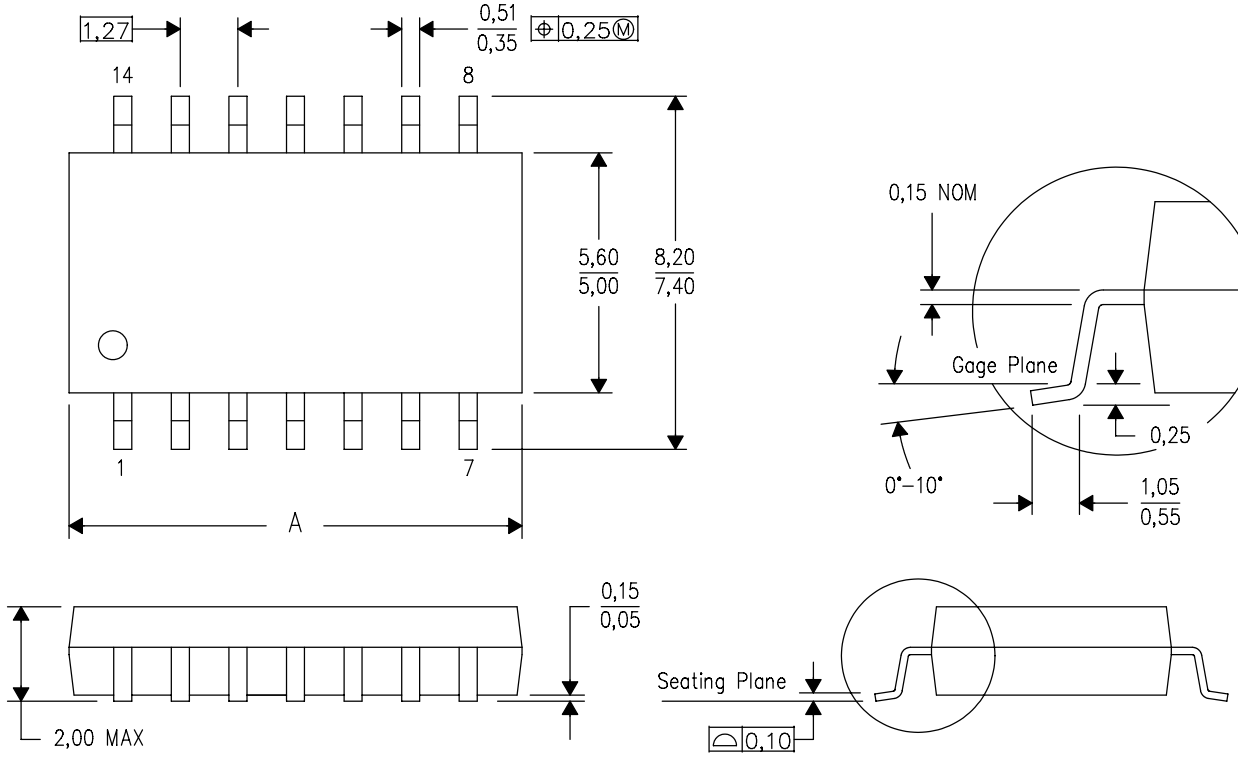
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

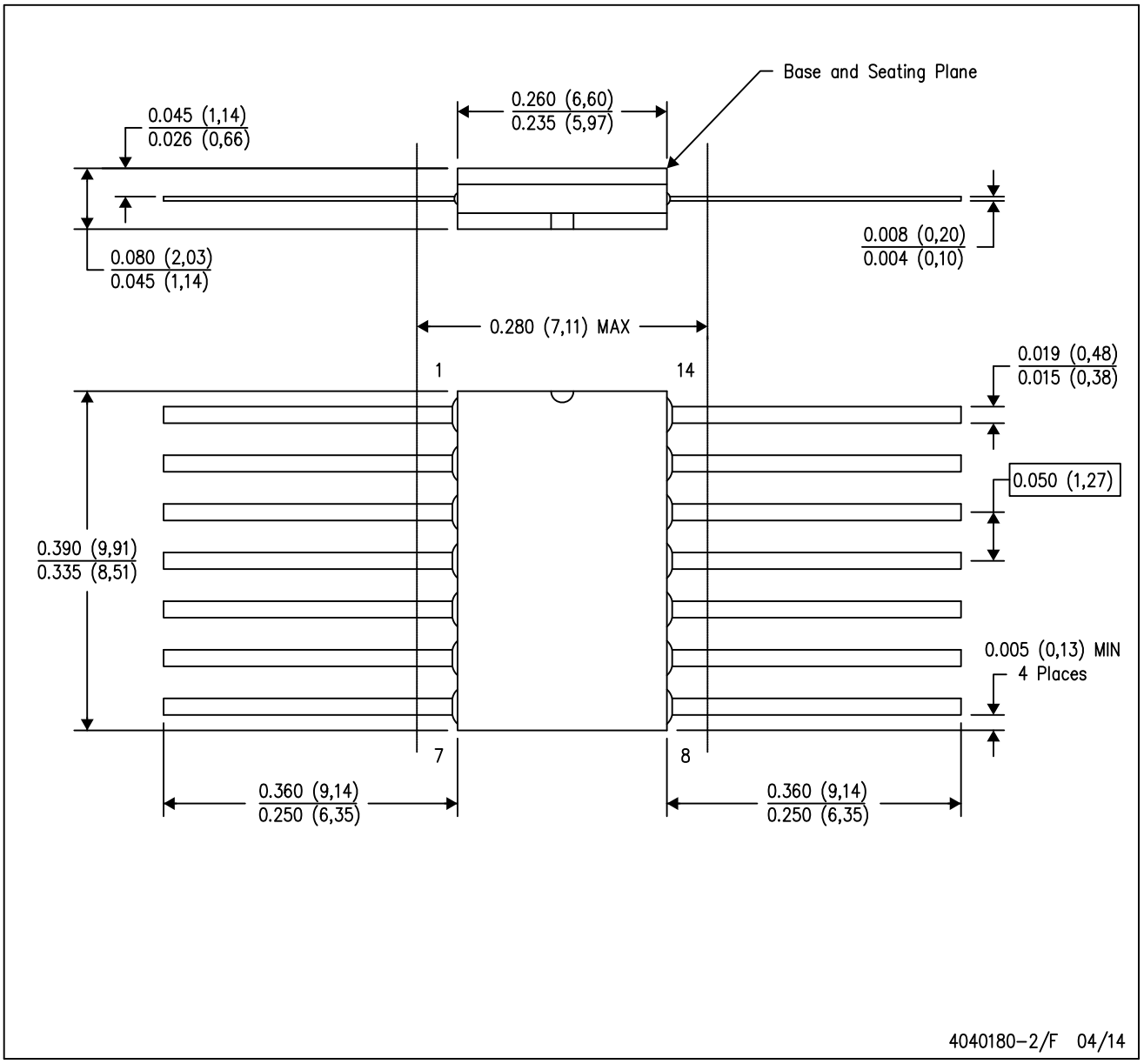


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

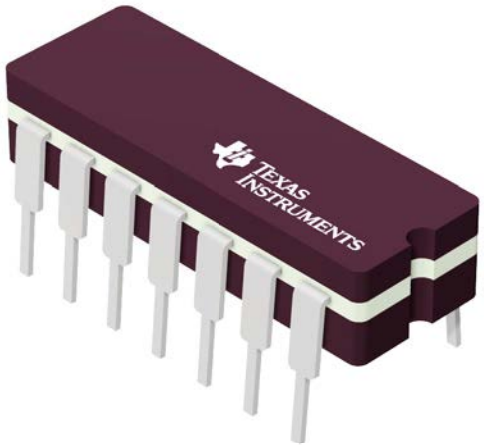


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

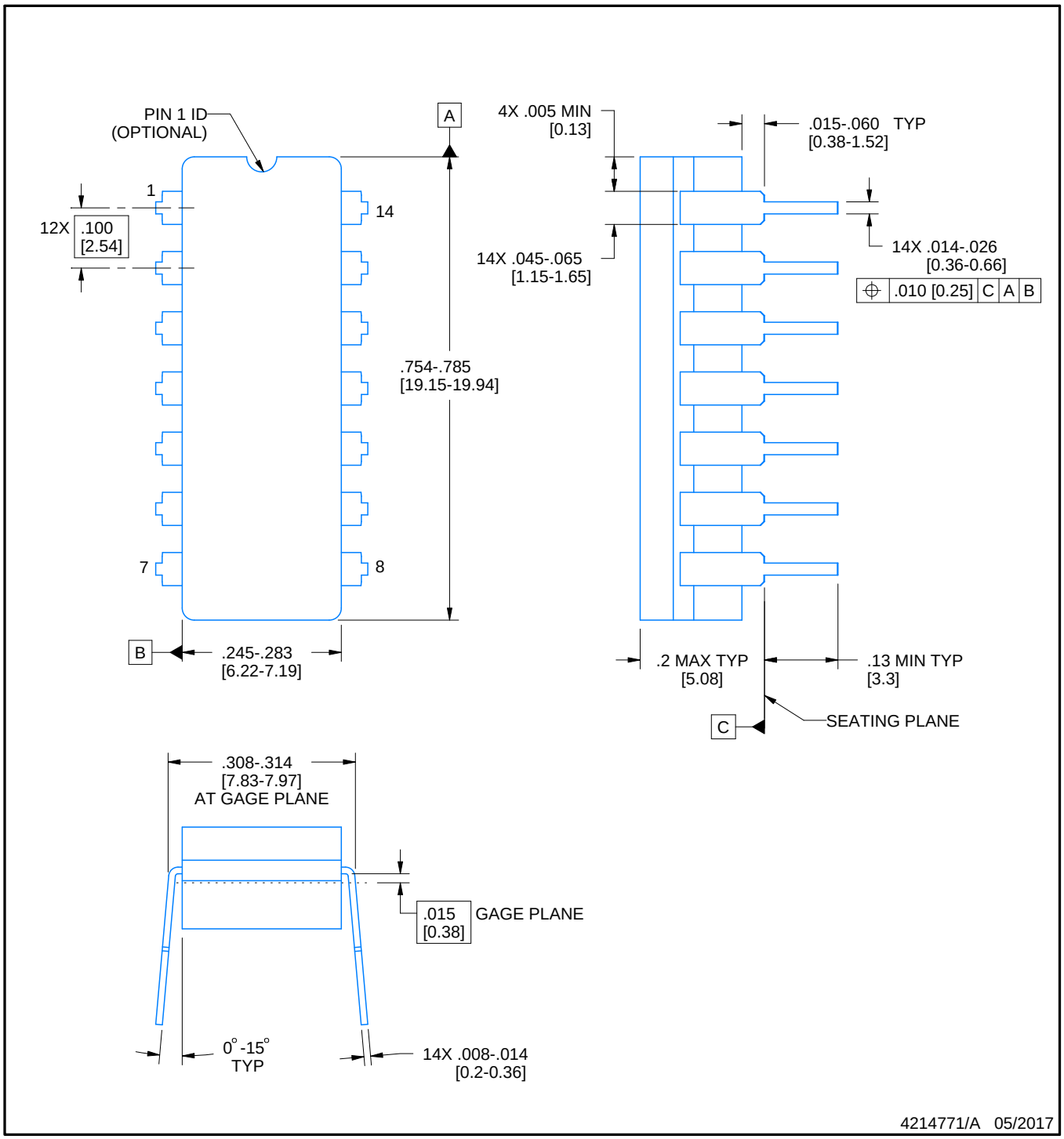
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

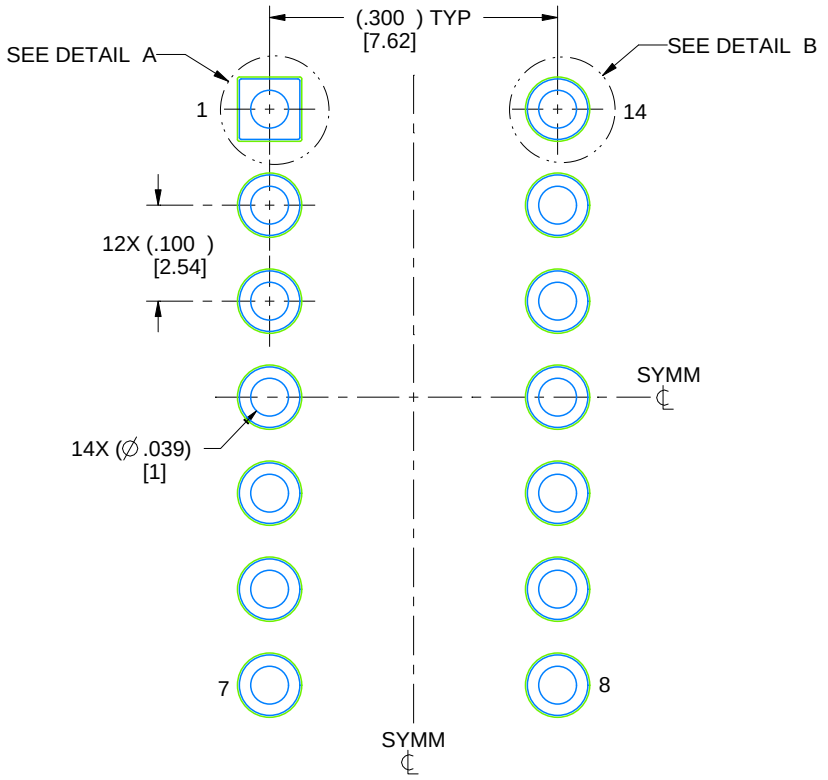
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

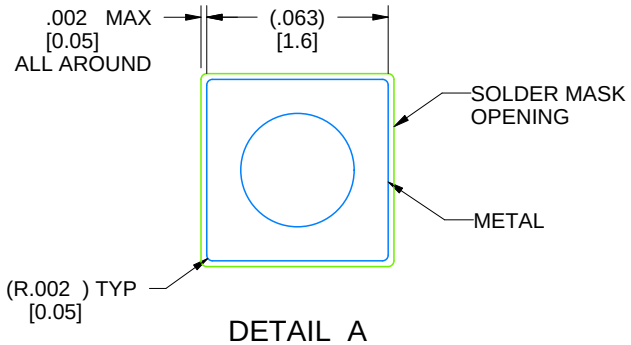
J0014A

CDIP - 5.08 mm max height

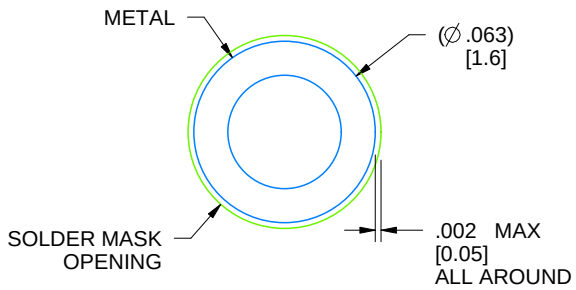
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



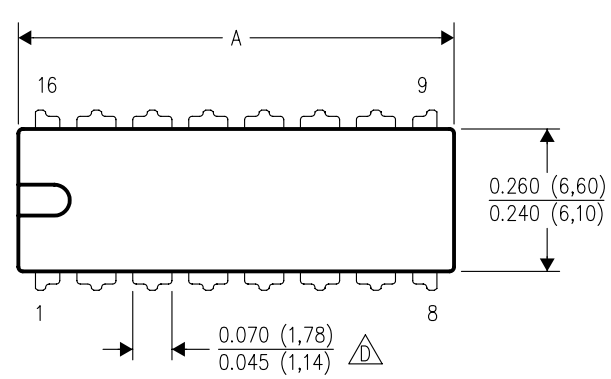
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

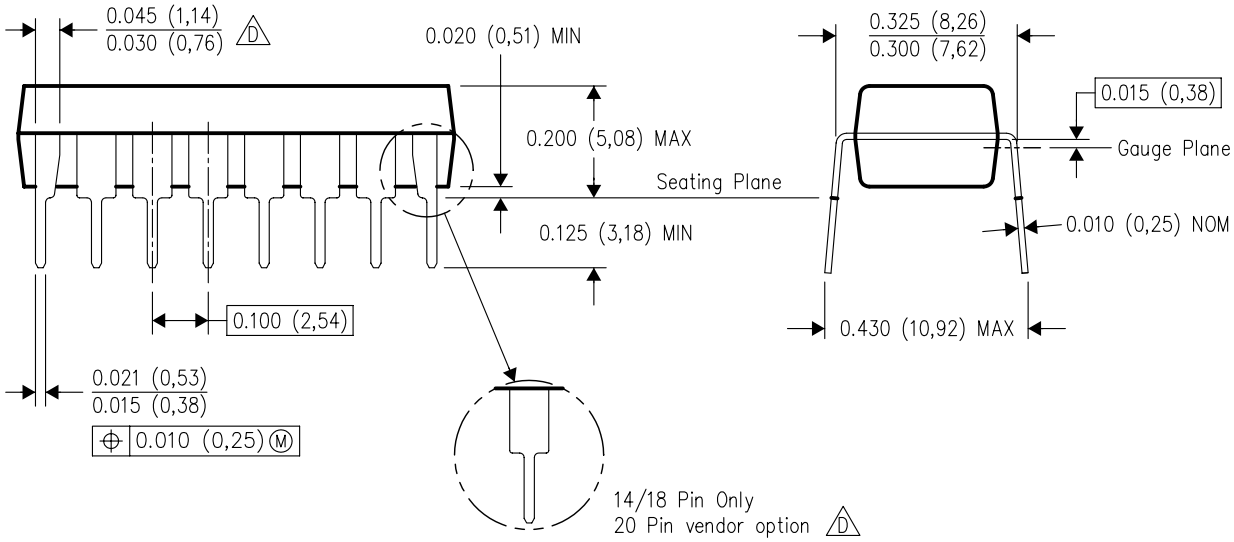
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265