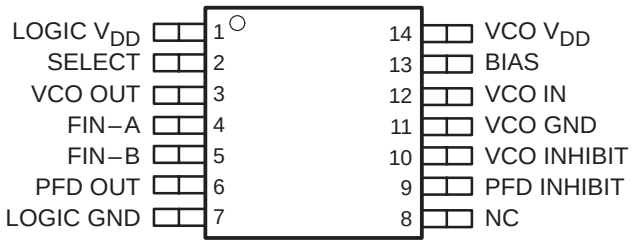
- **Voltage-Controlled Oscillator (VCO) Section:**
  - **Complete Oscillator Using Only One External Bias Resistor (R_{BIAS})**
  - **Lock Frequency:**
    22 MHz to 50 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1 Output)
    11 MHz to 25 MHz (V_{DD} = 5 V ±5%, T_A = –20°C to 75°C, ×1/2 Output)
  - **Output Frequency . . . ×1 and ×1/2 Selectable**
- **Phase-Frequency Detector (PFD) Section Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump**
- **Independent VCO, PFD Power-Down Mode**
- **Thin Small-Outline Package (14 terminal)**
- **CMOS Technology**
- **Typical Applications:**
  - **Frequency Synthesis**
  - **Modulation/Demodulation**
  - **Fractional Frequency Division**
- **Application Report Available†**
- **CMOS Input Logic Level**

PW PACKAGE†
(TOP VIEW)

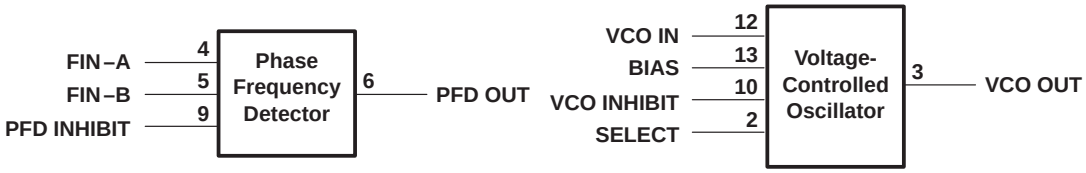


† Available in tape and reel only and ordered as the TLC2932IPWLE.
NC – No internal connection

description

The TLC2932 is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The VCO has a 1/2 frequency divider at the output stage. The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions, which can be used as a power-down mode. The TLC2932 is suitable for use as a high-performance PLL due to the high speed and stable oscillation capability of the device.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE
	SMALL OUTLINE (PW)
–20°C to 75°C	TLC2932IPWLE

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† TLC2932 Phase-Locked-Loop Building Block With Analog Voltage-Controlled Oscillator and Phase Frequency Detector (SLAA011).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
FIN–A	4	I	Input reference frequency $f_{(REF\ IN)}$ is applied to FIN–A.
FIN–B	5	I	Input for VCO external counter output frequency $f_{(FIN-B)}$. FIN–B is nominally provided from the external counter.
LOGIC GND	7		GND for the internal logic.
LOGIC V_{DD}	1		Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.
NC	8		No internal connection.
PFD INHIBIT	9	I	PFD inhibit control. When PFD INHIBIT is high, PFD output is in the high-impedance state, see Table 3.
PFD OUT	6	O	PFD output. When the PFD INHIBIT is high, PFD output is in the high-impedance state.
BIAS	13	I	Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.
SELECT	2	I	VCO output frequency select. When SELECT is high, the VCO output frequency is $\times$1/2 and when low, the output frequency is $\times$1, see Table 1.
VCO IN	12	I	VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.
VCO INHIBIT	10	I	VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 2).
VCO GND	11		GND for VCO.
VCO OUT	3	O	VCO output. When the VCO INHIBIT is high, VCO output is low.
VCO V_{DD}	14		Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.

detailed description

VCO oscillation frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. The bias resistor value for the minimum temperature coefficient is nominally 3.3 kΩ with 3-V at the VCO V_{DD} terminal and nominally 2.2 kΩ with 5-V at the VCO V_{DD} terminal. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

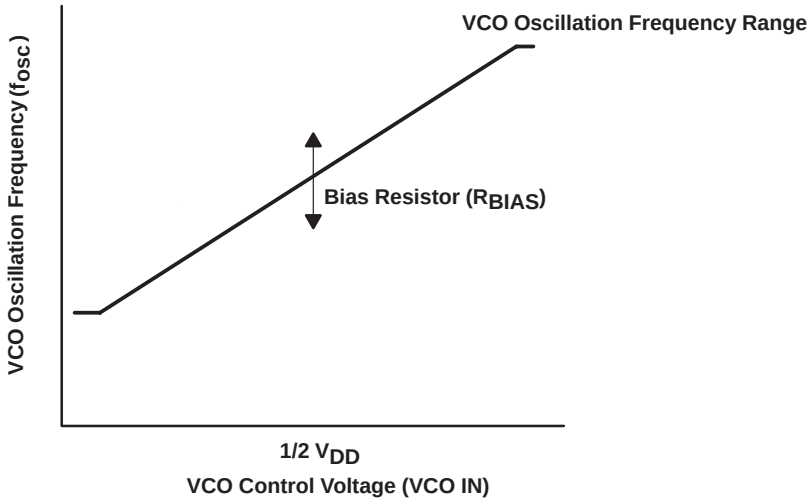


Figure 1. VCO Oscillation Frequency

VCO output frequency 1/2 divider

The TLC2932 SELECT terminal sets the f_{osc} or 1/2 f_{osc} VCO output frequency as shown in Table 1. The 1/2 f_{osc} output should be used for minimum VCO output jitter.

Table 1. VCO Output 1/2 Divider Function

SELECT	VCO OUTPUT
Low	f_{osc}
High	1/2 f_{osc}

VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode, refer to Table 2.

Table 2. VCO Inhibit Function

VCO INHIBIT	VCO OSCILLATOR	VCO OUTPUT	$I_{DD(VCO)}$
Low	Active	Active	Normal
High	Stopped	Low level	Power Down

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN–A and FIN–B as shown in Figure 2. Nominally the reference is supplied to FIN–A, and the frequency from the external counter output is fed to FIN–B.

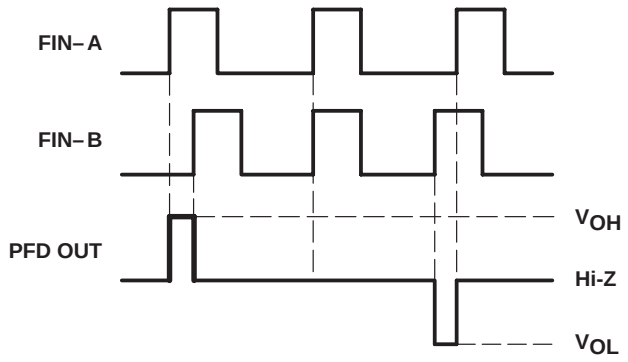


Figure 2. PFD Function Timing Chart

PFD output control

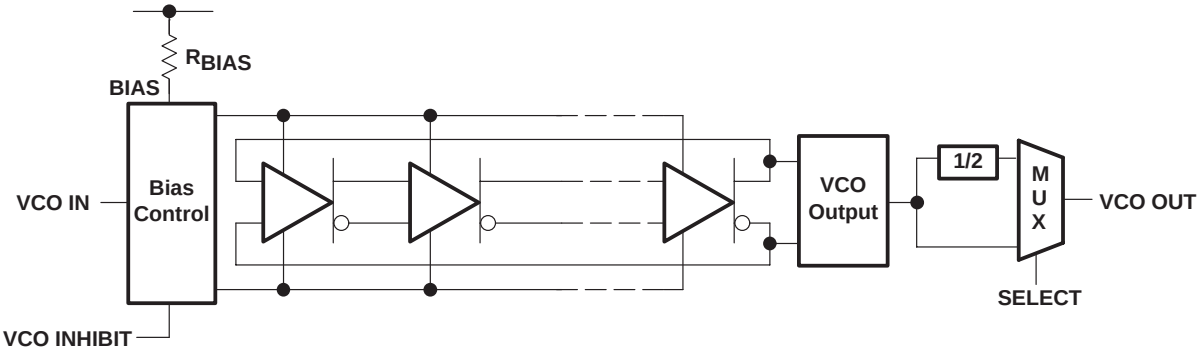
A high level on the PFD INHIBIT terminal places the PFD output in the high-impedance state and the PFD stops phase detection as shown in Table 3. A high level on the PFD INHIBIT terminal also can be used as the power-down mode for the PFD.

Table 3. VCO Output Control Function

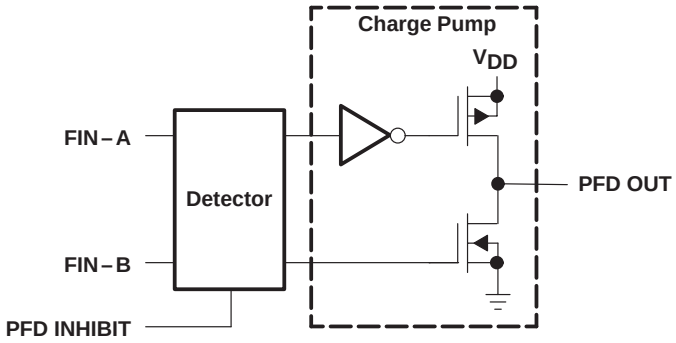
PFD INHIBIT	DETECTION	PFD OUTPUT	$I_{DD(PFD)}$
Low	Active	Active	Normal
High	Stopped	Hi-Z	Power Down

schematics

VCO block schematic



PFD block schematic



absolute maximum ratings†

Supply voltage (each supply), V_{DD} (see Note 1)	7 V
Input voltage range (each input), V_I (see Note 1)	–0.5 V to V_{DD} + 0.5 V
Input current (each input), I_I	±20 mA
Output current (each output), I_O	±20 mA
Continuous total power dissipation, at (or below) T_A = 25°C (see Note 2)	700 mW
Operating free-air temperature range, T_A	–20°C to 75°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 5.6 mW/°C.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (each supply, see Note 3)	V_{DD} = 3 V	2.85	3	3.15	V
	V_{DD} = 5 V	4.75	5	5.25	
Input voltage, V_I (inputs except VCO IN)		0		V_{DD}	V
Output current, I_O (each output)		0		±2	mA
VCO control voltage at VCO IN		0.9		V_{DD}	V
Lock frequency (×1 output)	V_{DD} = 3 V	14		21	MHz
	V_{DD} = 5 V	22		50	
Lock frequency (×1/2 output)	V_{DD} = 3 V	7		10.5	MHz
	V_{DD} = 5 V	11		25	
Bias resistor, R_{BIAS}	V_{DD} = 3 V	2.2	3.3	4.3	kΩ
	V_{DD} = 5 V	1.5	2.2	3.3	

NOTE 3: It is recommended that the logic supply terminal (LOGIC V_{DD}) and the VCO supply terminal (VCO V_{DD}) should be at the same voltage and separated from each other.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.3	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		0.9	1.5	2.1	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	µA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	µA
$I_{DD(VCO)}$	VCO supply current	See Note 5		5	15	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	2.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	µA
V_{IH}	High-level input voltage at FIN–A, FIN–B		2.7			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				0.5	V
V_{IT}	Input threshold voltage at PFD INHIBIT		0.9	1.5	2.1	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	µA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.1	1.5	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 3 V, rectangular wave), NC = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}	15	19	23	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		7	14	ns
		C_L = 50 pF, See Figure 3		14		
t_f	Fall time	C_L = 15 pF, See Figure 3		6	12	ns
		C_L = 50 pF, See Figure 3		10		
	Duty cycle at VCO OUT	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.04		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 3.3 kΩ, VCO IN = 1.5 V, V_{DD} = 2.85 V to 3.15 V		0.02		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 3.3 kΩ		100		ps

NOTES: 8. The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The low-pass-filter (LPF) circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		20			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	50	ns
t_{PHZ}	PFD output disable time from high level			23	50	
t_{PZL}	PFD output enable time to low level			11	30	ns
t_{PZH}	PFD output enable time to high level			10	30	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			2.1	10	ns

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA	4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
V_{IT}	Input threshold voltage at SELECT, VCO INHIBIT		1.5	2.5	3.5	V
I_I	Input current at SELECT, VCO INHIBIT	$V_I = V_{DD}$ or GND			±1	μA
$Z_{i(VCO\ IN)}$	Input impedance	VCO IN = 1/2 V_{DD}		10		MΩ
$I_{DD(INH)}$	VCO supply current (inhibit)	See Note 4		0.01	1	μA
$I_{DD(VCO)}$	VCO supply current	See Note 5		15	35	mA

NOTES: 4. Current into VCO V_{DD}, when VCO INHIBIT = V_{DD}, and PFD is inhibited.
5. Current into VCO V_{DD}, when VCO IN = 1/2 V_{DD}, R_{BIAS} = 3.3 kΩ, VCO INHIBIT = GND, and PFD is inhibited.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA	4.5			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.2	V
I_{OZ}	High-impedance-state output current	PFD INHIBIT = high, $V_I = V_{DD}$ or GND			±1	μA
V_{IH}	High-level input voltage at FIN–A, FIN–B		4.5			V
V_{IL}	Low-level input voltage at FIN–A, FIN–B				1	V
V_{IT}	Input threshold voltage at PFD INHIBIT		1.5	2.5	3.5	V
C_i	Input capacitance at FIN–A, FIN–B			5		pF
Z_i	Input impedance at FIN–A, FIN–B			10		MΩ
$I_{DD(Z)}$	High-impedance-state PFD supply current	See Note 6		0.01	1	μA
$I_{DD(PFD)}$	PFD supply current	See Note 7		0.15	3	mA

NOTES: 6. Current into LOGIC V_{DD}, when FIN–A, FIN–B = GND, PFD INHIBIT = V_{DD}, no load, and VCO OUT is inhibited.
7. Current into LOGIC V_{DD}, when FIN–A, FIN–B = 1 MHz ($V_{I(PP)}$ = 5 V, rectangular wave), PFD INHIBIT = GND, no load, and VCO OUT is inhibited.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

VCO section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Operating oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}	30	41	52	MHz
$t_{s(fosc)}$	Time to stable oscillation (see Note 8)	Measured from VCO INHIBIT↓			10	µs
t_r	Rise time	C_L = 15 pF, See Figure 3		5.5	10	ns
		C_L = 50 pF, See Figure 3		8		
t_f	Fall time	C_L = 15 pF, See Figure 3		5	10	ns
		C_L = 50 pF, See Figure 3		6		
	Duty cycle at VCO OUT	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD},	45%	50%	55%	
$\alpha_{(fosc)}$	Temperature coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 1/2 V_{DD}, T_A = –20°C to 75°C		0.06		%/°C
$k_{SVS(fosc)}$	Supply voltage coefficient of oscillation frequency	R_{BIAS} = 2.2 kΩ, VCO IN = 2.5 V, V_{DD} = 4.75 V to 5.25 V		0.006		%/mV
	Jitter absolute (see Note 9)	R_{BIAS} = 2.2 kΩ		100		ps

NOTES: 8: The time period to the stable VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. The LPF circuit is shown in Figure 28 with calculated values listed in Table 7. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed PCB with no device socket.

PFD section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency		40			MHz
t_{PLZ}	PFD output disable time from low level	See Figures 4 and 5 and Table 4		21	40	ns
t_{PHZ}	PFD output disable time from high level			20	40	
t_{PZL}	PFD output enable time to low level			7.3	20	ns
t_{PZH}	PFD output enable time to high level			6.5	20	
t_r	Rise time	C_L = 15 pF, See Figure 4		2.3	10	ns
t_f	Fall time			1.7	10	ns

PARAMETER MEASUREMENT INFORMATION

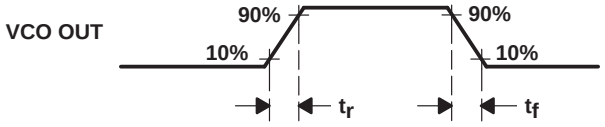
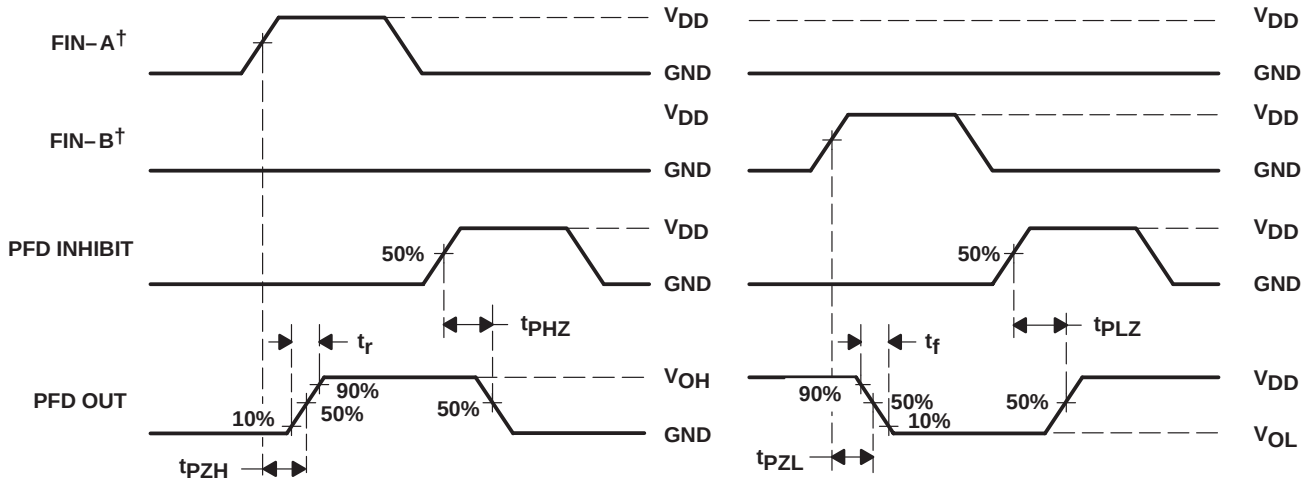


Figure 3. VCO Output Voltage Waveform



(a) OUTPUT PULLDOWN (see Figure 5 and Table 4)

(b) OUTPUT PULLUP (see Figure 5 and Table 4)

† FIN–A and FIN–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

Table 4. PFD Output Test Conditions

PARAMETER	R_L	C_L	S_1	S_2
t_{PZH}	1 kΩ	15 pF	Open	Close
t_{PHZ}				
t_r				
t_{PZL}			Close	Open
t_{PLZ}				
t_f				

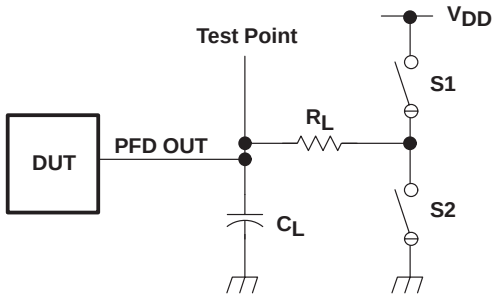


Figure 5. PFD Output Test Conditions

TYPICAL CHARACTERISTICS

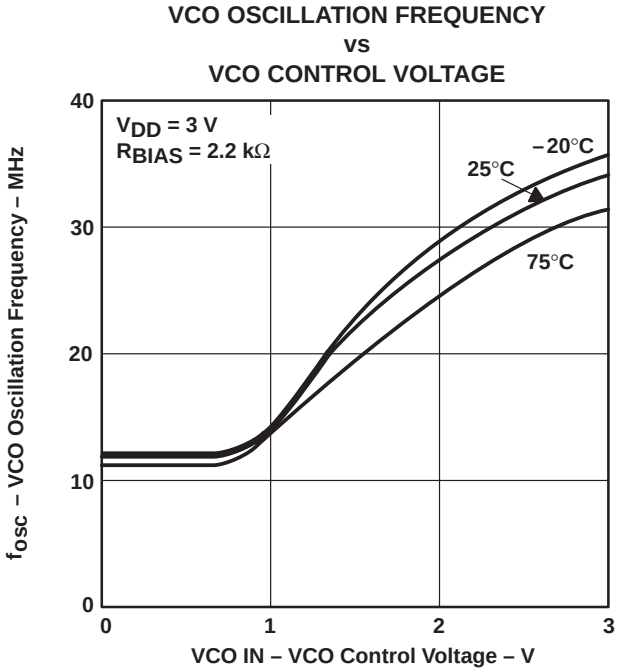


Figure 6

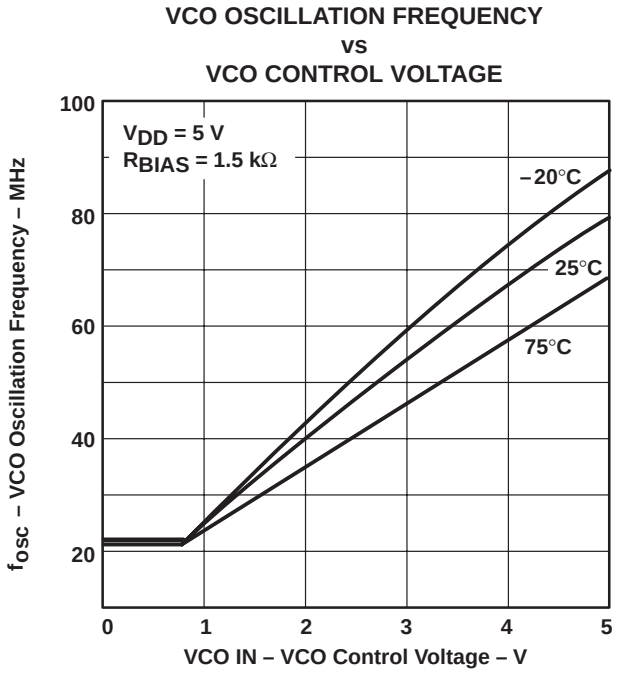


Figure 7

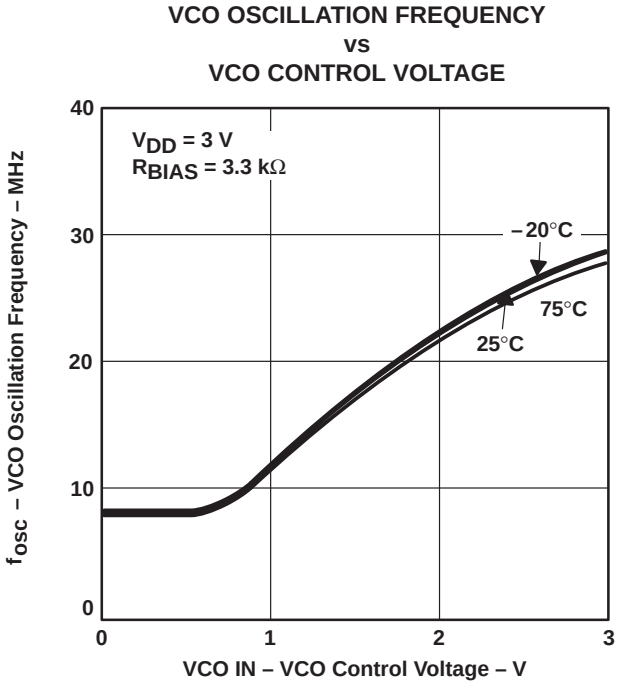


Figure 8

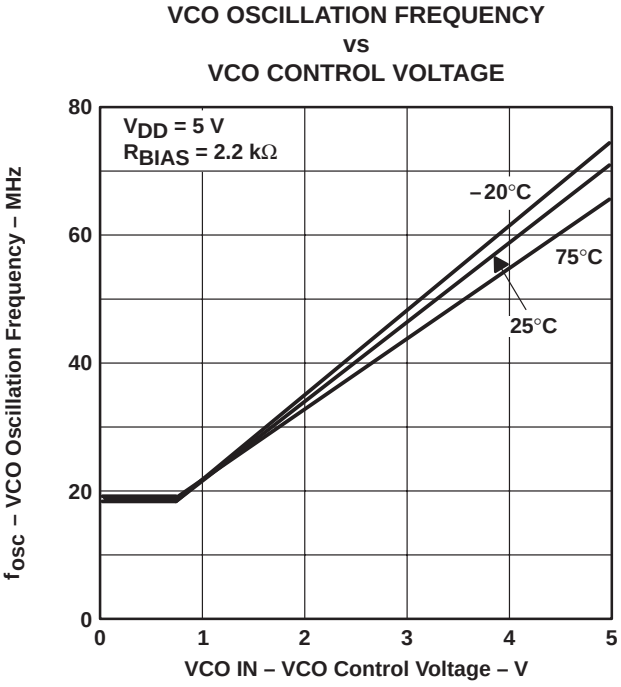


Figure 9

TYPICAL CHARACTERISTICS

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

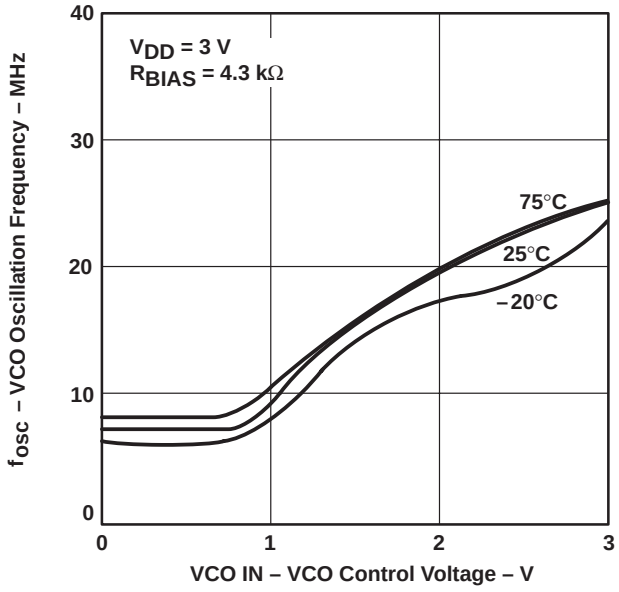


Figure 10

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

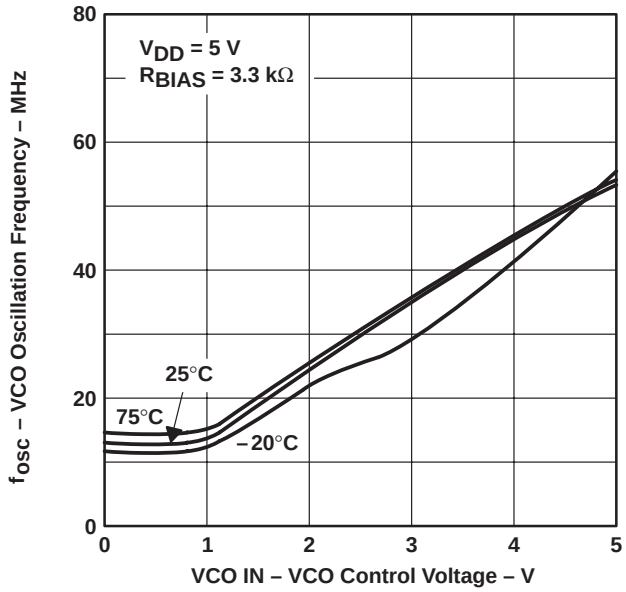


Figure 11

VCO OSCILLATION FREQUENCY
vs
BIAS RESISTOR

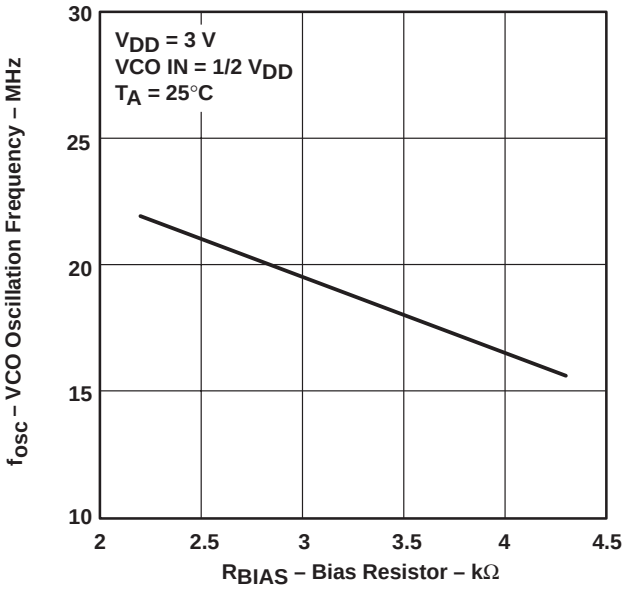


Figure 12

VCO OSCILLATION FREQUENCY
vs
BIAS RESISTOR

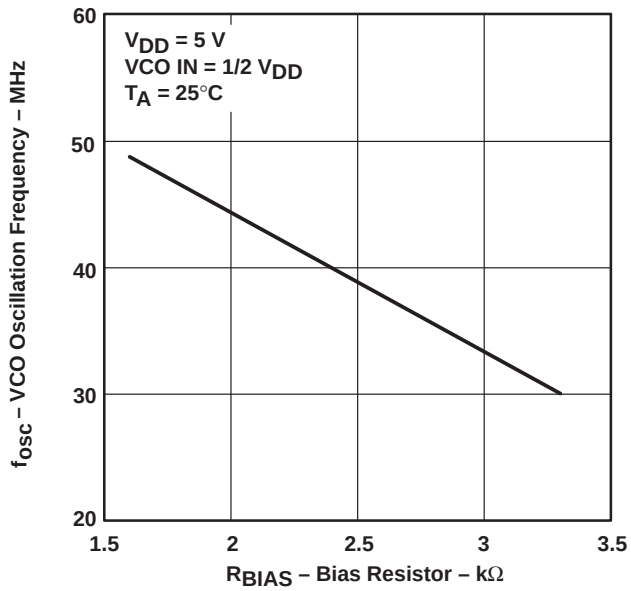


Figure 13

TYPICAL CHARACTERISTICS

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

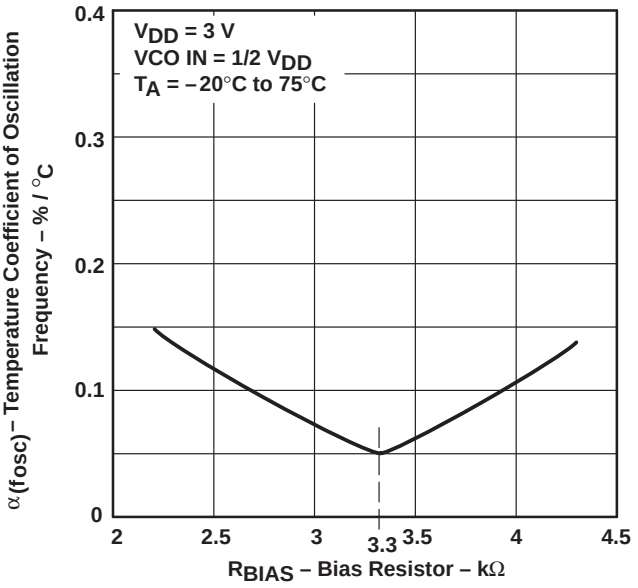


Figure 14

TEMPERATURE COEFFICIENT OF OSCILLATION FREQUENCY vs BIAS RESISTOR

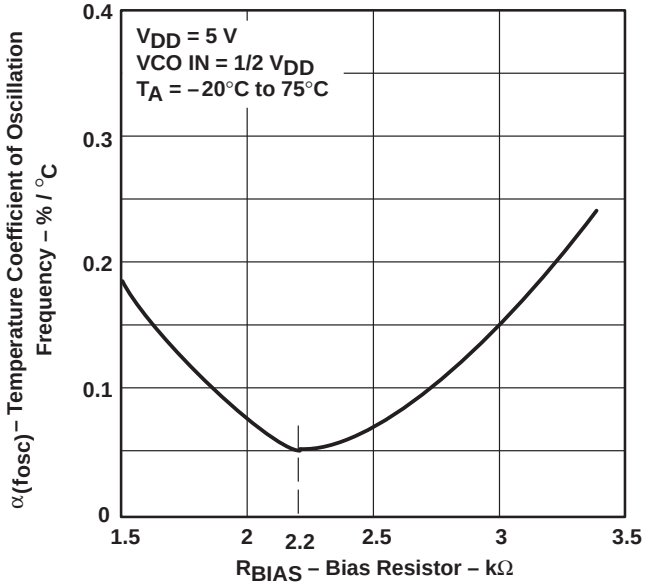


Figure 15

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

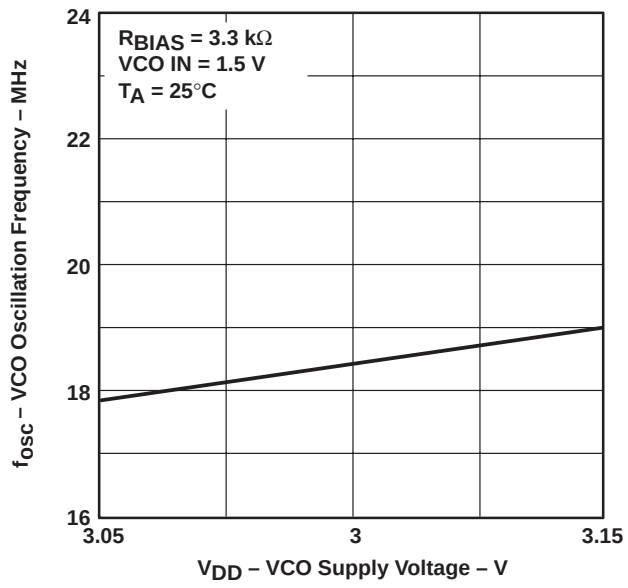


Figure 16

VCO OSCILLATION FREQUENCY vs VCO SUPPLY VOLTAGE

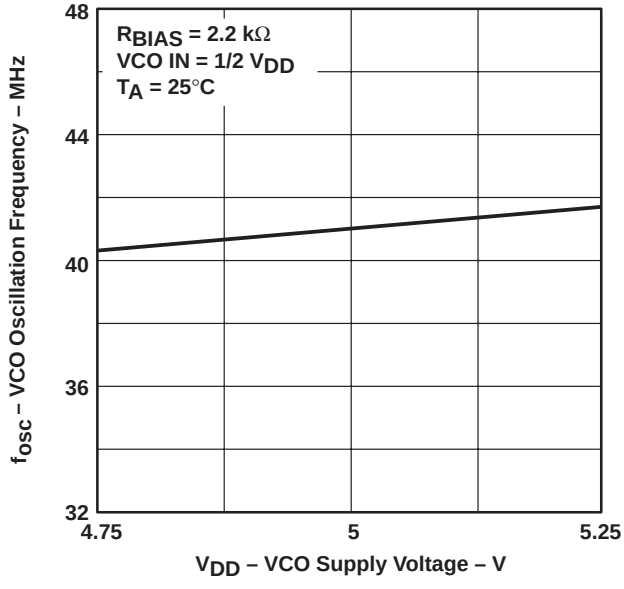


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

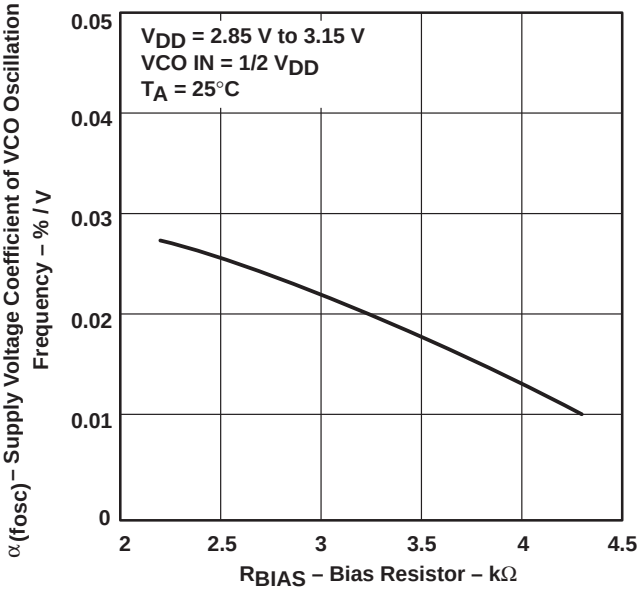


Figure 18

SUPPLY VOLTAGE COEFFICIENT OF VCO OSCILLATION FREQUENCY vs BIAS RESISTOR

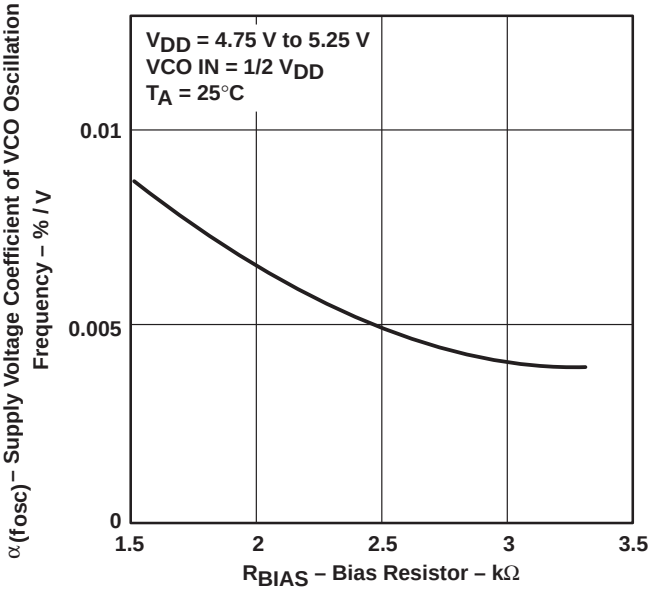


Figure 19

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

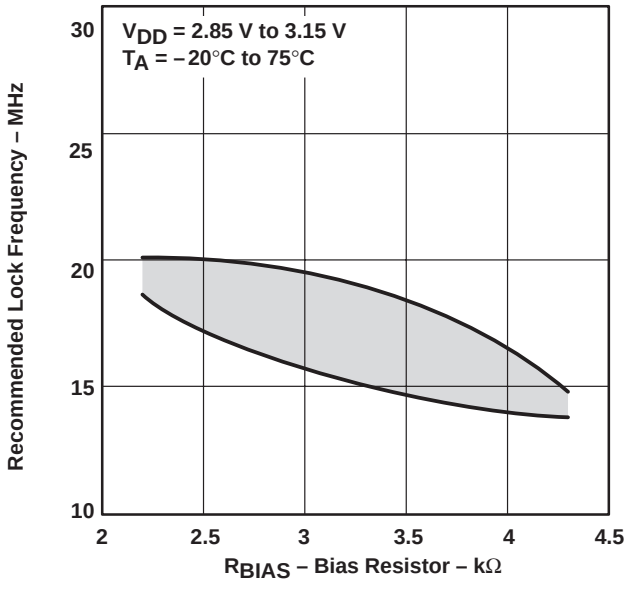


Figure 20

RECOMMENDED LOCK FREQUENCY (×1 OUTPUT) vs BIAS RESISTOR

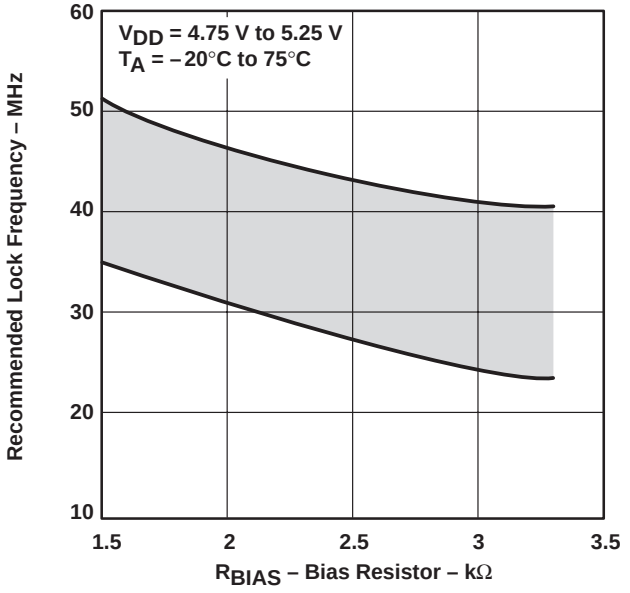


Figure 21

APPLICATION INFORMATION

**RECOMMENDED LOCK FREQUENCY
(×1/2 OUTPUT)
vs
BIAS RESISTOR**

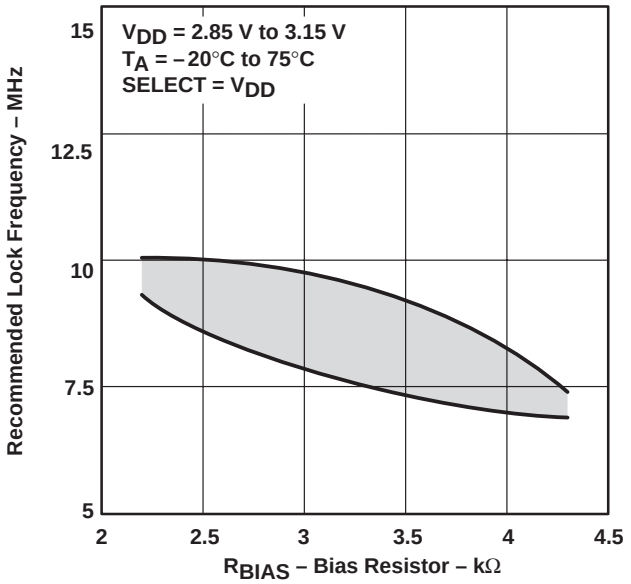


Figure 22

**RECOMMENDED LOCK FREQUENCY
(×1/2 OUTPUT)
vs
BIAS RESISTOR**

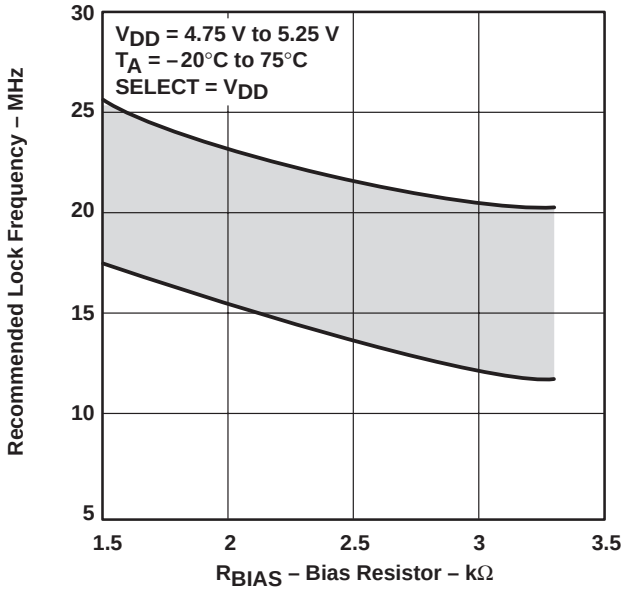


Figure 23

APPLICATION INFORMATION

gain of VCO and PFD

Figure 24 is a block diagram of the PLL. The countdown N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The K_p and K_V values are obtained from the operating characteristics of the device as shown in Figure 24. K_p is defined from the phase detector V_{OL} and V_{OH} specifications and the equation shown in Figure 24(b). K_V is defined from Figures 8, 9, 10, and 11 as shown in Figure 24(c).

The parameters for the block diagram with the units are as follows:

K_V : VCO gain (rad/s/V)
K_p : PFD gain (V/rad)
K_f : LPF gain (V/V)
K_N : count down divider gain (1/N)

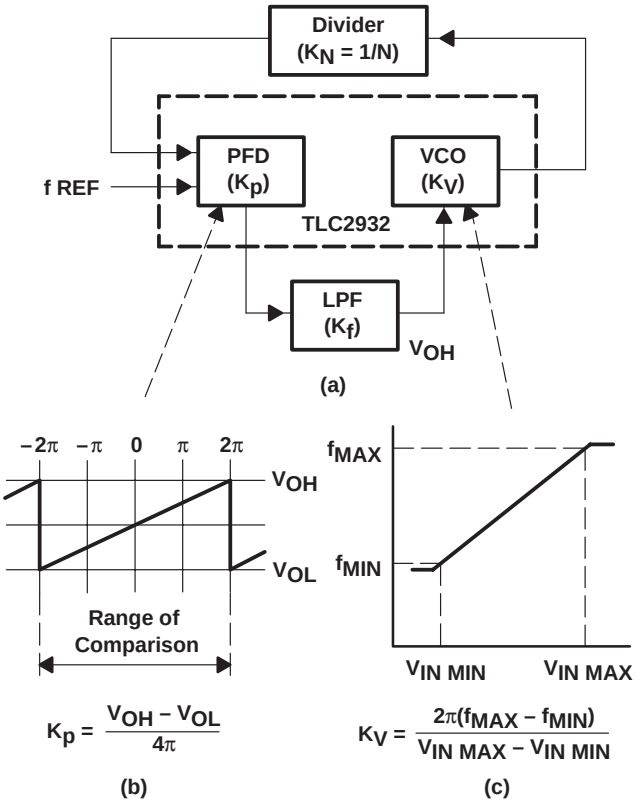


Figure 24. Example of a PLL Block Diagram

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

R_{BIAS}

The external bias resistor sets the VCO center frequency with 1/2 V_{DD} applied to the VCO IN terminal. However, for optimum temperature performance, a resistor value of 3.3 kΩ with a 3-V supply and a resistor value of 2.5 kΩ for a 5-V supply is recommended. For the most accurate results, a metal-film resistor is the better choice but a carbon-compositiion resistor can be used with excellent results also. A 0.22 μF capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 25 is as follows:

$$\Delta\omega_H \simeq 0.8 \left(K_p\right) \left(K_V\right) \left(K_f\,(\infty)\right)$$

Where

$K_f\,(\infty)$ = the filter transfer function value at $\omega = \infty$

APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 25. When the active filter of Figure 25(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

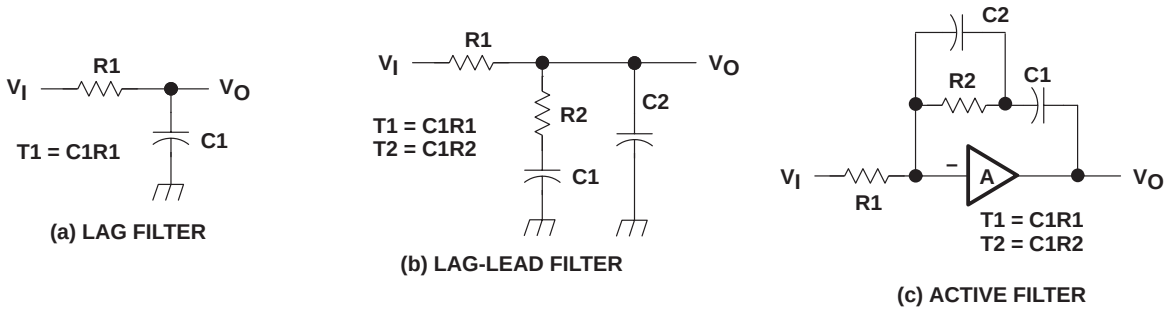


Figure 25. LPF Examples for PLL

the passive filter

The transfer function for the lag-lead filter shown in Figure 25(b) is;

$$\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T2}{1 + s \cdot (T1 + T2)}$$

Where

$$T1 = R1 \cdot C1 \text{ and } T2 = R2 \cdot C1$$

Using this filter makes the closed loop PLL system a second-order type 1 system. The response curves of this system to a unit step are shown in Figure 26.

the active filter

When using the active integrator shown in Figure 25(c), the phase detector inputs must be reversed since the integrator adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 25(c) is:

$$F(s) = \frac{1 + s \cdot R2 \cdot C1}{s \cdot R1 \cdot C1}$$

Using this filter makes the closed loop PLL system a second-order type 2 system. The response curves of this system to a unit step are shown in Figure 27.

basic design example

The following design example presupposes that the input reference frequency and the required frequency of the VCO are within the respective ranges of the device.

APPLICATION INFORMATION

basic design example (continued)

Assume the loop has to have a 100 μs settling time (t_s) with a countdown N = 8. Using the Type 1, second order response curves of Figure 26, a value of 4.5 radians is selected for $\omega_n t_s$ with a damping factor of 0.7. This selection gives a good combination for settling time, accuracy, and loop gain margin. The initial parameters are summarized in Table 5. The loop constants, K_V and K_p, are calculated from the data sheet specifications and Table 6 shows these values.

The natural loop frequency is calculated as follows:

Since

$$\omega_n t_s = 4.5$$

Then

$$\omega_n = \frac{4.5}{100\ \mu s} = 45\ \text{k-radians/sec}$$

Table 5. Design Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Division factor	N	8	
Lockup time	t	100	μs
Radian value to selected lockup time	$\omega_n t$	4.5	rad
Damping factor	ζ	0.7	

Table 6. Device Specifications

PARAMETER	SYMBOL	VALUE	UNITS
VCO gain	K_V	76.6	Mrad/V/s
f_{MAX}		70	MHz
f_{MIN}		20	MHz
$V_{IN\ MAX}$		5	V
$V_{IN\ MIN}$		0.9	V
PFD gain	K_p	0.342357	V/rad

Table 7. Calculated Values

PARAMETER	SYMBOL	VALUE	UNITS
Natural angular frequency	ω_n	45000	rad/sec
$K = (K_V \bullet K_p)/N$		3.277	Mrad/sec
Lag-lead filter Calculated value Nearest standard value	R1	15870 16000	Ω
Calculated value Nearest standard value	R2	308 300	Ω
Selected value	C1	0.1	μF

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Using the low-pass filter in Figure 25(b) and divider ratio N, the transfer function for phase and frequency are shown in equations 1 and 2. Note that the transfer function for phase differs from the transfer function for frequency by only the divider value N. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, transfer function of Figure 24 (a) for phase is

$$\frac{\Phi 2(s)}{\Phi 1(s)} = \frac{K_p \cdot K_V}{N \cdot (T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (1)$$

and the transfer function for frequency is

$$\frac{F_{OUT}(s)}{F_{REF}(s)} = \frac{K_p \cdot K_V}{(T1 + T2)} \left[\frac{1 + s \cdot T2}{s^2 + s \cdot \left[1 + \frac{K_p \cdot K_V \cdot T2}{N \cdot (T1 + T2)} \right] + \frac{K_p \cdot K_V}{N \cdot (T1 + T2)}} \right] \quad (2)$$

The standard two-pole denominator is $D = s^2 + 2\,\zeta\,\omega_n\,s + \omega_n^2$ and comparing the coefficients of the denominator of equation 1 and 2 with the standard two-pole denominator gives the following results.

$$\omega_n = \sqrt{\frac{K_p \cdot K_V}{N \cdot (T1 + T2)}}$$

Solving for T1 + T2

$$T1 + T2 = \frac{K_p \cdot K_V}{N \cdot \omega_n^2} \quad (3)$$

and by using this value for T1 + T2 in equation 3 the damping factor is

$$\zeta = \frac{\omega_n}{2} \cdot \left(T2 + \frac{N}{K_p \cdot K_V} \right)$$

solving for T2

$$T2 = \frac{2\,\zeta}{\omega} - \frac{N}{K_p \cdot K_V}$$

then by substituting for T2 in equation 3

$$T1 = \frac{K_V \cdot K_p}{N \cdot \omega_n^2} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}$$

APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

$$R2 = \left[\frac{2\,\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1}$$

$$R1 = \left[\frac{K_p \cdot K_v}{\omega_n{}^2 \cdot N} - \frac{2\,\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V}\right]\frac{1}{C1}$$

The capacitor, C1, is usually chosen between 1 μF and 0.1 μF to allow for reasonable resistor values and physical capacitor size. In this example, C1 is chosen to be 0.1 μF and the corresponding R1 and R2 calculated values are listed in Table 7.

APPLICATION INFORMATION

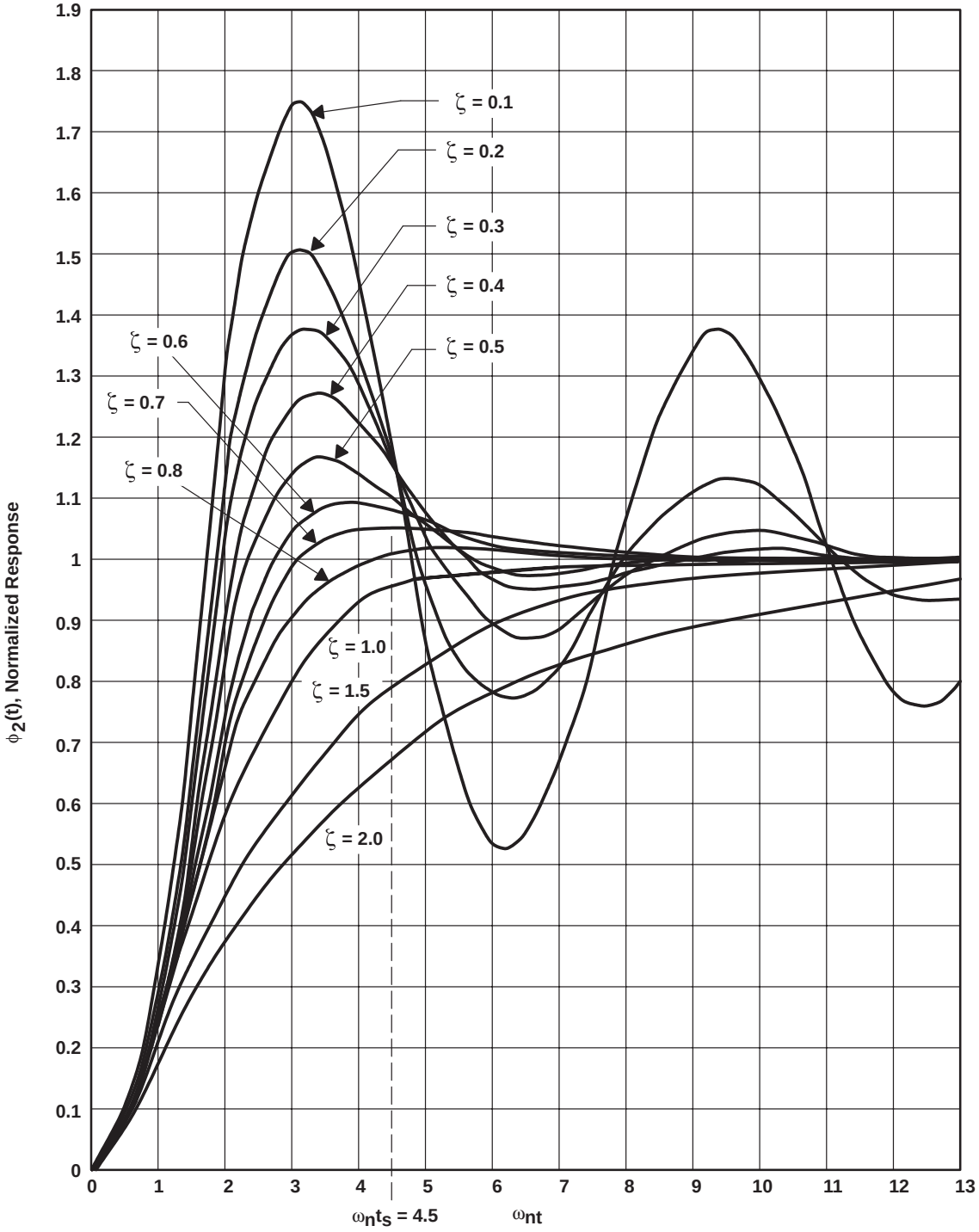


Figure 26. Type 1 Second-Order Step Response

APPLICATION INFORMATION

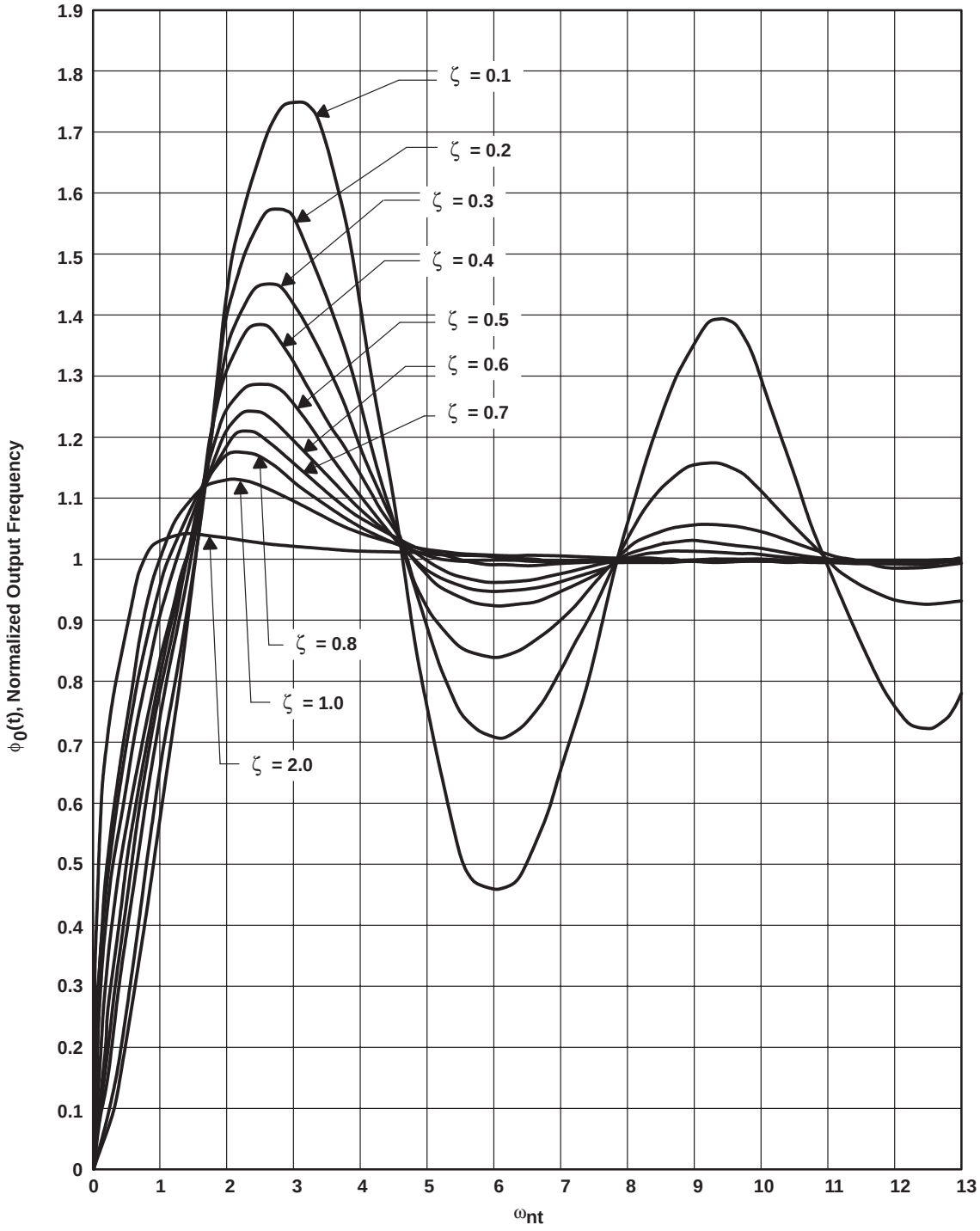


Figure 27. Type 2 Second-Order Step Response

APPLICATION INFORMATION

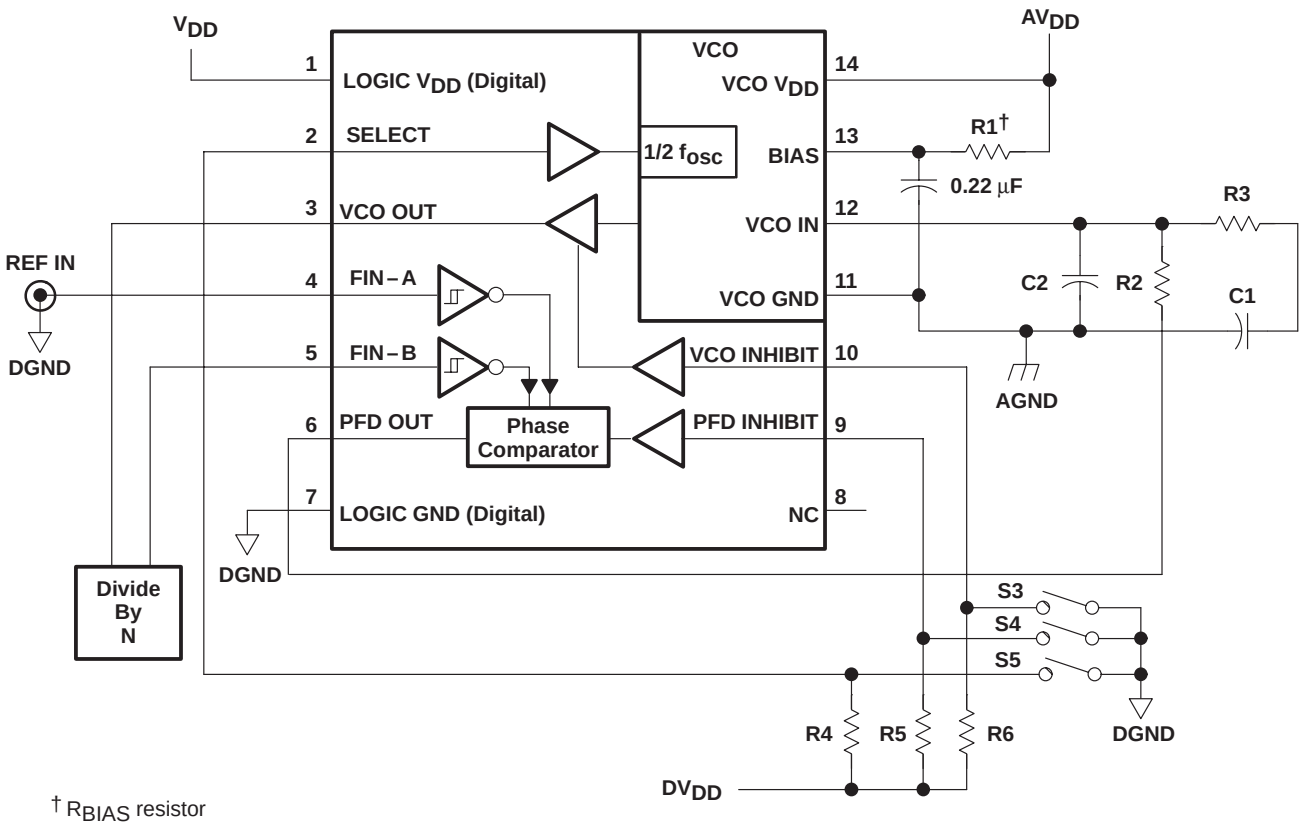


Figure 28. Evaluation and Operation Schematic

PCB layout considerations

The TLC2932 contains a high frequency analog oscillator; therefore, very careful breadboarding and printed-circuit-board (PCB) layout is required for evaluation.

The following design recommendations benefit the TLC2932 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- RF breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_{DD} and VCO V_{DD} should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_{DD} to GND and LOGIC V_{DD} to GND should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to GND.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2932IPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-	Y2932
TLC2932IPWR	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-	Y2932

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

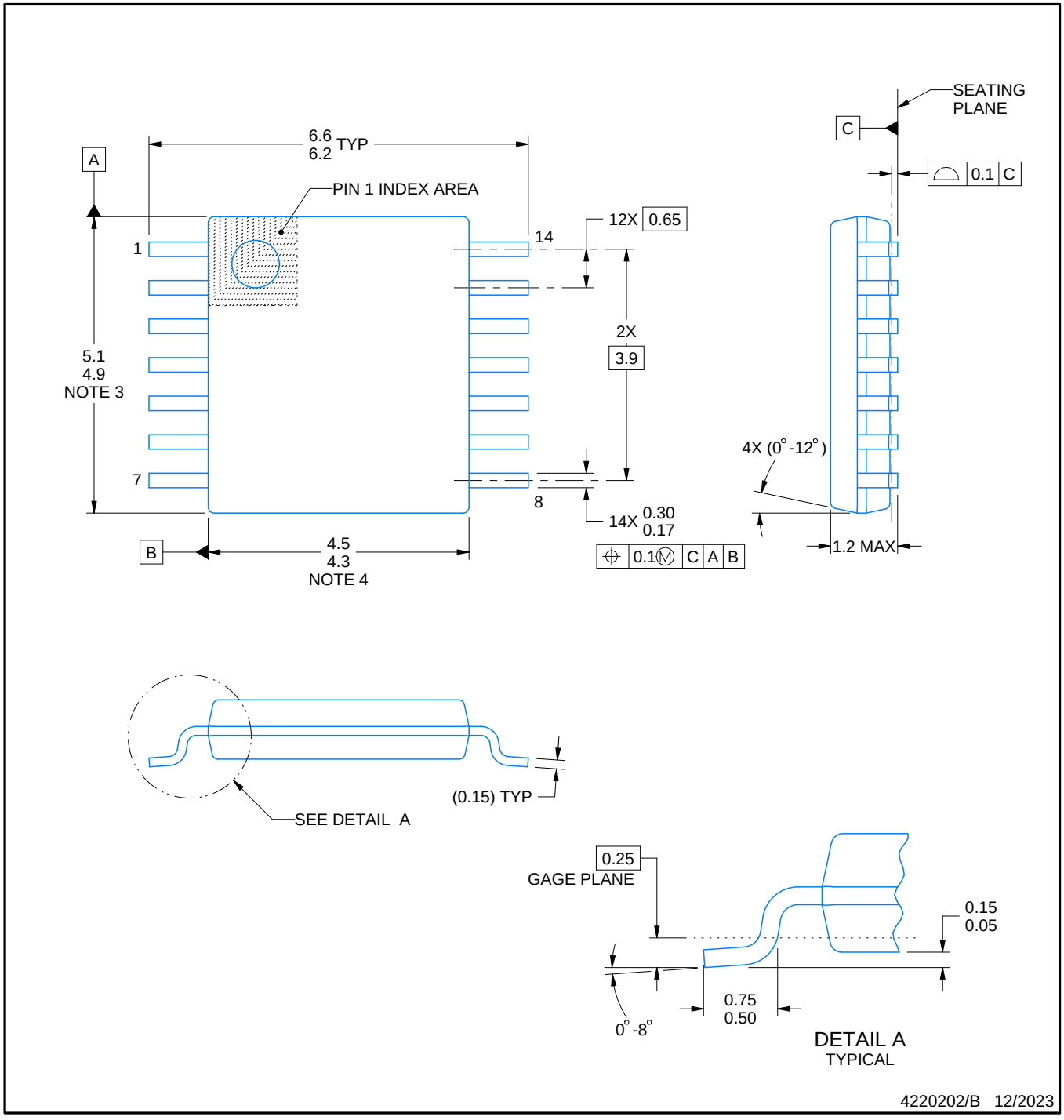
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

PW0014A

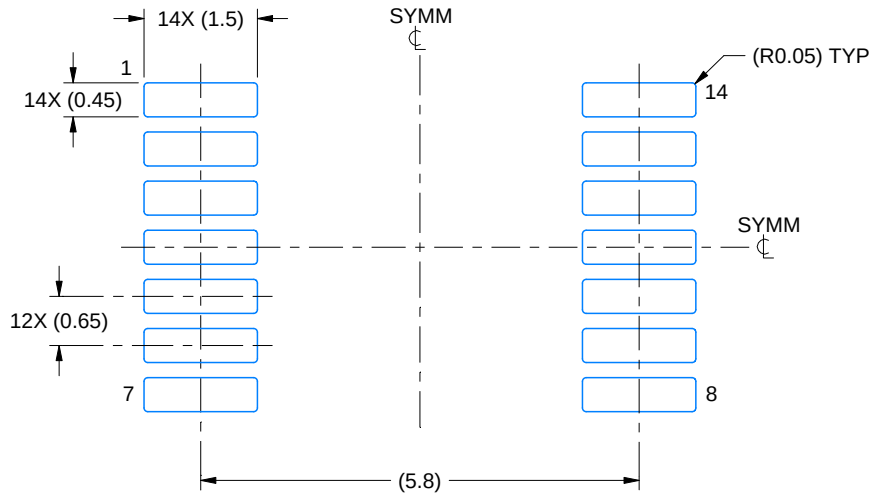
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

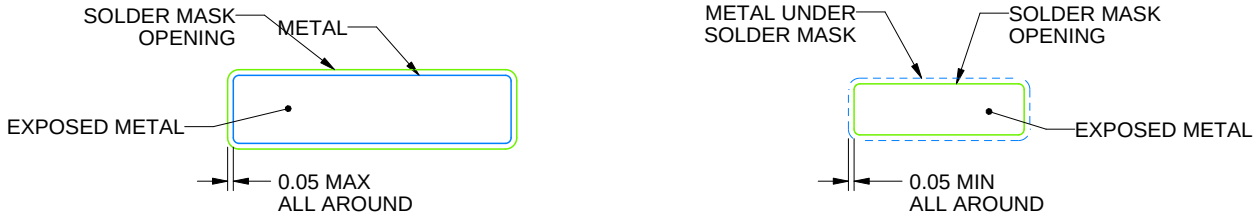


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

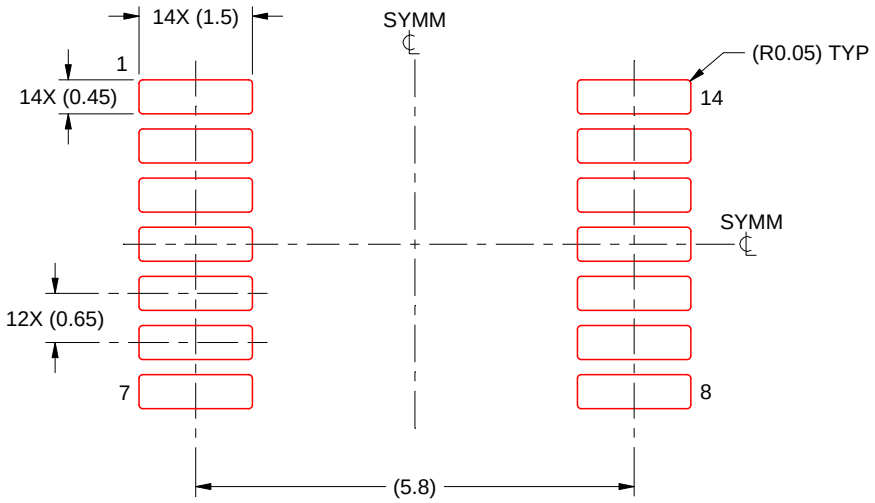


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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