TEXAS INSTRUMENTS
TLV9051-Q1, TLV9052-Q1
SBOSAH8 – FEBRUARY 2024

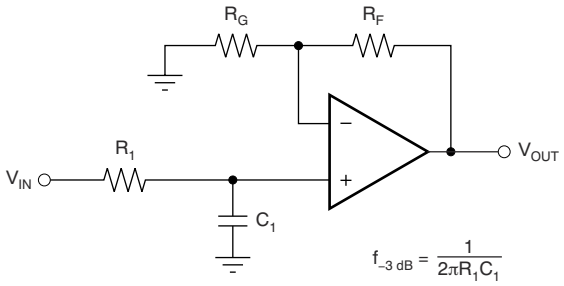
TLV905x-Q1 Automotive 5MHz, 15V/µs High Slew-Rate, RRIO, CMOS Op Amp

1 Features

- High slew rate: 15V/µs
- Low quiescent current: 330µA
- Rail-to-rail input and output
- Low input offset voltage: ±0.33mV
- Unity-gain bandwidth: 5MHz
- Low broadband noise: 15nV/√Hz
- Low input bias current: 2pA
- Unity-gain stable
- Internal RFI and EMI filter
- Scalable family of CMOS op amps for low-cost applications
- Operational at supply voltages as low as 1.8V
- Extended temperature range: –40°C to 125°C

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- HEV/EV traction inverter and motor control
- HEV/EV DC/DC converter
- HEV/EV battery-management system (BMS)
- On-board (OBC) and wireless charger
- Automotive body motors
- Automotive heating and cooling



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

3 Description

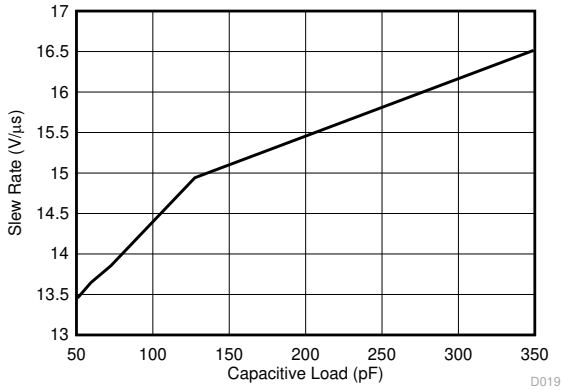
The TLV9051-Q1, TLV9052-Q1, and TLV9054-Q1 devices are single, dual, and quad operational amplifiers, respectively. The devices are designed for low voltage operation from 1.8V to 6.0V. The inputs and outputs can operate from rail to rail at a very high slew rate. These devices are an excellent choice for cost-constrained applications where low-voltage operation, high slew rate, and low quiescent current is needed. The capacitive-load drive of the TLV905x-Q1 family is 150pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads.

The TLV905x-Q1 family is easy to use due to the devices being unity-gain stable, including a RFI and EMI filter, and being free from phase reversal in an overdrive condition.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE	PACKAGE SIZE(3)
TLV9051-Q1	Single	DBV (SOT-23, 5)(2)	2.90mm × 2.80mm
		DCK (SC70, 5)(2)	2.00mm × 2.10mm
TLV9052-Q1	Dual	D (SOIC, 8)(2)	4.90mm × 6.00mm
		PW (TSSOP, 8)(2)	3.00mm × 6.40mm
		DGK (VSSOP, 8)(2)	3.00mm × 4.90mm
TLV9054-Q1	Quad	D (SOIC, 14)(2)	8.65mm × 6.00mm
		PW (TSSOP, 14)(2)	5.00mm × 6.40mm

(1) For more information, see Section 10
(2) This package is for preview only.
(3) The package size (length x width) is a nominal value and includes pins, where applicable.



Slew Rate vs Load Capacitance

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4 Pin Configuration and Functions

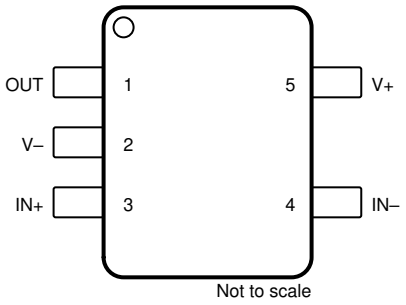

Figure 4-1. TLV9051-Q1 DBV Package, 5-Pin SOT-23 (Top View)

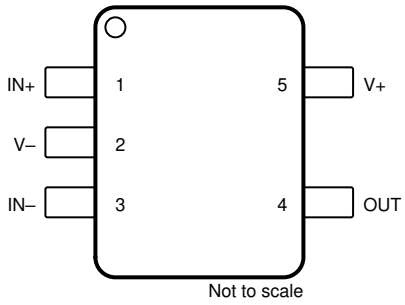

Figure 4-2. TLV9051-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 4-1. Pin Functions: TLV9051-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC-70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	—	Positive (high) supply

(1) I = input, O = output

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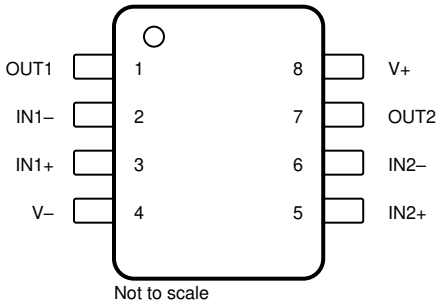

Figure 4-3. TLV9052-Q1 D, DGK, PW Packages, 8-Pin SOIC, VSSOP, TSSOP (Top View)

Table 4-2. Pin Functions: TLV9052-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply

(1) I = input, O = output

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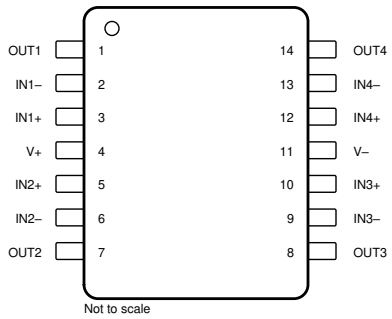

Figure 4-4. TLV9054-Q1 D, PW Packages, 14-Pin SOIC, TSSOP (Top View)

Table 4-3. Pin Functions: TLV9054-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (low) supply or ground (for single-supply operation)
V+	4	—	Positive (high) supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage				7	V
Signal input pins	Voltage[2]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current[2]		–10	10	mA
Output short-circuit[3]			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$ - Other Packages	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	6	V
V_I	Common mode voltage range	(V–) – 0.1	(V+) + 0.1	V
T_A	Specified temperature	–40	125	°C

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5.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV9051-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV9052-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC[1]		TLV9054-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V

at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5V		±0.33	±1.6	mV
		V_S = 5V, T_A = –40°C to +125°C			±2	
dV_{OS}/dT	Drift	V_S = 5V, T_A = –40°C to +125°C		±0.5		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V – 5.5V, V_{CM} = (V–)		±13	±80	µV/V
	Channel separation, dc	At dc		115		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	V_S = 1.8V to 5.5V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, (V–) – 0.1V < V_{CM} < (V+) – 1.4V, T_A = –40°C to +125°C	80	96		dB
		V_S = 5.5V, V_{CM} = –0.1V to 5.6V, T_A = –40°C to +125°C	62	79		
		V_S = 1.8V, (V–) – 0.1V < V_{CM} < (V+) – 1.4V, T_A = –40°C to +125°C		88		
		V_S = 1.8V, V_{CM} = –0.1V to 1.9V, T_A = –40°C to +125°C		72		
INPUT BIAS CURRENT						
I_B	Input bias current			±2	±18[2]	pA
		T_A = –40°C to +125°C			±525[2]	pA
I_{OS}	Input offset current			±1	±15[2]	pA
		T_A = –40°C to +125°C			±440[2]	pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5V, f = 0.1Hz to 10Hz		6		$µV_{PP}$
e_n	Input voltage noise density	V_S = 5V, f = 10kHz		15		nV/√Hz
		V_S = 5V, f = 1kHz		20		nV/√Hz
i_n	Input current noise density	f = 1kHz		18		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8V, (V–) + 0.04V < V_O < (V+) – 0.04V, R_L = 10kΩ		106		dB
		V_S = 5.5V, (V–) + 0.05V < V_O < (V+) – 0.05V, R_L = 10kΩ	104	128		
		V_S = 1.8V, (V–) + 0.06V < V_O < (V+) – 0.06V, R_L = 2kΩ		108		
		V_S = 5.5V, (V–) + 0.15V < V_O < (V+) – 0.15V, R_L = 2kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5.5V, G = +1		5		MHz
$φ_m$	Phase margin	V_S = 5.5V, G = +1		60		Degrees
SR	Slew rate	V_S = 5.5V, G = +1, C_L = 130pF		15		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5V, 2-V step , G = +1, C_L = 100pF		0.75		µs
		To 0.01%, V_S = 5.5V, 2-V step , G = +1, C_L = 100pF		1		
t_{OR}	Overload recovery time	V_S = 5.5V, V_{IN} × gain > V_S		0.3		µs
THD + N	Total harmonic distortion + noise[1]	V_S = 5.5V, V_{CM} = 2.5V, V_O = 1V_{RMS}, G = +1, f = 1kHz		0.0006%		

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5.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8V to 5.5V (continued)

at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted);

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5V, R_L = 10kΩ,			16	mV
		V_S = 5.5V, R_L = 2kΩ,			40	
I_{SC}	Short-circuit current	V_S = 5V		±50		mA
Z_O	Open-loop output impedance	V_S = 5V, f = 5MHz		250		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5V, I_O = 0mA,		330	450	µA
		V_S = 5.5V, I_O = 0mA, T_A = –40°C to +125°C			475	

(1) Third-order filter; bandwidth = 80kHz at –3dB.
(2) Specified by design and characterization; not production tested.

5.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

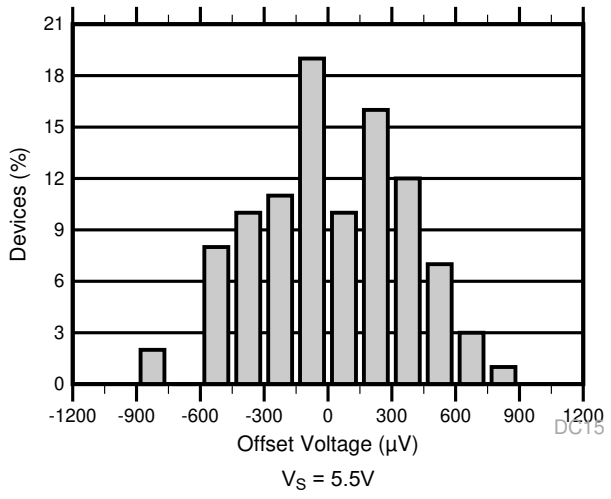

Figure 5-1. Offset Voltage Production Distribution

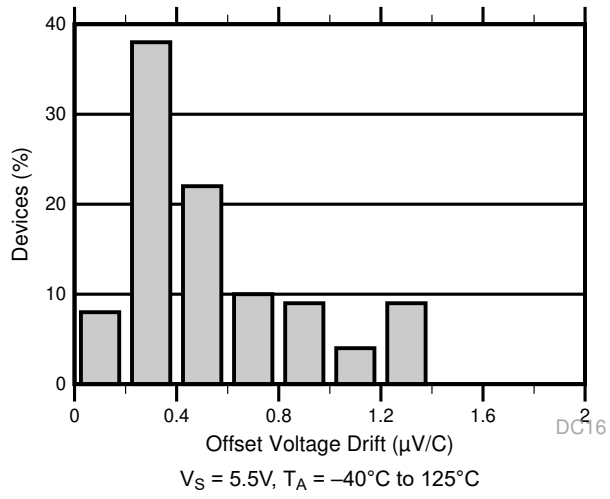

Figure 5-2. Offset Voltage Drift Distribution

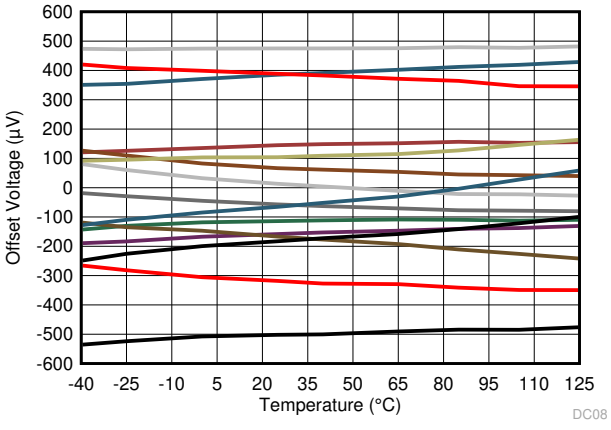

Figure 5-3. Offset Voltage vs Temperature

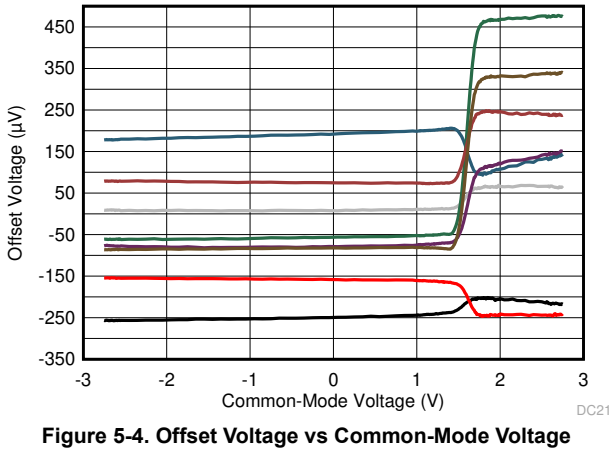

Figure 5-4. Offset Voltage vs Common-Mode Voltage

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

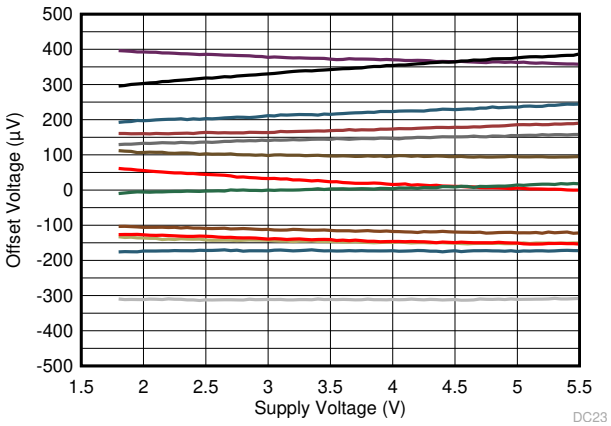

Figure 5-5. Offset Voltage vs Power Supply

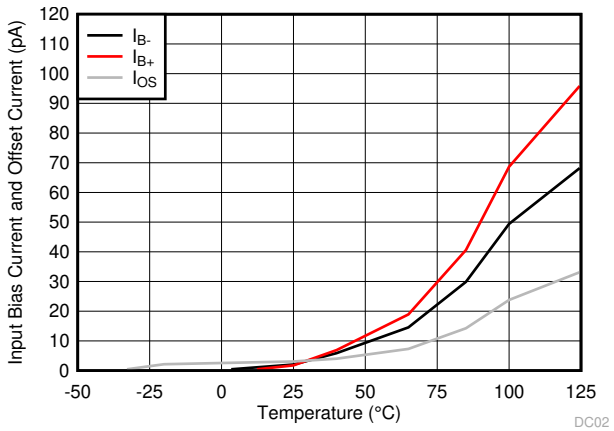

Figure 5-6. Input Bias Current vs Temperature

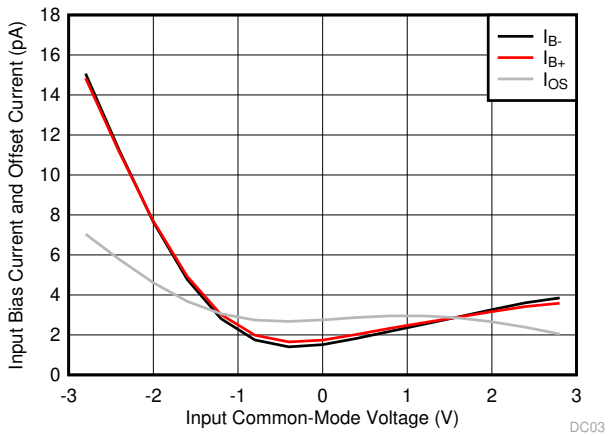

Figure 5-7. Input Bias Current and Offset Current vs Common-Mode Voltage

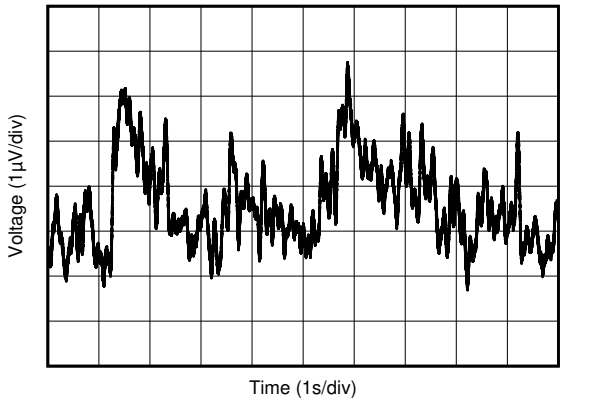

Figure 5-8. 0.1-Hz to 10-Hz Input Voltage Noise

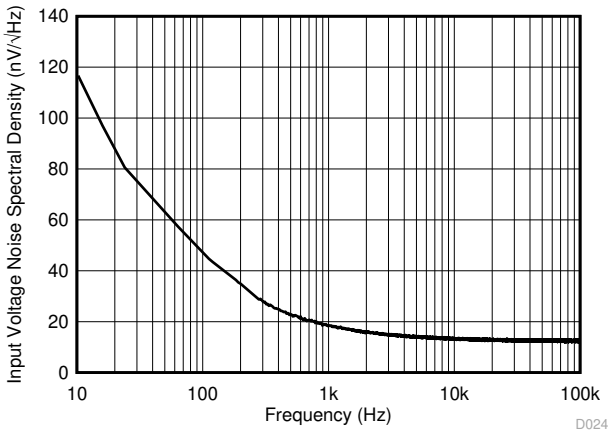

Figure 5-9. Input Voltage Noise Spectral Density vs Frequency

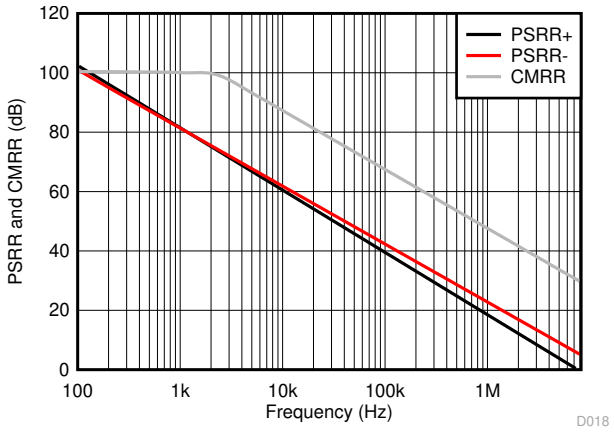

Figure 5-10. CMRR and PSRR vs Frequency (Referred to Input)

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

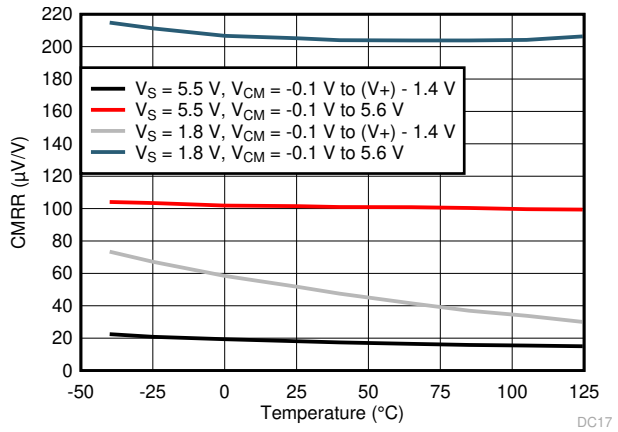
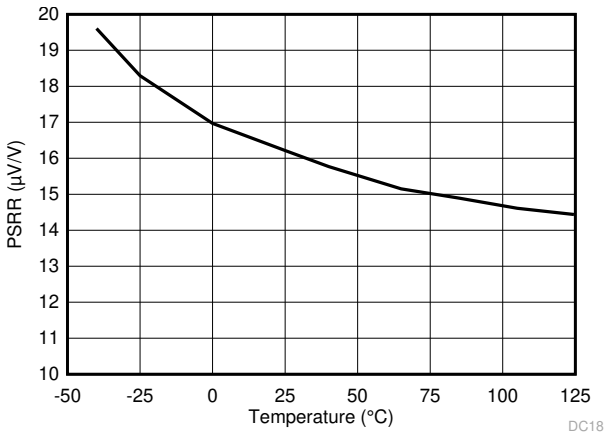


Figure 5-11. CMRR vs Temperature



V_S = 1.8V to 5.5V

Figure 5-12. PSRR vs Temperature

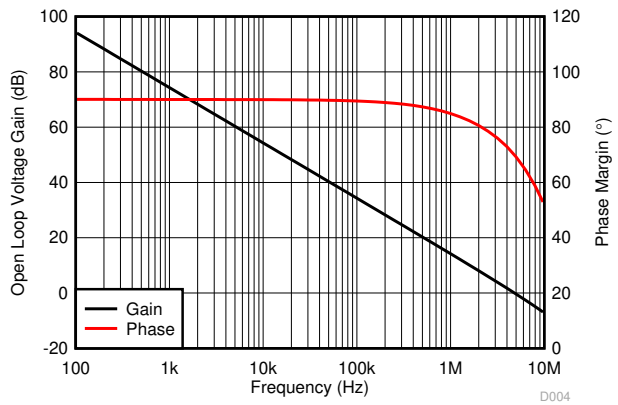


Figure 5-13. Open Loop Voltage Gain and Phase vs Frequency

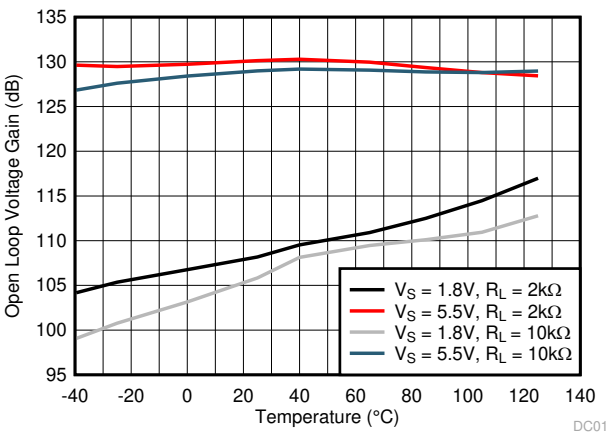


Figure 5-14. Open Loop Voltage Gain vs Temperature

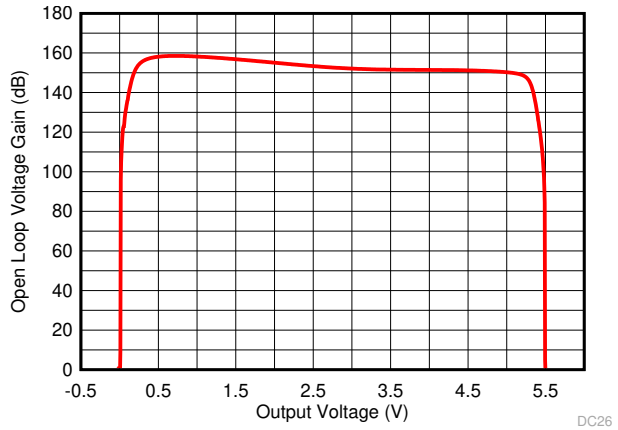


Figure 5-15. Open Loop Voltage Gain vs Output Voltage

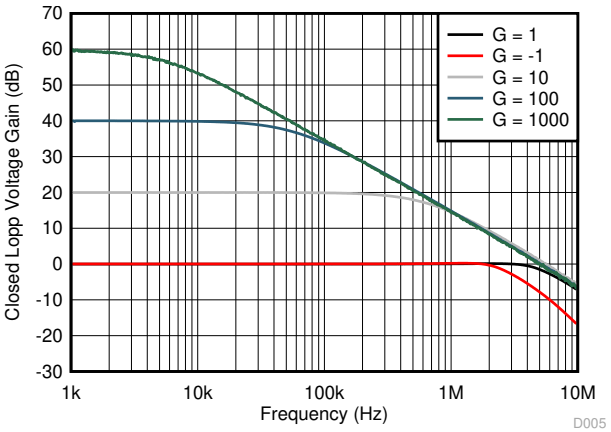


Figure 5-16. Closed Loop Voltage Gain vs Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

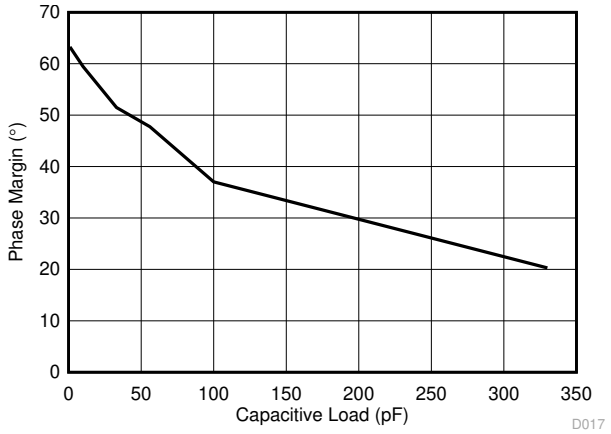


Figure 5-17. Phase Margin vs Capacitive Load

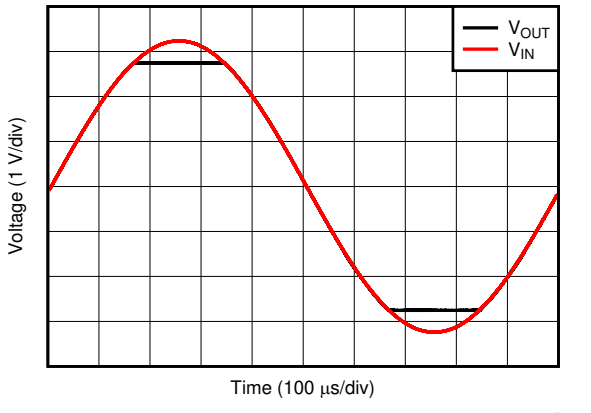
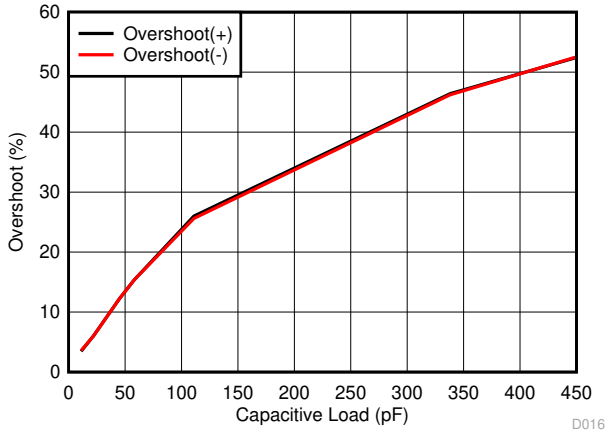


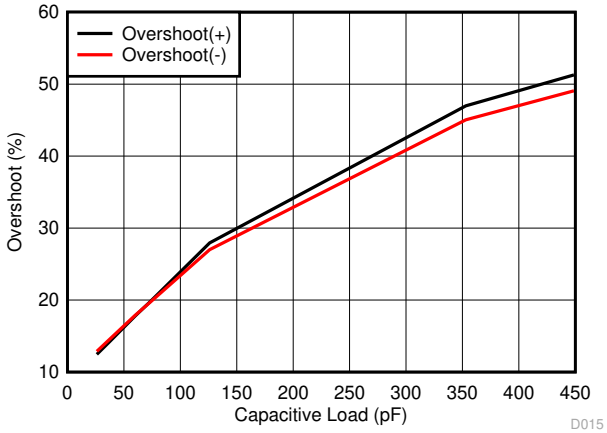
Figure 5-18. No Phase Reversal



G = +1V/V

V_{OUT} step = 100 mV_{p-p}

Figure 5-19. Small-Signal Overshoot vs Load Capacitance



G = –1V/V

V_{OUT} step = 100 mV_{p-p}

Figure 5-20. Small-Signal Overshoot vs Load Capacitance

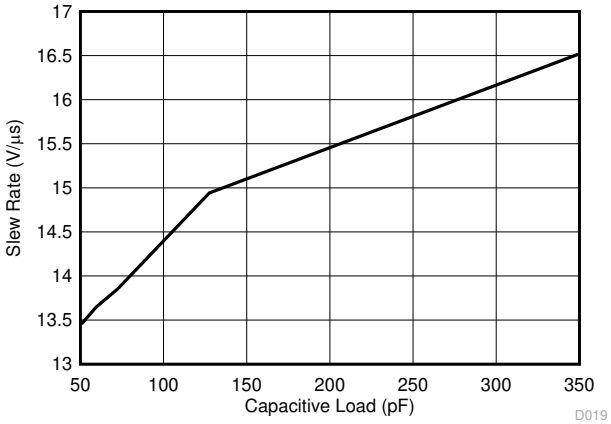
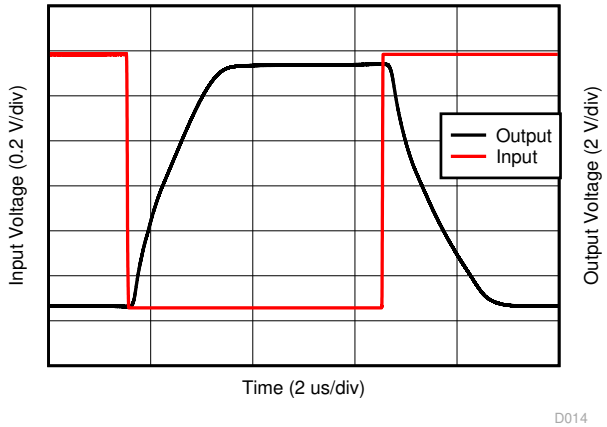


Figure 5-21. Slew Rate vs Capacitive Load



G = –10V/V

Figure 5-22. Overload Recovery

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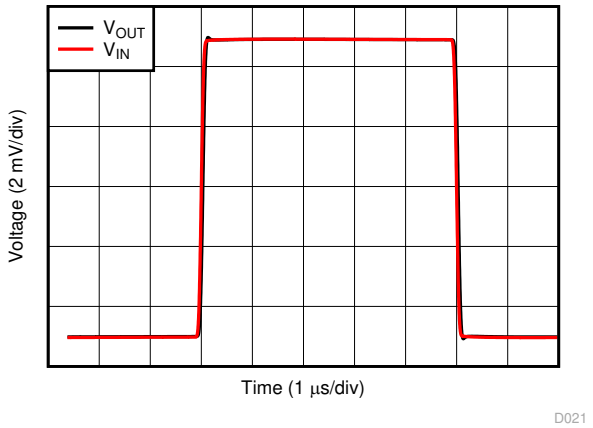
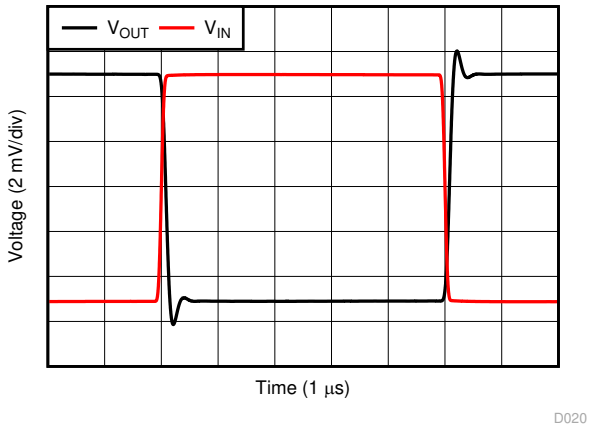
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



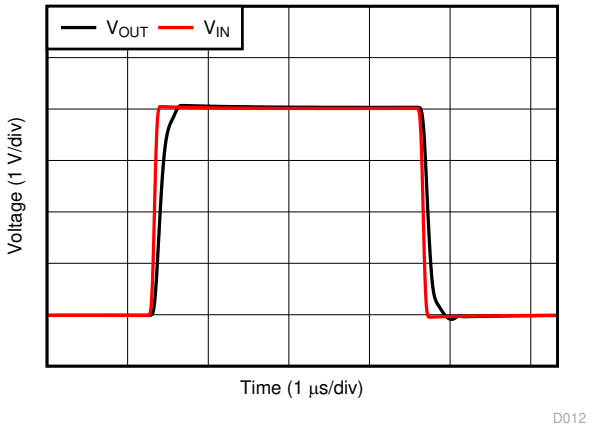
G = +1V/V
V_{OUT} step = 10 mV_{p-p}

Figure 5-23. Small-Signal Step Response



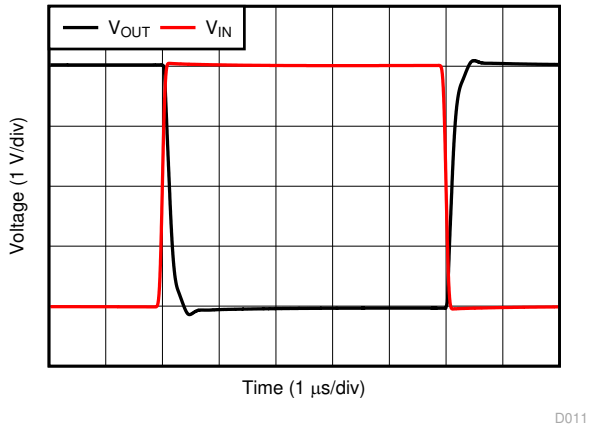
G = –1V/V
V_{OUT} step = 10 mV_{p-p}

Figure 5-24. Small-Signal Step Response



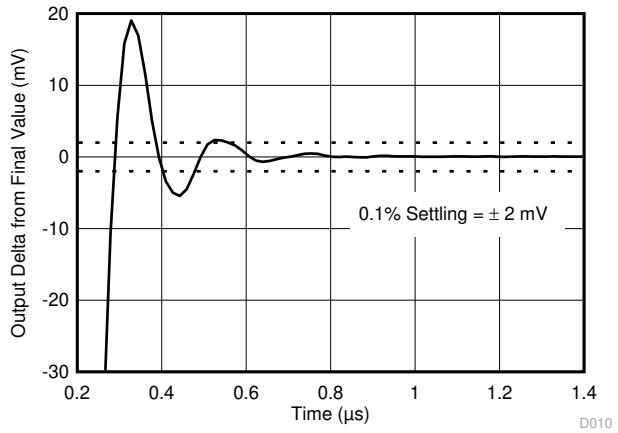
G = +1V/V
V_{OUT} step = $4V_{p-p}$

Figure 5-25. Large-Signal Step Response



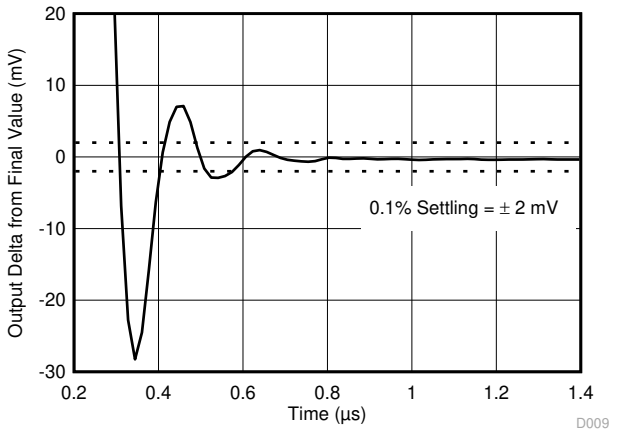
G = –1V/V
V_{OUT} step = $4V_{p-p}$

Figure 5-26. Large-Signal Step Response



C_L = 100pF G = +1V/V

Figure 5-27. Positive Large-Signal Settling Time



C_L = 100pF G = +1V/V

Figure 5-28. Negative Large-Signal Settling Time

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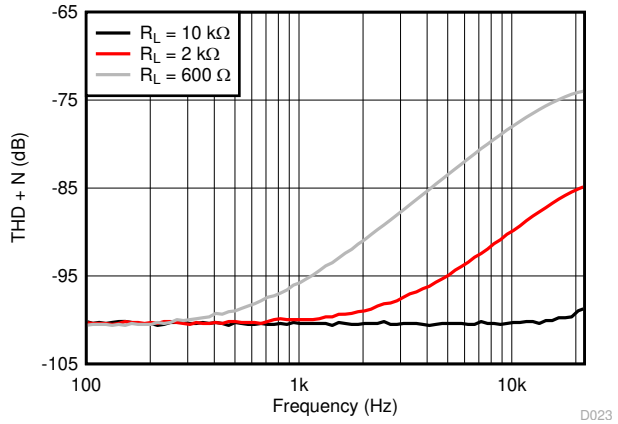
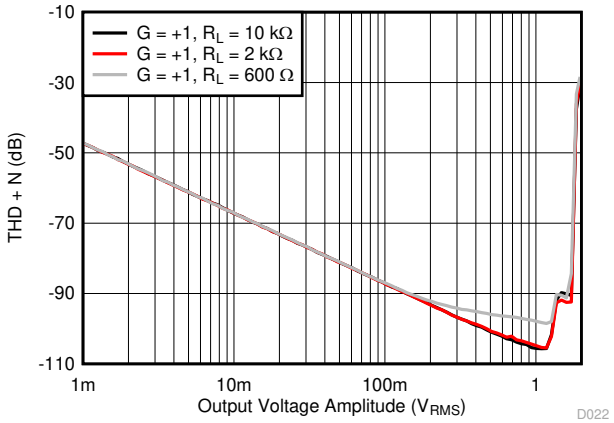
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_{OUT} = 0.5V_{RMS} G = +1 V_{CM} = 2.5V
BW = 80kHz

Figure 5-29. THD + N vs Frequency



f = 1kHz G = +1 V_{CM} = 2.5V
BW = 80kHz

Figure 5-30. THD + N vs Amplitude

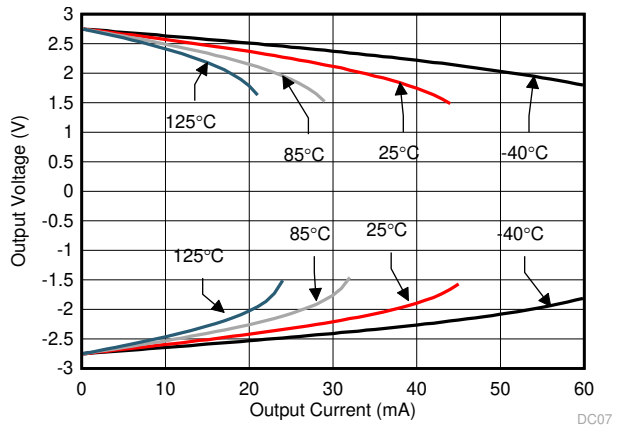


Figure 5-31. Output Voltage Swing vs Output Current

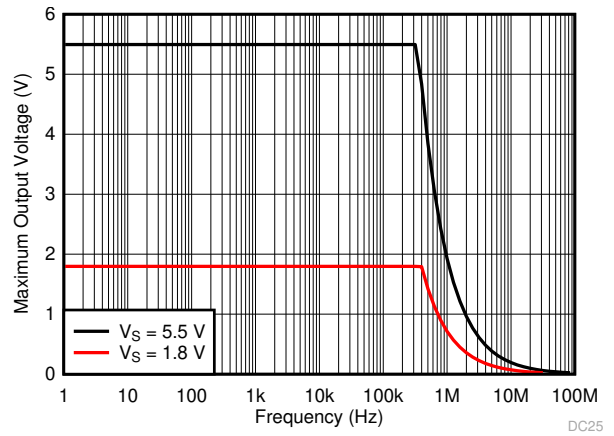


Figure 5-32. Maximum Output Voltage vs Frequency and Supply Voltage

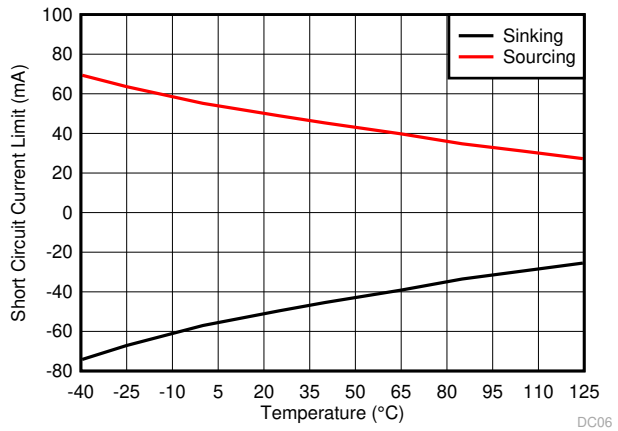


Figure 5-33. Short-Circuit Current vs Temperature

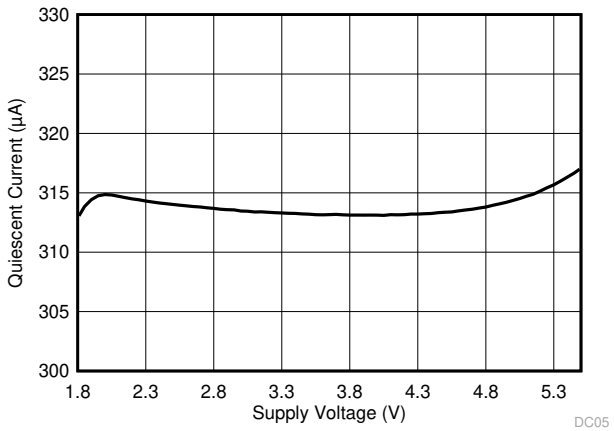


Figure 5-34. Quiescent Current vs Supply Voltage

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

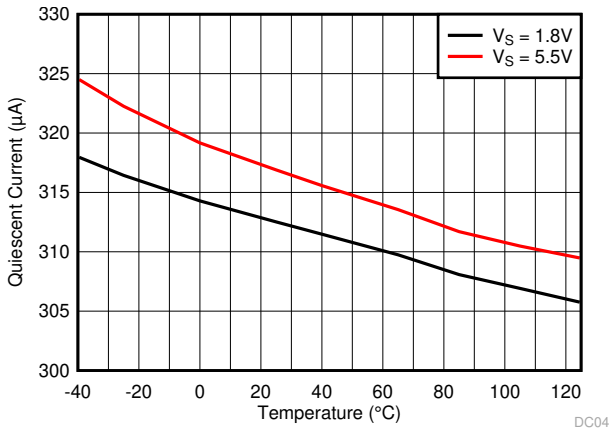


Figure 5-35. Quiescent Current vs Temperature

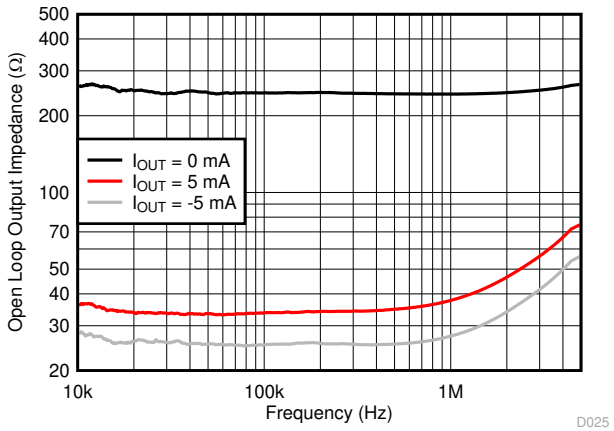
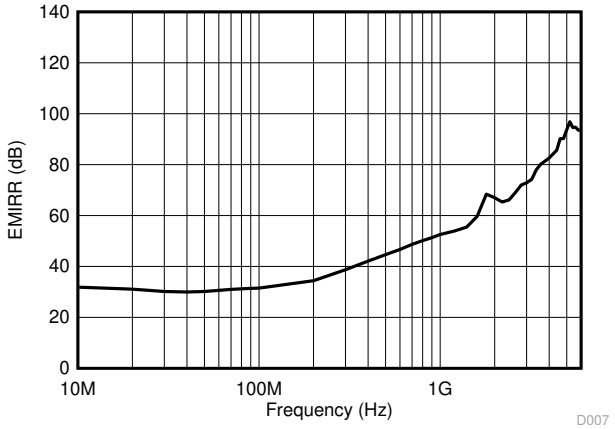
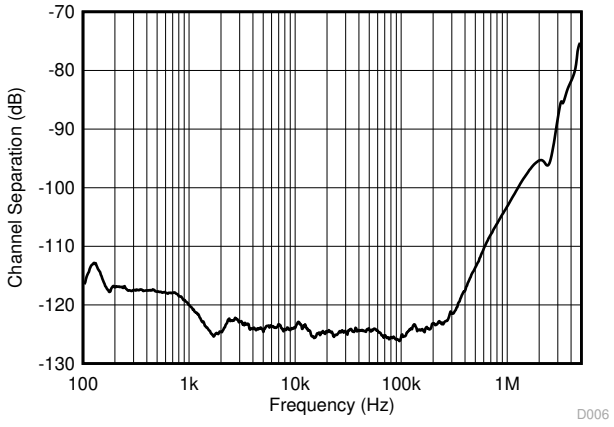


Figure 5-36. Open-Loop Output Impedance vs Frequency



P_{RF} = –10dBm

Figure 5-37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



P_{RF} = –10dBm

Figure 5-38. Channel Separation vs Frequency

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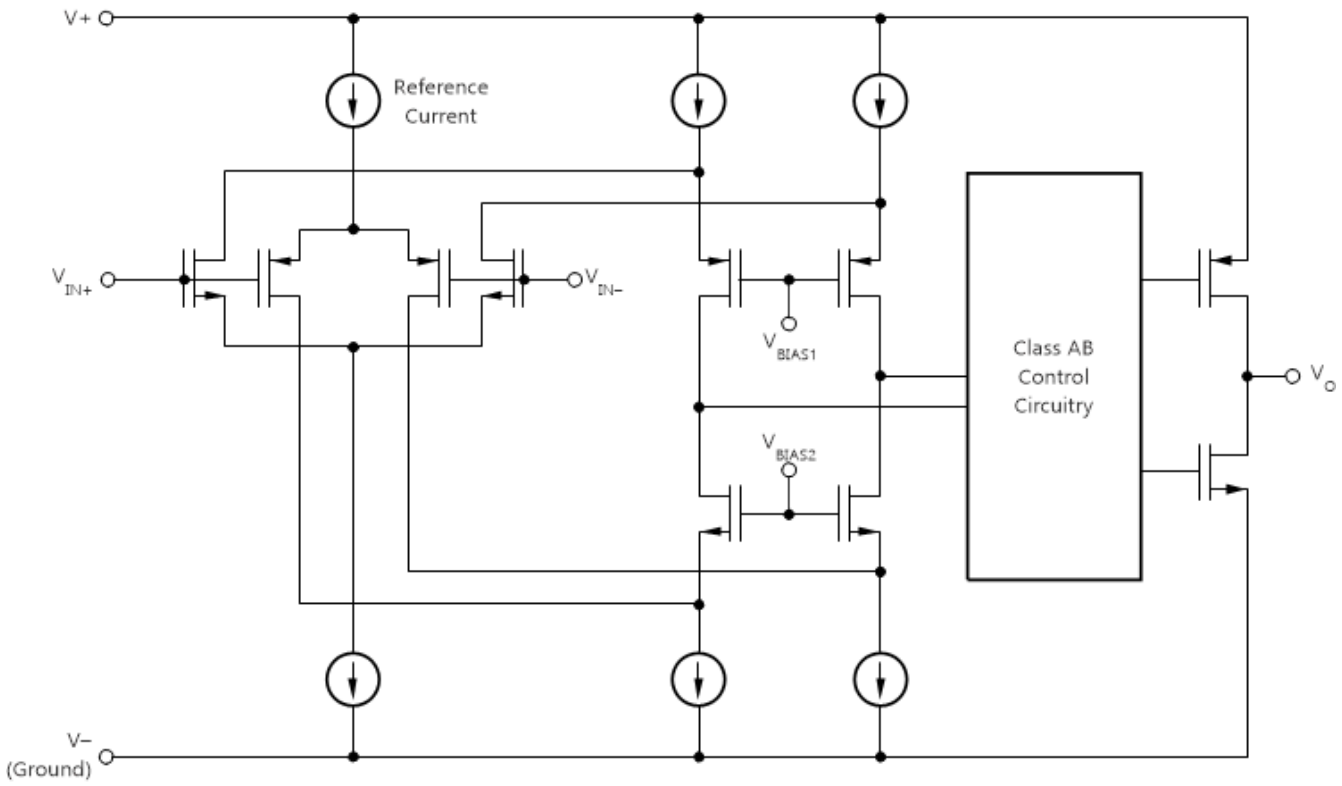
6 Detailed Description

6.1 Overview

The TLV905x-Q1 devices are a 5MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 6V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x-Q1 family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Operating Voltage

The TLV905x-Q1 family of op amps is specified for operation from 1.8V to 6.0V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics*.

6.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV905x-Q1 family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 6.0V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4V to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately (V+) – 1.4V. There is a small transition region, typically (V+) – 1.2V to (V+) – 1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4V to (V+) – 1.2V on the low end, and up to (V+) – 1V to (V+) – 0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

6.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x-Q1 family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 16mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

6.3.4 EMI Rejection

The TLV905x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-1 shows the results of this testing on the TLV905x-Q1. Table 6-1 lists the EMIRR IN+ values for the TLV905x-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

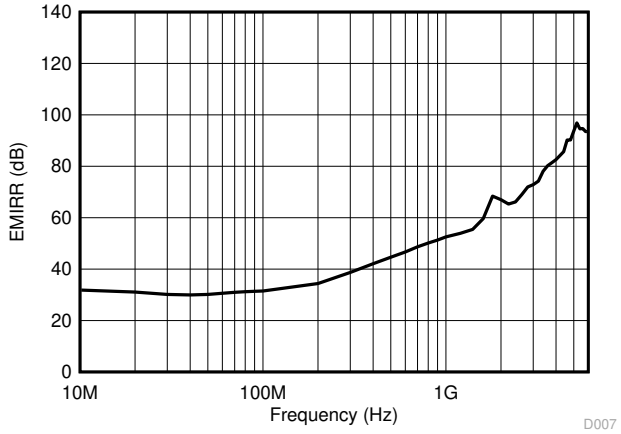

Figure 6-1. EMIRR Testing

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Table 6-1. TLV905x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	41.8dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	53.1dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	71.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	81.2dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	92.5dB

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6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to a linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x-Q1 family is approximately 300ns.

6.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance ESD circuitry has to an electrical overstress event is helpful. Figure 6-2 shows the ESD circuits contained in the TLV905x-Q1 devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where the diode routes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

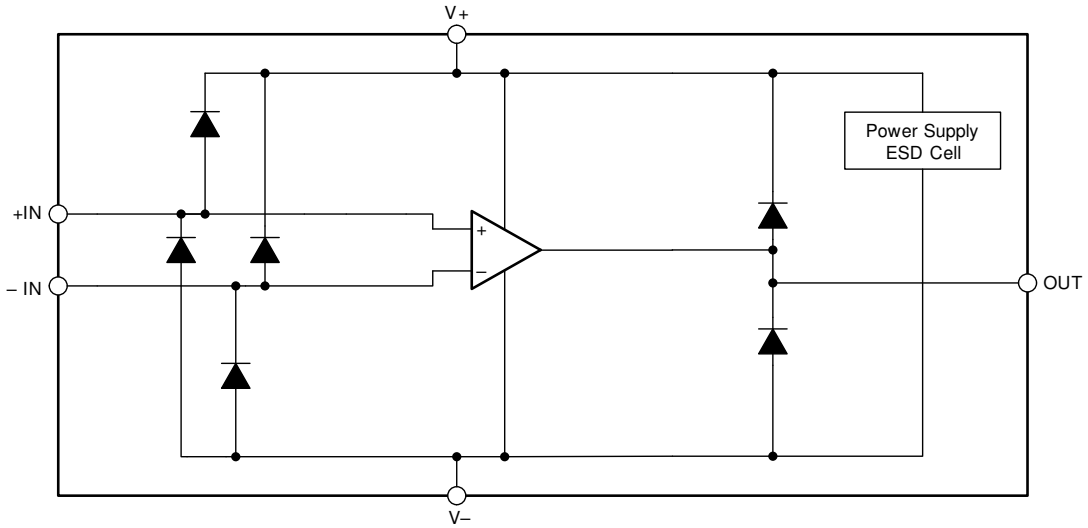

Figure 6-2. Equivalent Internal ESD Circuitry

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6.3.7 Input Protection

The TLV905x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA (for more information, see *Absolute Maximum Ratings*). Figure 6-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

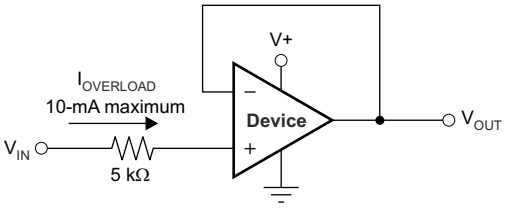

Figure 6-3. Input Current Protection

6.4 Device Functional Modes

The TLV905x-Q1 family is operational when the power-supply voltage is between 1.8V (±0.9V) and 6.0V (±3.0V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV905x-Q1 family features 5MHz bandwidth and very high slew rate of 15V/µs with only 330µA of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of 15nV/√Hz at 10kHz, low input bias current, and a typical input offset voltage of 0.33mV.

7.2 Typical Low-Side Current Sense Application

Figure 7-1 shows the TLV905x-Q1 configured in a low-side current sensing application.

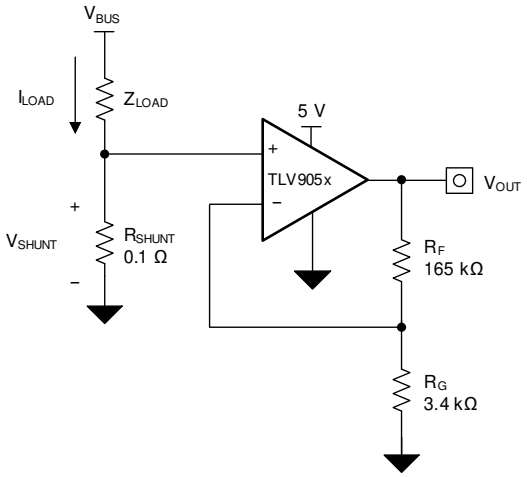

Figure 7-1. TLV905x-Q1 in a Low-Side, Current-Sensing Application

7.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.95V
- Maximum shunt voltage: 100mV

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7.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} equals 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV905x-Q1 device to produce an output voltage of approximately 0V to 4.95V. Equation 3 calculates the gain required for the TLV905x-Q1 device to produce the required output voltage.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT_{MIN}}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using Equation 3, the required gain equals 49.5V/V, which is set with the R_F and R_G resistors. Equation 4 sizes the R_F and R_G, resistors to set the gain of the TLV905x-Q1 device to 49.5V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165kΩ and R_G to equal 3.4kΩ provides a combination that equals approximately 49.5V/V. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.3 Application Curve

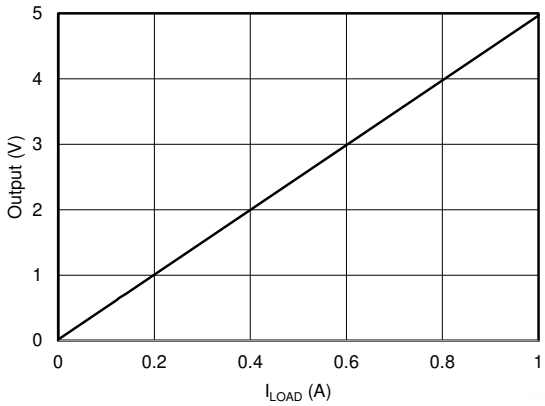

Figure 7-2. Low-Side, Current-Sense Transfer Function

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7.3 Power Supply Recommendations

The TLV905x-Q1 family is specified for operation from 1.8V to 6.0V (±0.9V to ±3.0V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7V can permanently damage the device; for more information, see the *Absolute Maximum Ratings* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see *Figure 7-3*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 7-3, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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7.4.2 Layout Example

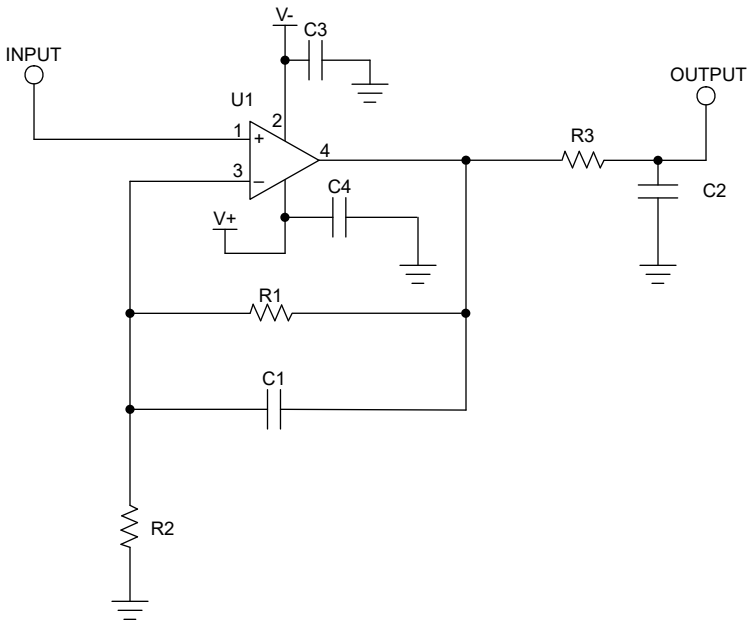

Figure 7-3. Schematic for Noninverting Configuration Layout Example

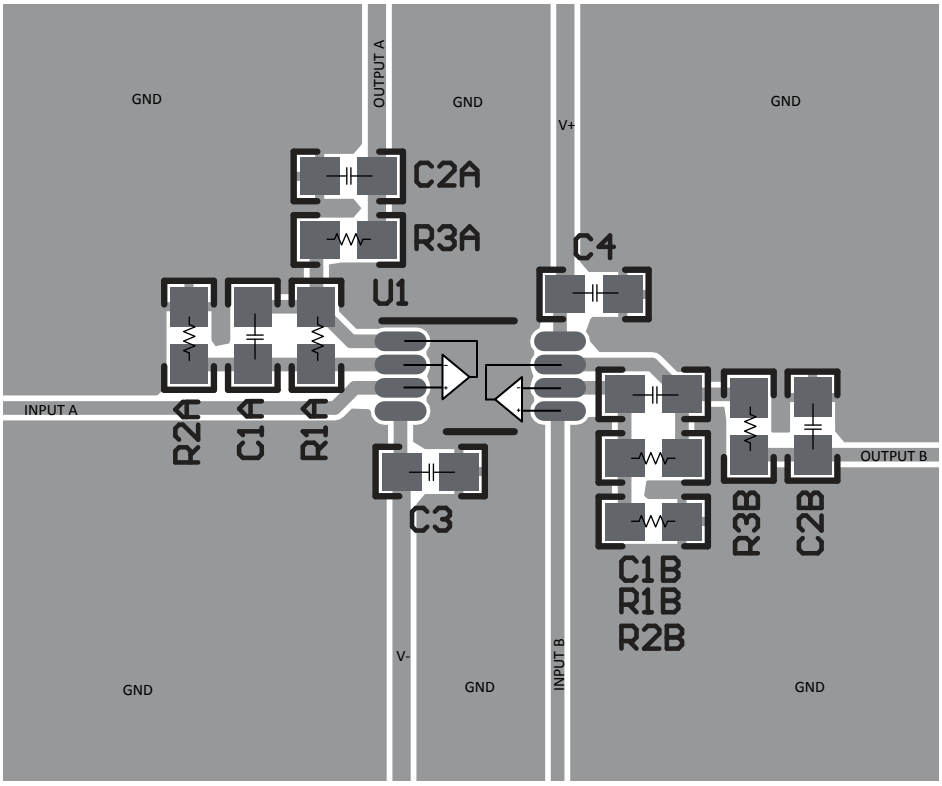

Figure 7-4. Example Layout for VSSOP-8 (DGK) Package

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Low Voltage, High Slew Rate Op-amps for Motor Drive Circuits* application report
- Texas Instruments, *TI Analog Circuit Cookbook* Analog Engineer's Circuit
- Texas Instruments, *TI Precision Labs - Amplifiers* training video

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

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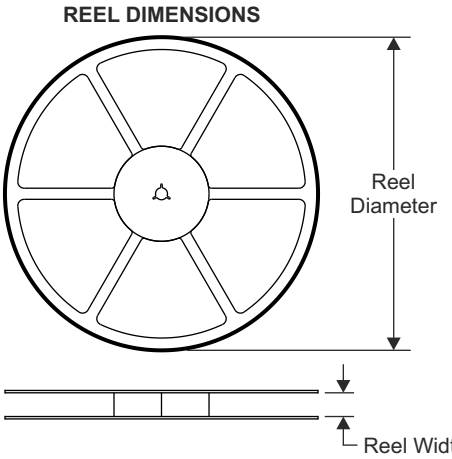
9 Revision History

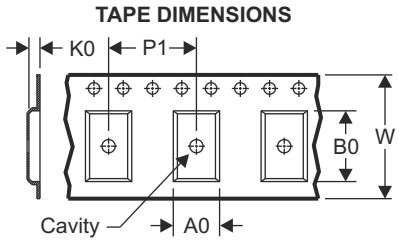
DATE	REVISION	NOTES
February 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

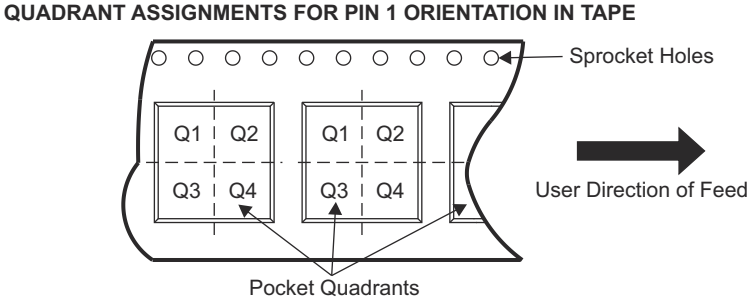
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

10.1 Tape and Reel Information





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051QDBVRQ1	SOT-23	DBV	5	3000	180	8	3.2	3.2	1.4	4	5.3	Q3
TLV9052QPWRQ1	TSSOP	PW	8	3000	330	12	7	3.6	1.6	8	12	Q3

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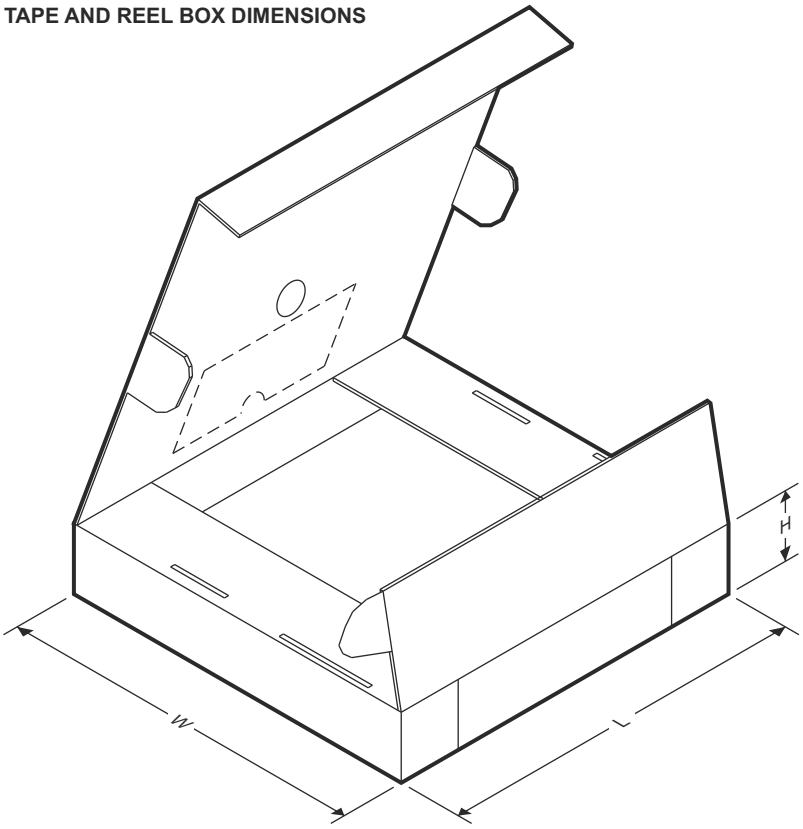
ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051QDBVRQ1	SOT-23	DBV	5	3000	210	185	35
TLV9052QPWRQ1	TSSOP	PW	8	3000	470	380	18

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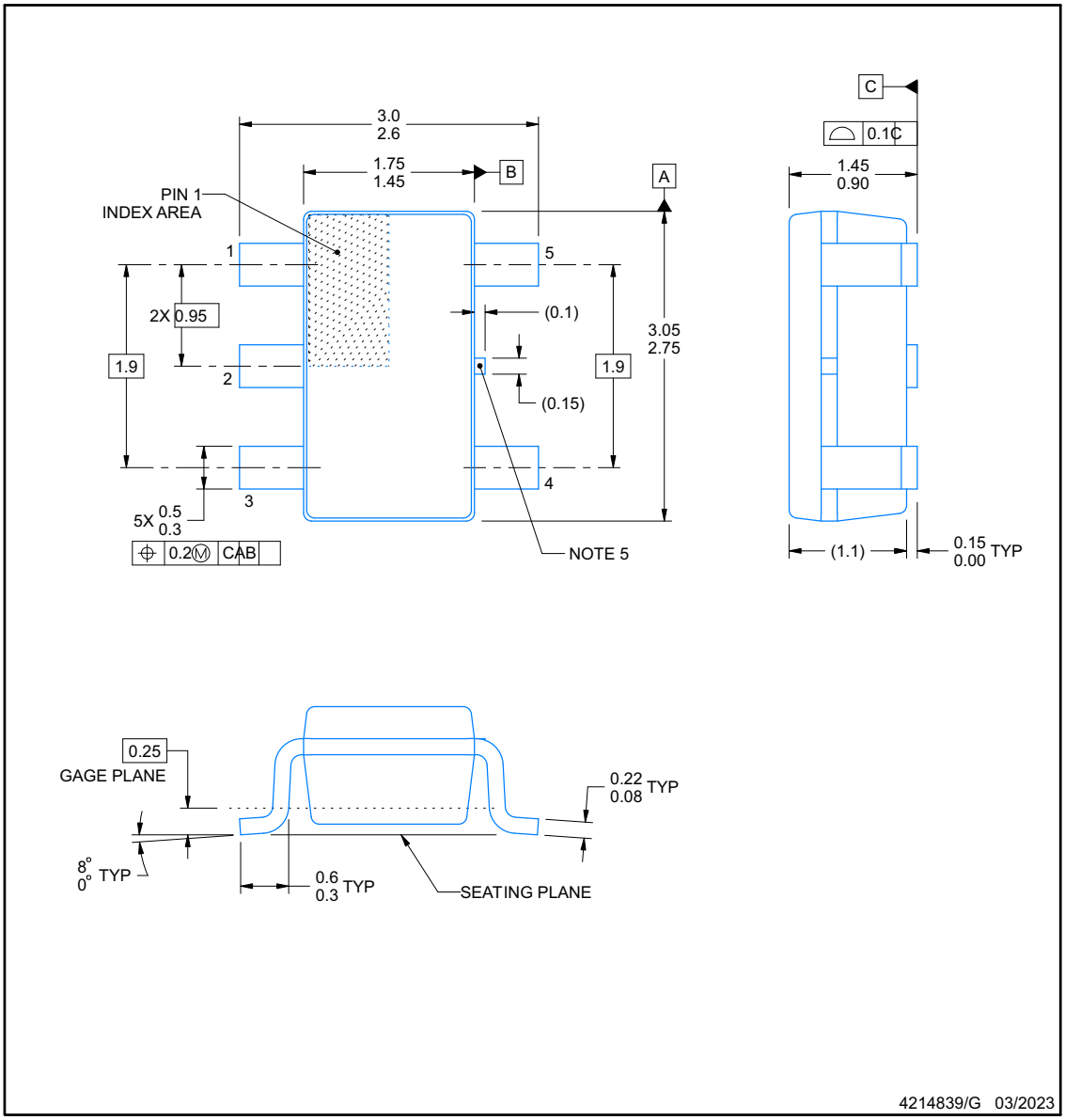
10.2 Mechanical Data

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

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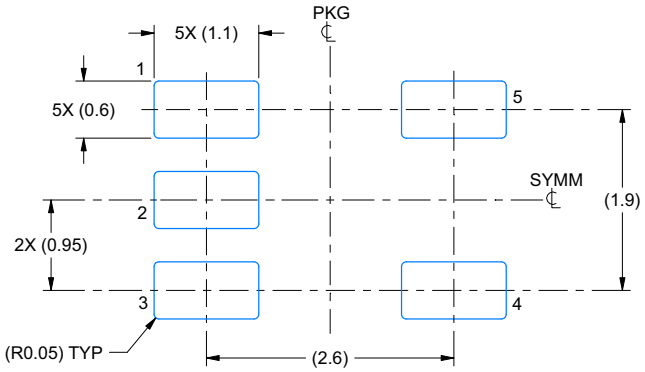
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

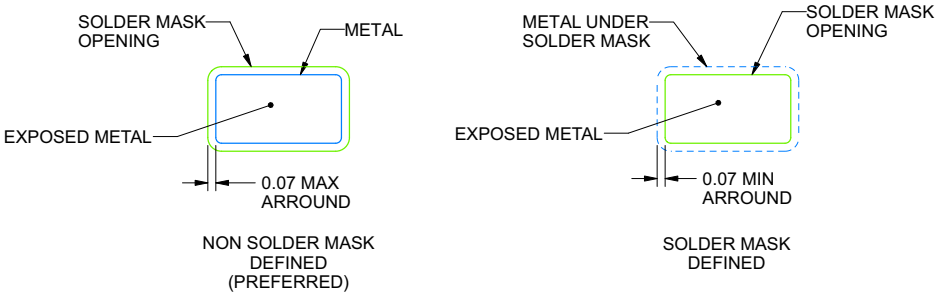
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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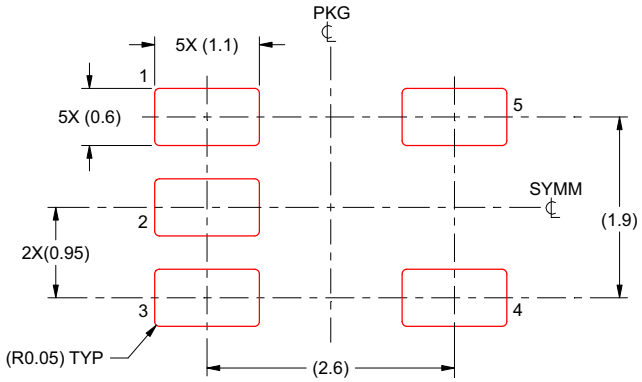
EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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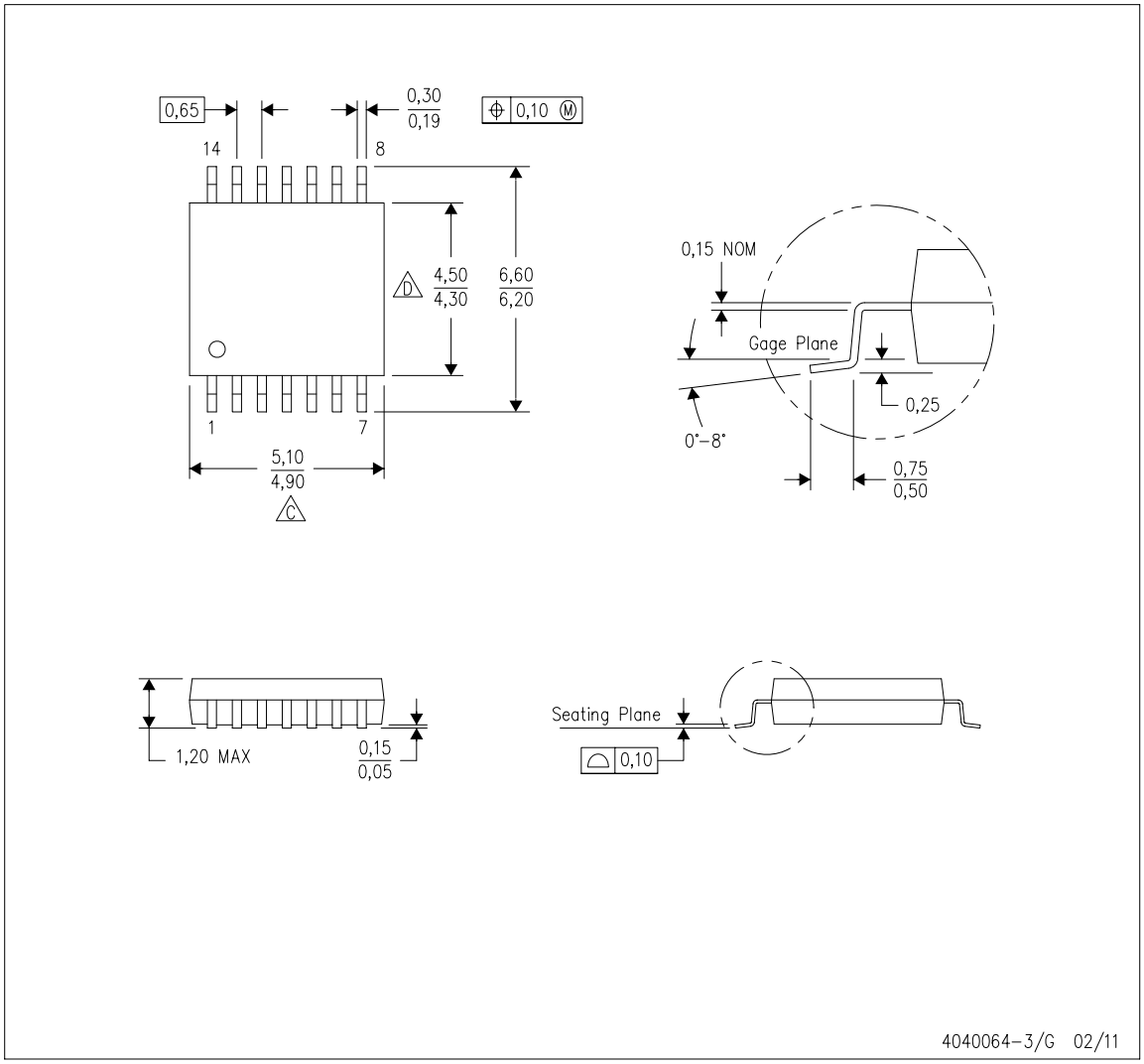
MECHANICAL DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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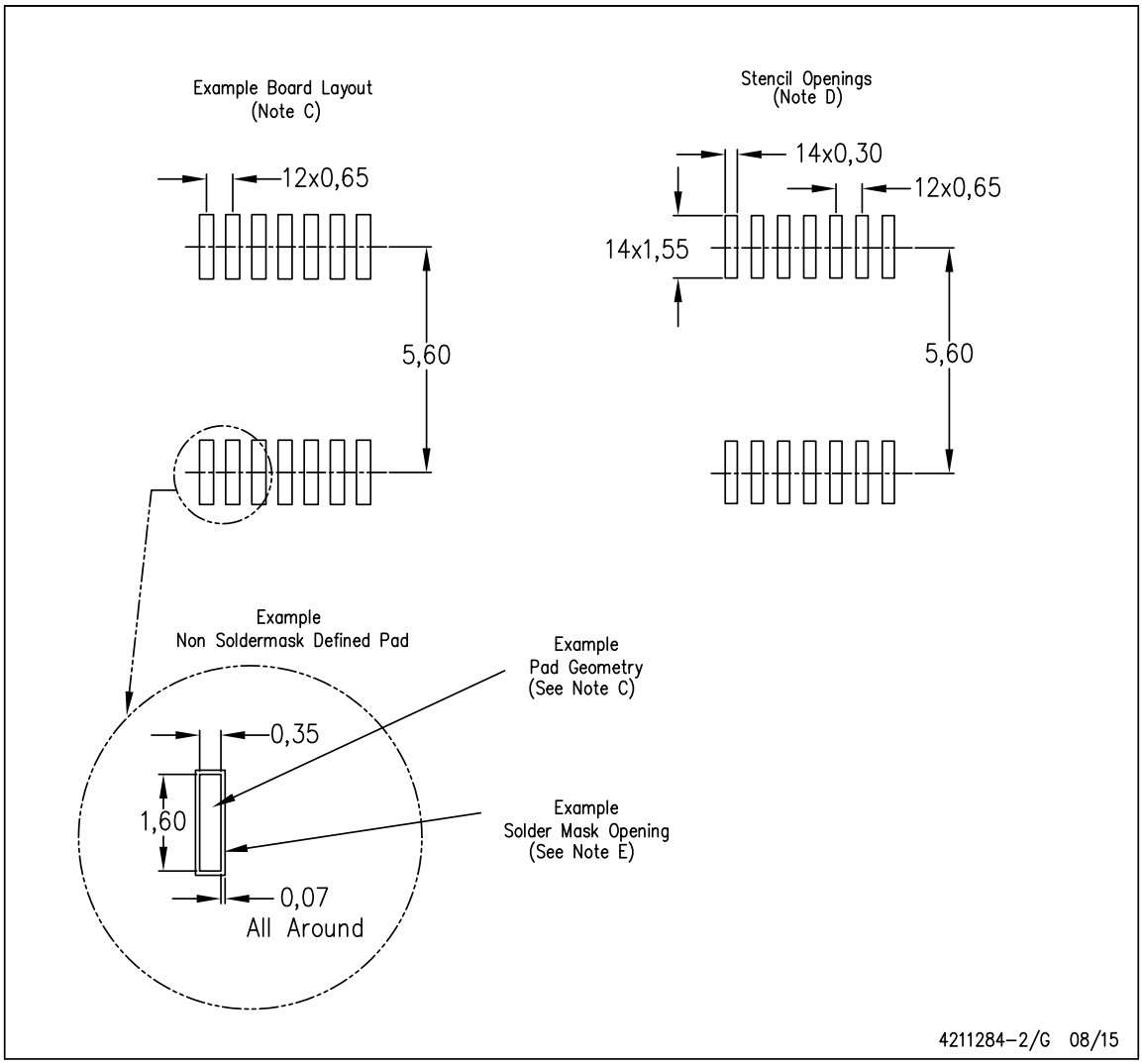
LAND PATTERN DATA

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9051QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV9052QPWRQ1	ACTIVE	TSSOP	PW	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV9052-Q1 :

- Catalog : TLV9052

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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