TPS22930 Ultra Small, Low On-Resistance Load Switch with Controlled Turn-On

1 Features

- Integrated single channel load switch
- Ultra small four terminal wafer-chip-scale package (nominal dimensions shown see addendum for details)
  - 0.9 mm × 0.9 mm, 0.5 mm pitch, 0.5-mm height (YZV)
- Input voltage range: 1.4 V to 5.5 V
- Ultra low R_{ON} resistance
  - R_{ON} = 35 mΩ at V_{IN} = 5 V
  - R_{ON} = 36 mΩ at V_{IN} = 3.6 V
  - R_{ON} = 49 mΩ at V_{IN} = 1.8 V
- 2-A maximum continuous switch current
- Low quiescent current (< 3 µA)
- Low control input threshold enables use of 1.2-V/1.8-V/2.5-V/3.3-V logic
- Controlled slew rate
- Under voltage lockout
- Reverse current protection when disabled

2 Applications

- Smartphone / wireless handsets
- Portable industrial / medical equipment
- Portable media players
- Point of sales terminals
- GPS navigation devices
- Digital cameras
- Portable instrumentation

3 Description

The TPS22930 is a small, low R_{ON} load switch with controlled turn on. The device contains a P-channel MOSFET that can operate over an input voltage range of 1.4 V to 5.5 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22930 is active high enable.

The TPS22930 device provides circuit breaker functionality by disabling the body diode during reverse voltage (also known as reverse current) situations. Reverse current protection is active only when the power-switch is disabled (off). The device disengages the body diode when the output voltage (V_{OUT}) is driven higher than the input (V_{IN}) to stop the flow of current towards the input side of the switch. Additionally, under-voltage lockout (UVLO) protection turns the switch off if the input voltage is too low.

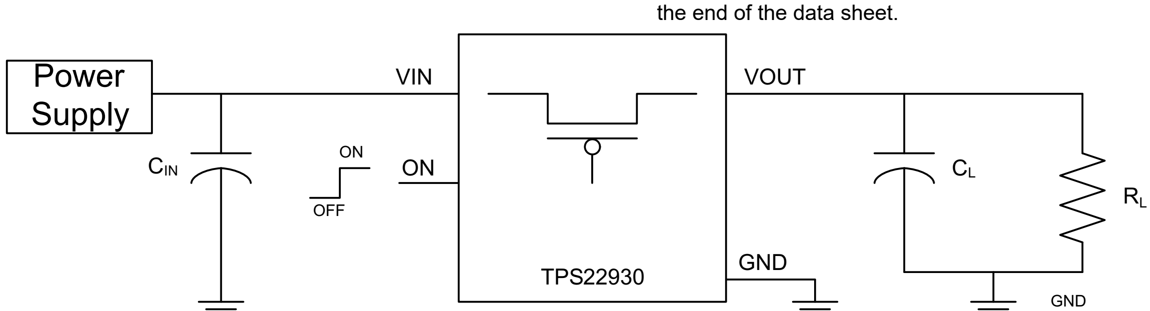
The slew rate of the device is internally controlled in order to avoid inrush current.

The TPS22930 is available in an ultra-small, space-saving 4-pin CSP package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
TPS22930	DSBGA (4)	0.92 mm × 0.92 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2021) to Revision D (July 2021) **Page**

- Updated $I_{RCP(leak)}$ spec to 2.6 μA.....5

Changes from Revision B (February 2016) to Revision C (January 2021) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document 1

Changes from Revision A (June 2015) to Revision B (February 2016) **Page**

- Made changes to *Pin Configurations and Functions* 1

Changes from Revision * (November 2012) to Revision A (June 2015) **Page**

- Removed Ordering Information table.....1
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Input voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse ≤1ms, 25% duty cycle		2.5	A
T_A	Operating free-air temperature [(3)]	–40	85	°C
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		1.4	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range		0	V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{IN} = 3.61 V to 5.5 V	1.1	5.5	V
		V_{IN} = 1.4 V to 3.6 V	1.1	5.5	
V_{IL}	Low-level input voltage, ON	V_{IN} = 3.61 V to 5.5 V	0	0.6	V
		V_{IN} = 1.4 V to 3.6 V	0	0.4	
C_{IN}	Input capacitor		1[(1)]		µF

(1) Refer to *Application Information* section.

5.4 Thermal Information

THERMAL METRIC[(1)]		TPS22930 YZV (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

Unless otherwise note, the specification in the following table applies over the operating ambient temperature **–40°C ≤ T_A ≤ 85°C** (Full). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
I_{IN}	Quiescent current	I_{OUT} = 0 V, V_{IN} = V_{ON} = 5.25 V	Full		2.3	10	μA
		I_{OUT} = 0 V, V_{IN} = V_{ON} = 4.2 V	Full		2.2	7	μA
		I_{OUT} = 0 V, V_{IN} = V_{ON} = 3.6 V	Full		2.1	7	μA
		I_{OUT} = 0 V, V_{IN} = V_{ON} = 2.5 V	Full		1.0	5	μA
		I_{OUT} = 0 V, V_{IN} = V_{ON} = 1.5 V	Full		0.8	5	μA
$I_{IN(off)}$	Off supply current	V_{OUT} = Open, V_{IN} = 5.25 V, V_{ON} = 0 V	Full		0.3	10	μA
		V_{OUT} = Open, V_{IN} = 4.2 V, V_{ON} = 0 V	Full		0.2	7	μA
		V_{OUT} = Open, V_{IN} = 3.6 V, V_{ON} = 0 V	Full		0.2	7	μA
		V_{OUT} = Open, V_{IN} = 2.5 V, V_{ON} = 0 V	Full		0.1	5	μA
		V_{OUT} = Open, V_{IN} = 1.5 V, V_{ON} = 0 V	Full		0.1	5	μA
$I_{IN(leak)}$	Leakage current	V_{OUT} = 0 V, V_{IN} = 5.25 V, V_{ON} = 0 V	Full		0.8	10	μA
		V_{OUT} = 0 V, V_{IN} = 4.2 V, V_{ON} = 0 V	Full		0.2	7	μA
		V_{OUT} = 0 V, V_{IN} = 3.6 V, V_{ON} = 0 V	Full		0.2	7	μA
		V_{OUT} = 0 V, V_{IN} = 2.5 V, V_{ON} = 0 V	Full		0.1	5	μA
		V_{OUT} = 0 V, V_{IN} = 1.5 V, V_{ON} = 0 V	Full		0.1	5	μA
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V	Full			0.5	μA
$I_{RCP(leak)}$	Reverse leakage current	V_{IN} = V_{ON} = GND, V_{OUT} = 5 V, measured from V_{IN}	Full			2.6	μA
UVLO	Undervoltage lockout	V_{IN} increasing, VON = 3.6 V, IOUT = –100 mA	Full			1.2	
		V_{IN} decreasing, VON = 3.6 V, IOUT = –100 mA	Full	0.5			
RESISTANCE CHARACTERISTICS							
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{IN} = 5.0 V	25°C		35	44	mΩ
			Full			50	mΩ
		I_{OUT} = –200 mA, V_{IN} = 4.2 V	25°C		35	44	mΩ
			Full			50	mΩ
		I_{OUT} = –200 mA, V_{IN} = 3.6 V	25°C		36	44	mΩ
			Full			50	mΩ
		I_{OUT} = –200 mA, V_{IN} = 2.5 V	25°C		39	44	mΩ
			Full			50	mΩ
		I_{OUT} = –200 mA, V_{IN} = 1.8 V	25°C		49	55	mΩ
			Full			62	mΩ
		I_{OUT} = –200 mA, V_{IN} = 1.5 V	25°C		59	66	mΩ
			Full			74	mΩ

5.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} = 5.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 μF		4.8		μs
t_{OFF}	Turn-off time			6.3		
t_R	V_{OUT} rise time			5.6		
t_F	V_{OUT} fall time			2.8		
V_{IN} = 4.2 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 μF		5.8		μs
t_{OFF}	Turn-off time			7.3		
t_R	V_{OUT} rise time			5.4		
t_F	V_{OUT} fall time			2.8		
V_{IN} = 3.0 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 μF		7.4		μs
t_{OFF}	Turn-off time			9.5		
t_R	V_{OUT} rise time			6.3		
t_F	V_{OUT} fall time			2.9		

5.7 Typical Characteristics

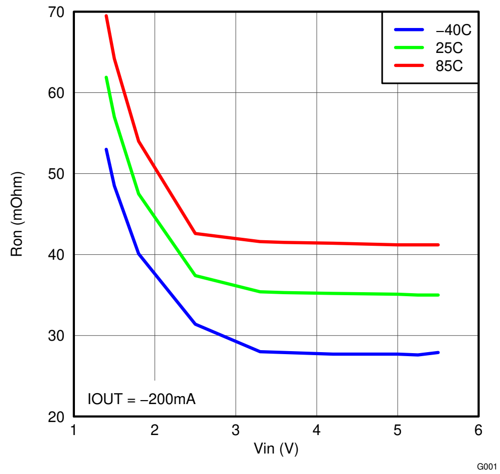


Figure 5-1. R_{ON} vs V_{IN}

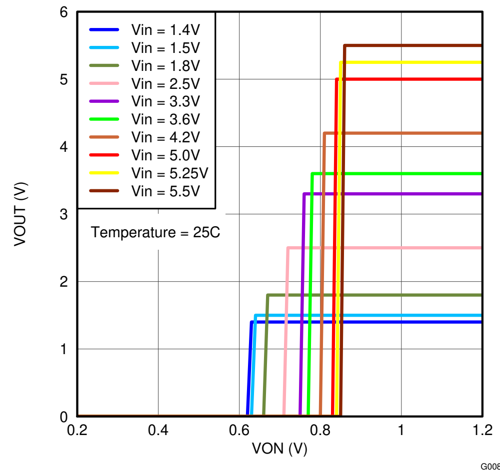


Figure 5-2. On Input Threshold

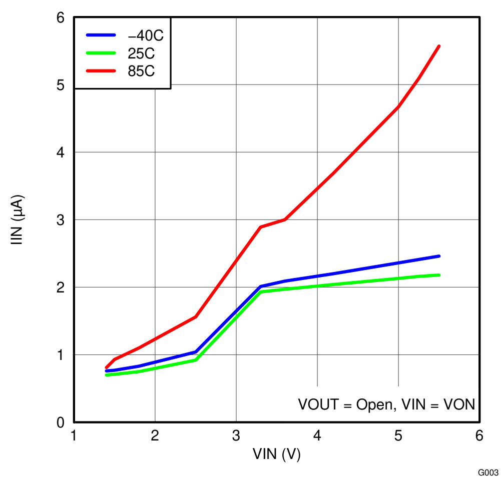


Figure 5-3. I_{IN} vs V_{IN}

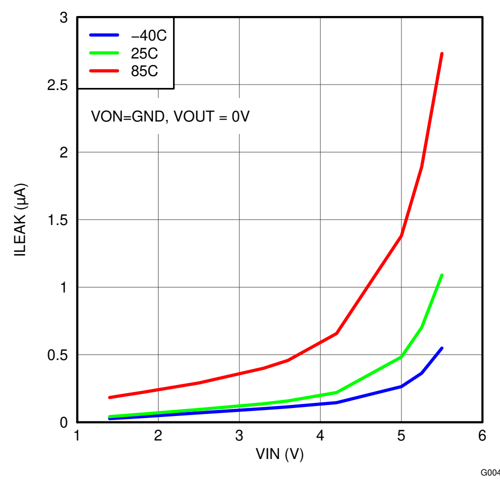


Figure 5-4. $I_{IN(leak)}$ vs V_{IN}

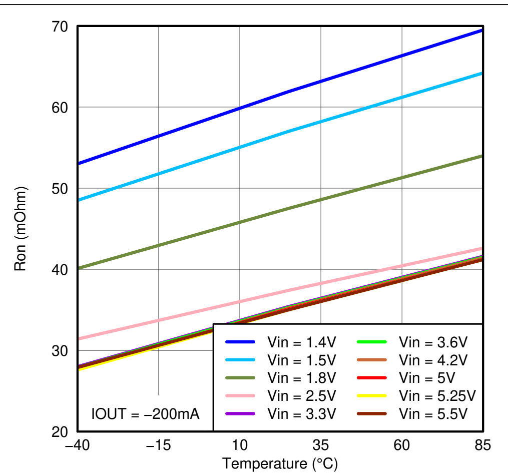


Figure 5-5. Temperature vs R_{ON}

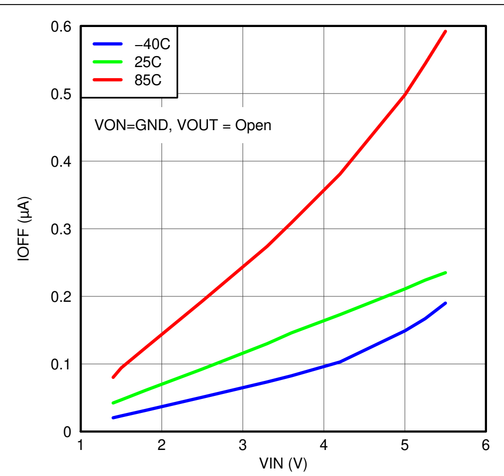


Figure 5-6. $I_{IN(off)}$ vs V_{IN}

5.7 Typical Characteristics (continued)

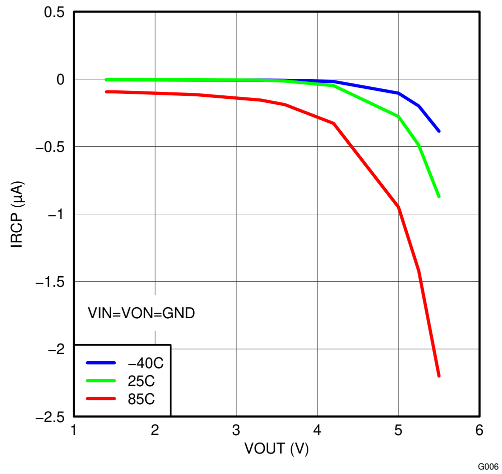


Figure 5-7. $I_{RCP(leak)}$ vs V_{OUT} (Measured On VIN)

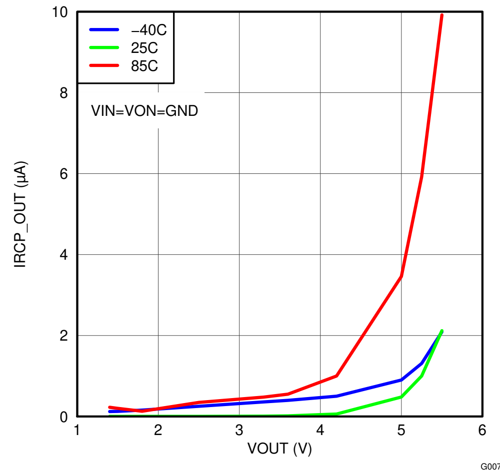


Figure 5-8. $I_{RCP(leak)}$ vs V_{OUT} (Measured on VOUT)

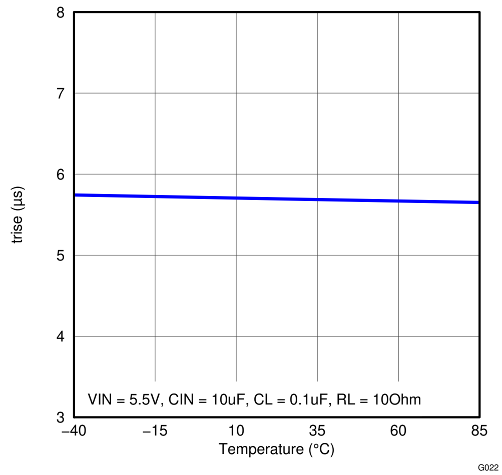


Figure 5-9. t_R vs Temperature (V_{IN} = 5.5 V)

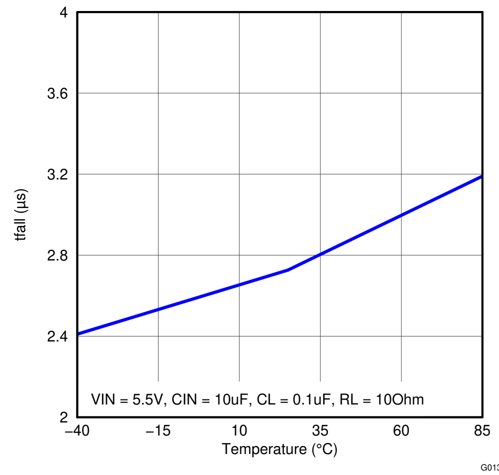


Figure 5-10. t_F vs Temperature (V_{IN} = 5.5 V)

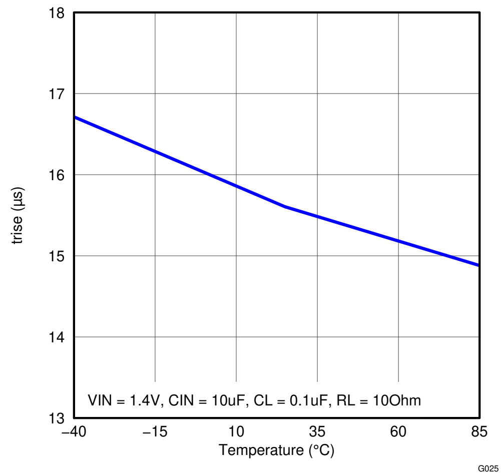


Figure 5-11. t_R vs Temperature (V_{IN} = 1.4 V)

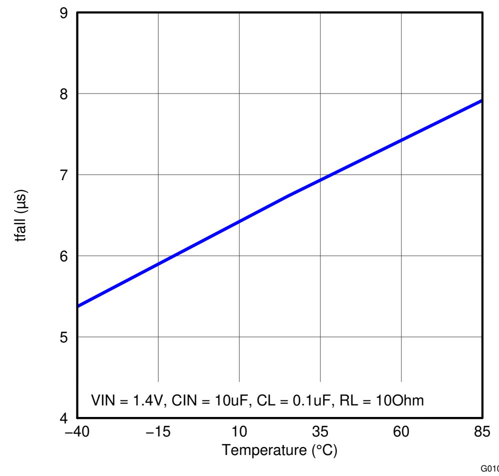


Figure 5-12. t_F vs Temperature (V_{IN} = 1.4 V)

5.7 Typical Characteristics (continued)

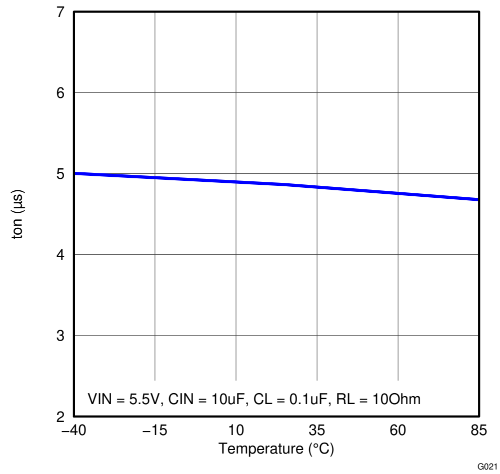


Figure 5-13. t_{ON} vs Temperature (V_{IN} = 5.5 V)

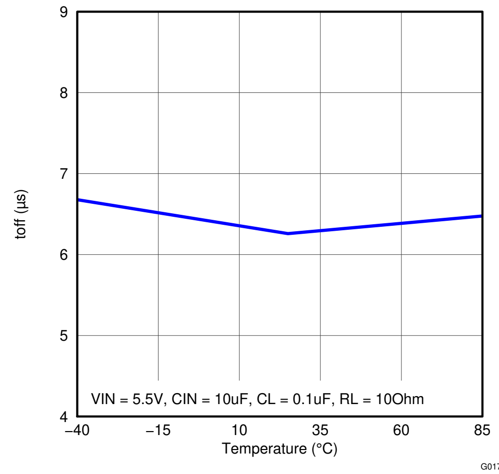


Figure 5-14. t_{OFF} vs Temperature (V_{IN} = 5.5 V)

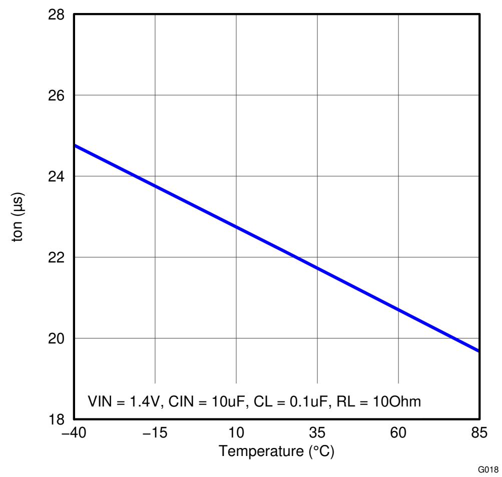


Figure 5-15. t_{ON} vs Temperature (V_{IN} = 1.4 V)

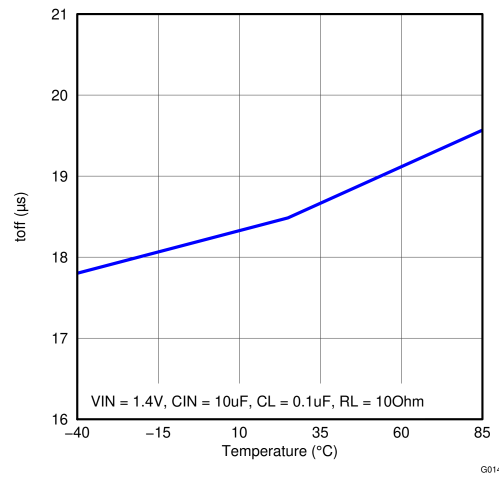


Figure 5-16. t_{OFF} vs Temperature (V_{IN} = 1.4 V)

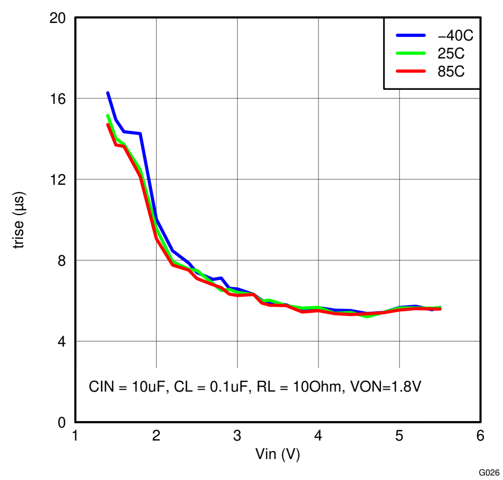


Figure 5-17. t_R vs V_{IN}

5.7.1 Typical AC Scope Captures at T_A = 25°C

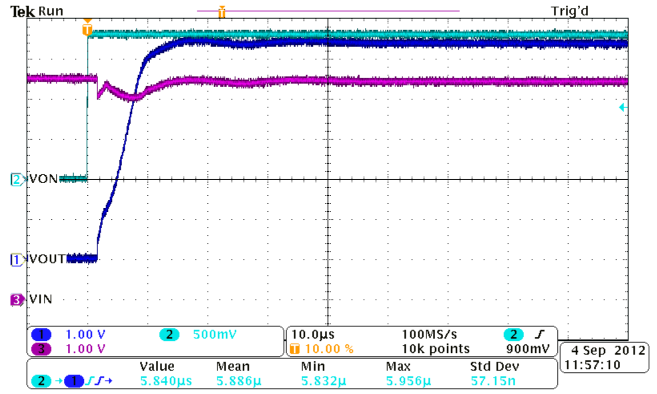


Figure 5-18. Turn-On Response Time (V_{IN} = 5.5 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

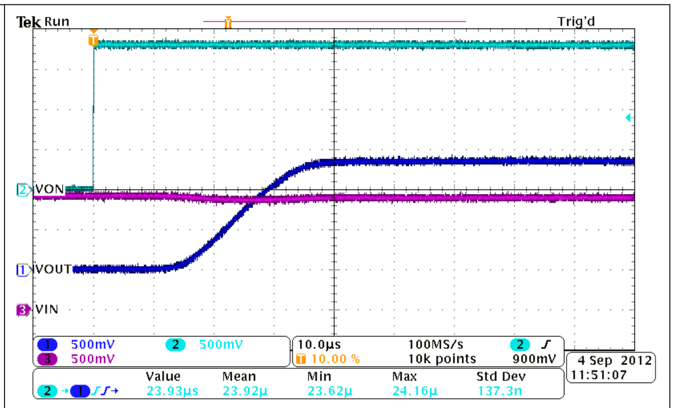


Figure 5-19. Turn-On Response Time (V_{IN} = 1.4 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

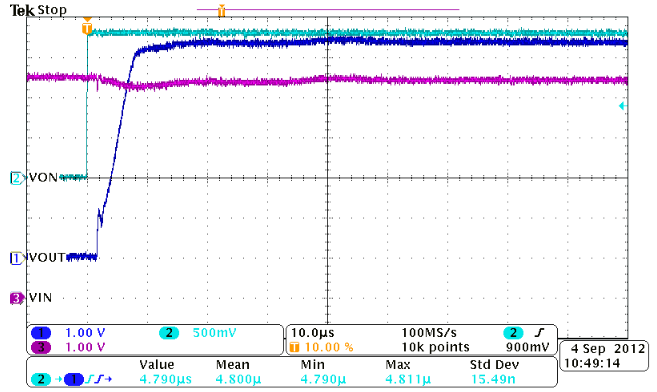


Figure 5-20. Turn-On Response Time (V_{IN} = 5.5 V, C_{IN} = 10 µF, C_L = 0.1 µF, R_L = 10 Ω)

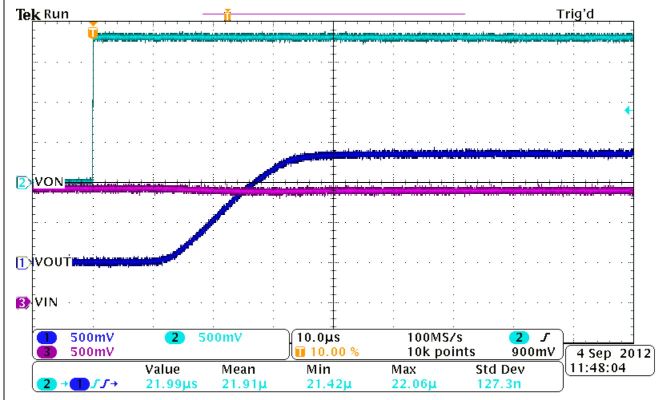


Figure 5-21. Turn-On Response Time (V_{IN} = 1.4 V, C_{IN} = 10 µF, C_L = 0.1 µF, R_L = 10 Ω)

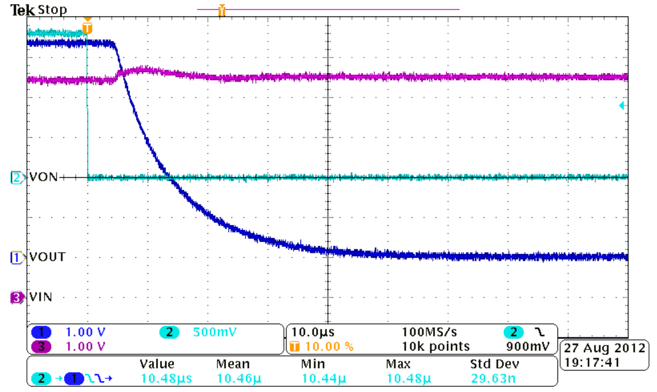


Figure 5-22. Turn-Off Response Time (V_{IN} = 5.5 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

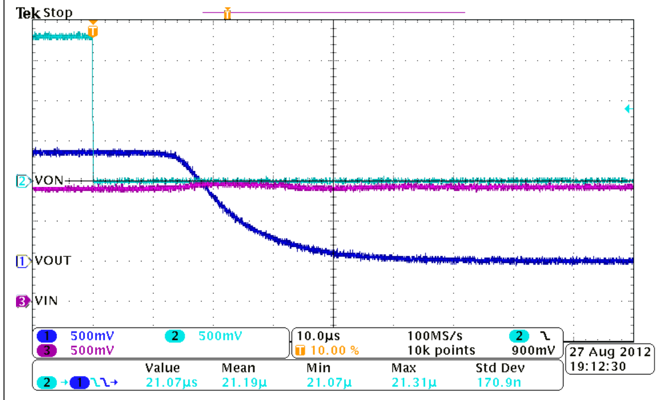


Figure 5-23. Turn-Off Response Time (V_{IN} = 1.4 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

5.7.1 Typical AC Scope Captures at T_A = 25°C (continued)

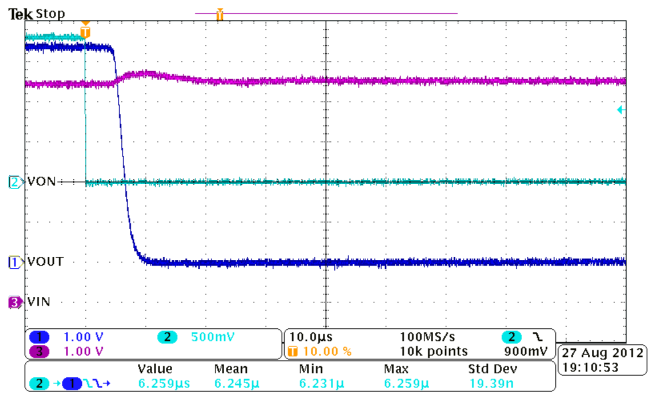


Figure 5-24. Turn-Off Response Time (V_{IN} = 5.5 V, C_{IN} = 10 µF, C_L = 0.1 µF, R_L = 10 Ω)

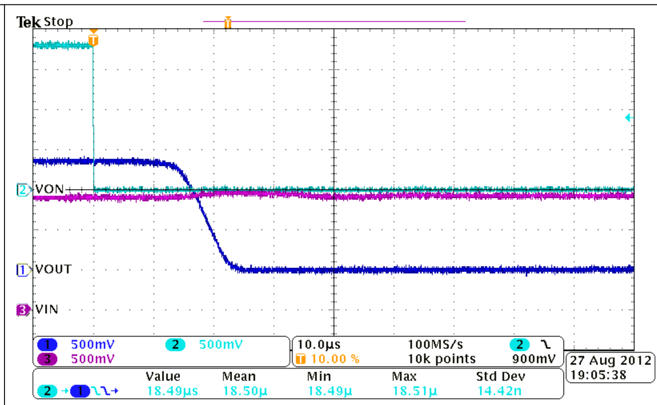


Figure 5-25. Turn-Off Response Time (V_{IN} = 1.4 V, C_{IN} = 10 µF, C_L = 0.1 µF, R_L = 10 Ω)

6 Pin Configuration and Functions

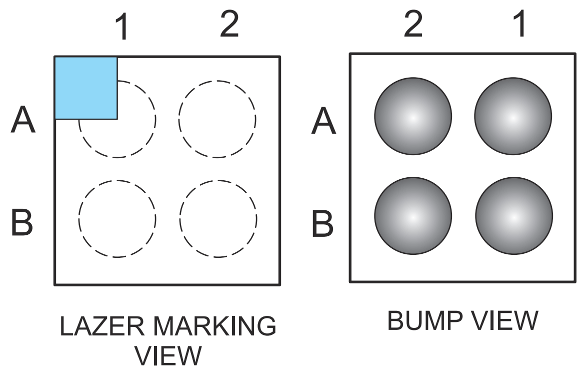


Figure 6-1. YZV Package 4-Pin DSBGA Bottom View

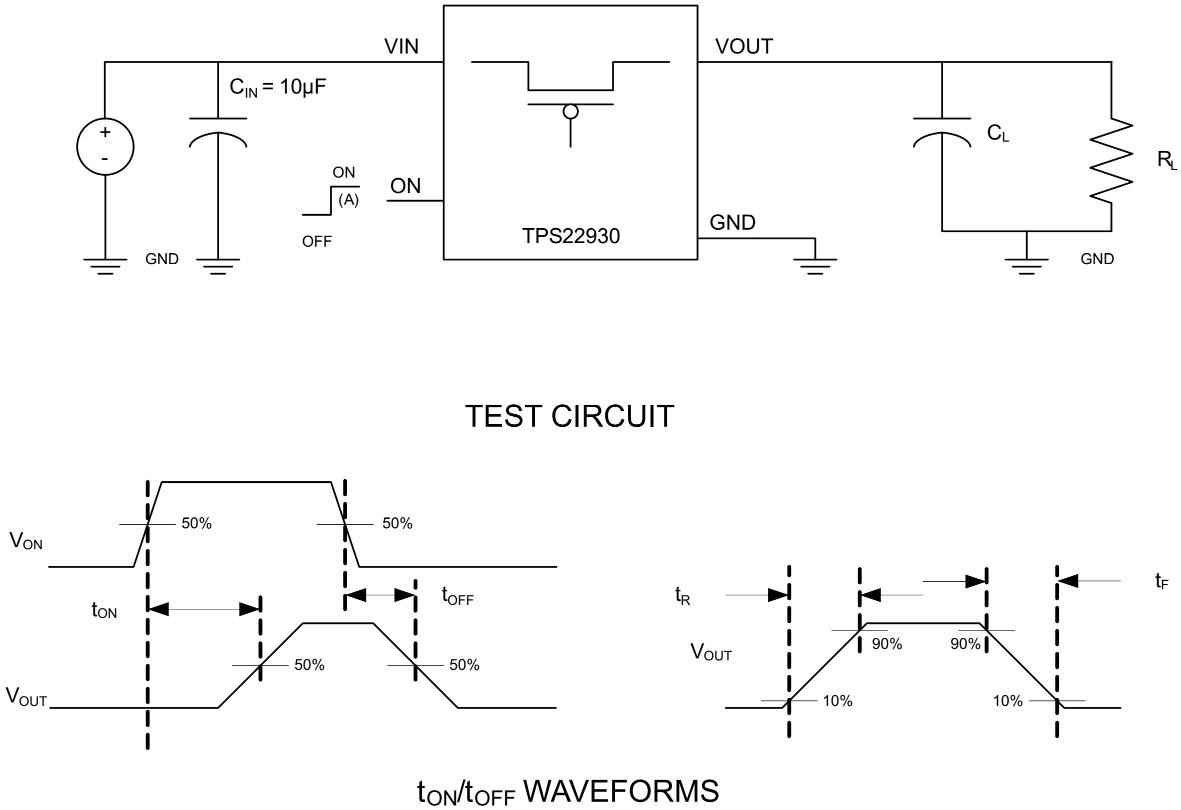
Table 6-1. Pin Assignments

A	VOUT	VIN
B	GND	ON
	1	**2**

Table 6-2. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VOUT	O	Switch output.
A2	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip during transients.
B1	GND	–	Device ground.
B2	ON	I	Switch control input, active high. Do no leave floating.

7 Parameter Measurement Information



(A) Rise and fall times of the control signal are 100ns.

Figure 7-1. Test Circuit and t_{ON}/t_{OFF} Waveforms

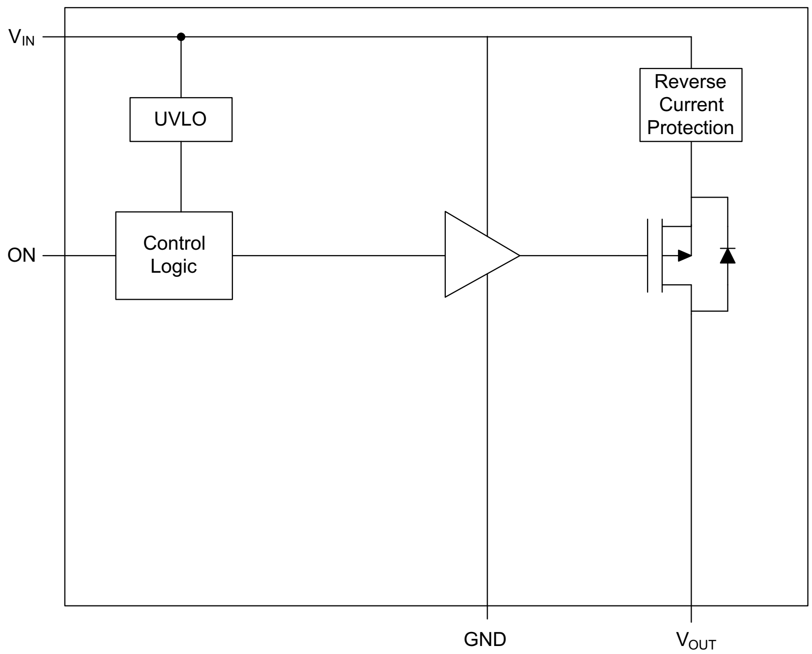
8 Detailed Description

8.1 Overview

The TPS22930 is a single channel, 2-A load switch in a 4-terminal BSGA package. A low enable threshold makes it capable of interfacing directly with low voltage control signals. In the off state, the device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from thee supply. When turning on, the output will rise with a controlled slew rate to limit inrush current.

The device will also disengage the body diode when disabled to provide reverse current protection. The undervoltage lockout (UVLO) threshold will ensure the switch is turned off and will block reverse current if the V_{IN} power supply is removed

8.2 Functional Block Diagram



8.3 Feature Description

Table 8-1. Feature List

DEVICE	R_{ON} (TYP) AT 4.2 V	RISE TIME AT 4.2 V (TYP)	QUICK OUTPUT DISCHARGE(1)	MAXIMUM CONTINUOUS CURRENT	ENABLE
TPS22930A	35 mΩ	5.4 µs	No	2 A	Active High

(1) This feature discharges output of the switch to GND through a resistor, preventing the output from floating when the pass FET is disabled.

8.3.1 On And Off Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage.

8.3.2 UVLO

UVLO turns off the switch if the input voltage drops below the under voltage lockout threshold. With the ON pin active, the input voltage rising above the under voltage lockout threshold will allow a controlled turn-on of the switch to limit current over-shoot.

The maximum UVLO of the TPS22930A is 1.2 V. This is under the minimum V_{IN} voltage and meets the system UVLO requirements. Once the device is disabled through UVLO, it will block reverse current in the case a voltage is applied to V_{OUT}

8.3.3 Reverse Current Protection

Reverse current protection (RCP) is only active when ON is asserted low. When ON is asserted high, current can flow from VOUT to VIN or from VIN to VOUT. This allows the device to function as a bi-directional switch when enabled.

8.4 Device Functional Modes

Table 8-2 describes the state of the switch and the reverse current protection as determined by the ON pin.

Table 8-2. Switch and Reverse Current Protection State

ON	V_{IN} to V_{Out}	RCP
H	On	Off
L	Off	On

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, it is recommended that a capacitor be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 100 times higher than the output capacitor to avoid excessive voltage drop; however, a 100 to 1 ratio is not required for proper functionality of the device.

9.1.2 Output Capacitor (Optional)

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 100 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 100 to 1 ratio is not required for proper functionality of the device.

9.2 Typical Application

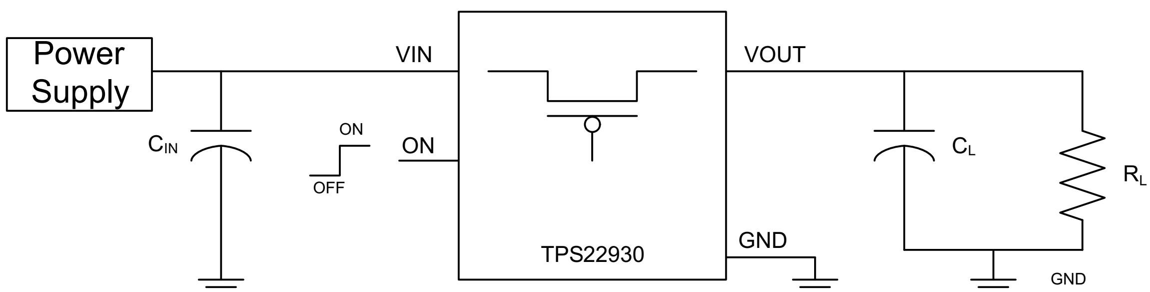


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design example, the following will be used as the system requirements.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN} Range	1.5 V to 5.5 V
UVLO Threshold	< 1.5 V
Reverse Current Protection	Requred
Load Current	1 A
Ambient Temperature	25 °C

9.2.2 Detailed Design Procedure

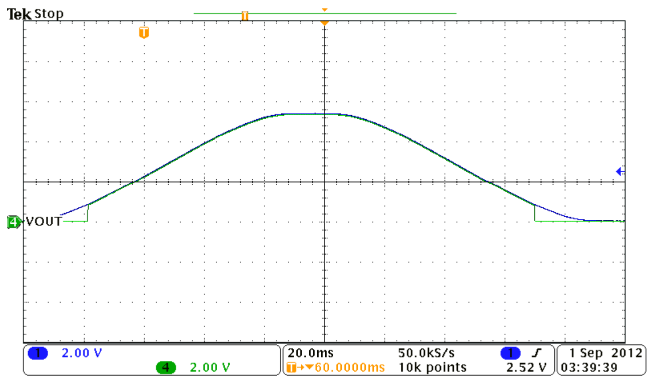
To begin the design process, the designer needs to know the following:

- Input Voltage range
- UVLO Threshold

- Load Current
- Ambient Temperature

9.2.3 Application Curve

UVLO Response shows the UVLO response when the device is enabled.



ON = 5 V

Figure 9-2. UVLO Response

10 Power Supply Recommendations

The device is designed to operate from a VIN range of 1.5 V to 5.5 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. in most situations, using an input capacitance of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The ON pin cannot be left floating and must be driven either high or low for proper functionality.

Figure 11-1 shows an example of a layout.

11.2 Layout Example

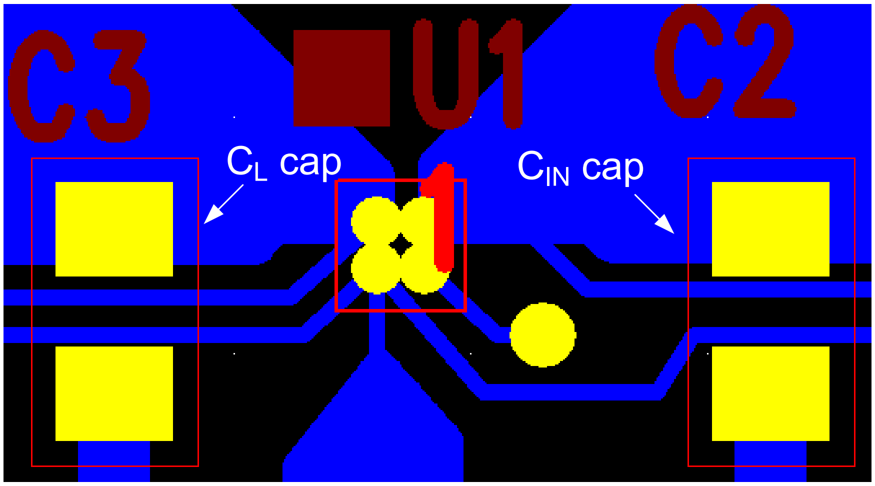


Figure 11-1. Layout Recommendation

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (1)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22930)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See *Thermal Information* table. This parameter is highly dependent upon board layout.

The power dissipated by the device depends on the R_{ON} of the device at a given V_{IN}. To calculate the amount of power being dissipated by the device, use the following equation:

$$P_{IR} = I^2 \times R_{ON} \quad (2)$$

where

- P_{IR} = power dissipated by the device
- I = load current in amperes
- R_{ON} = resistance of the device in Ohms at a given V_{IN} (see *Electrical Characteristics* table)

The result from Equation 2 should always be less than or equal to the result from Equation 1.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

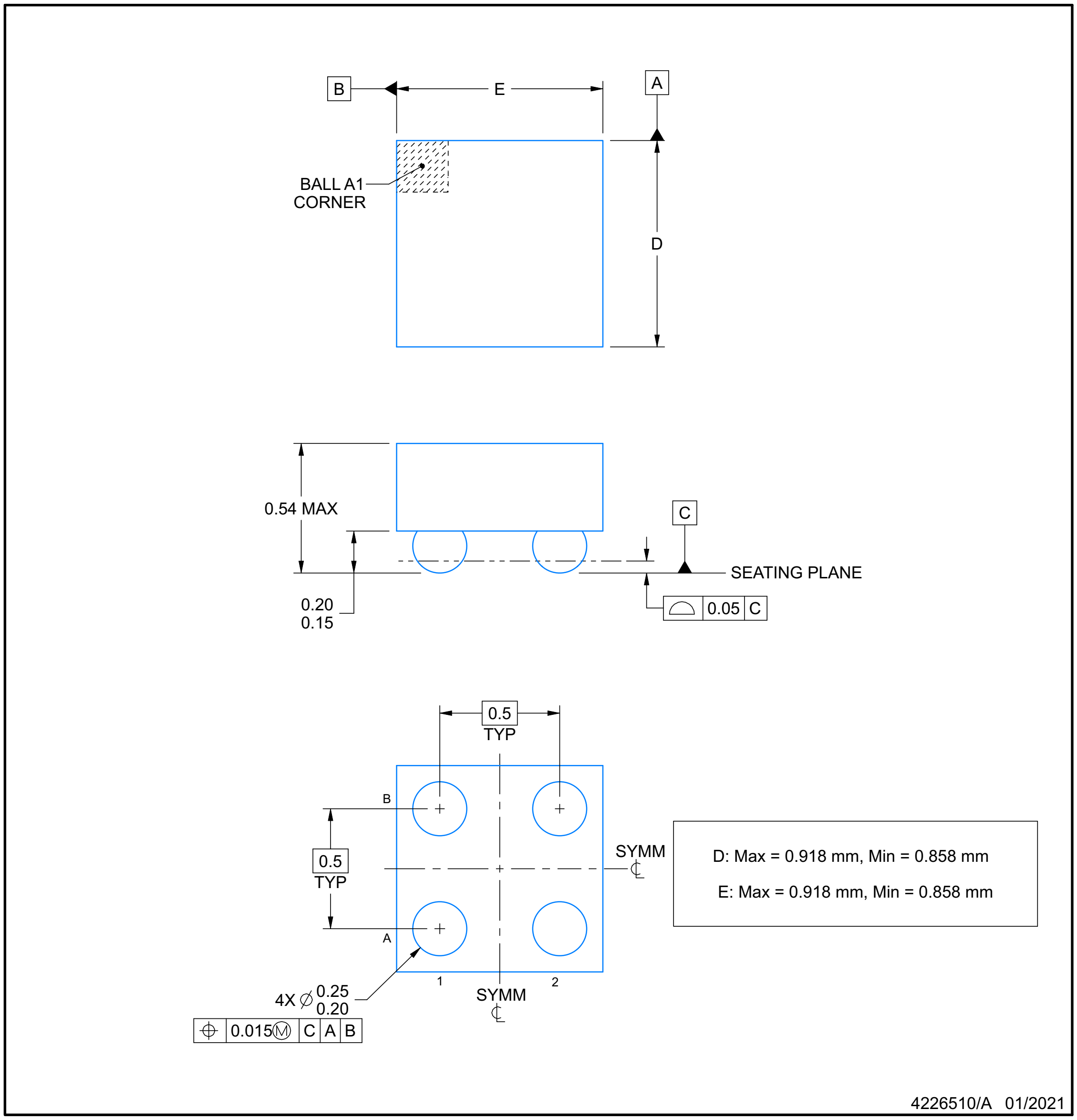
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YZV0004-C01

DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

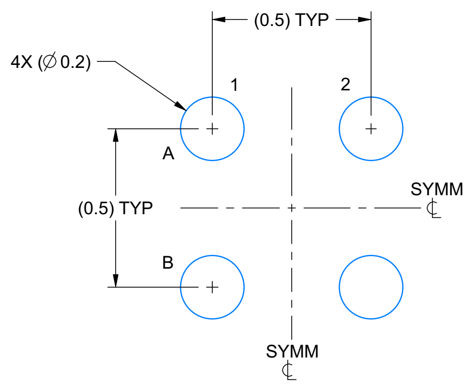
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

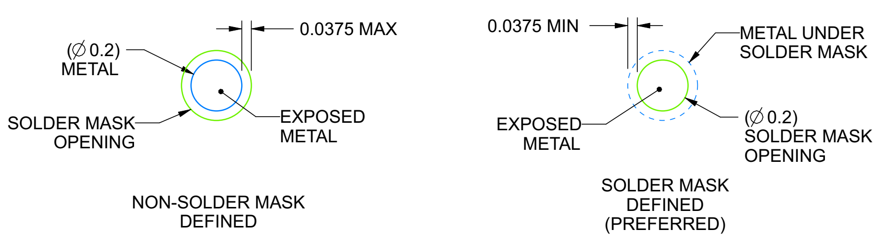
YZV0004-C01

DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226510/A 01/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

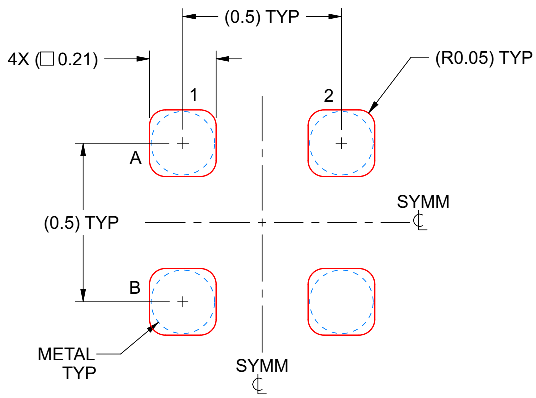
Texas Instruments
www.ti.com

EXAMPLE STENCIL DESIGN

YZV0004-C01

DSBGA - 0.54 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226510/A 01/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22930AYZVR	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q
TPS22930AYZVR.A	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q
TPS22930AYZVR.B	Active	Production	DSBGA (YZV) | 4	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q
TPS22930AYZVT	Active	Production	DSBGA (YZV) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q
TPS22930AYZVT.A	Active	Production	DSBGA (YZV) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q
TPS22930AYZVT.B	Active	Production	DSBGA (YZV) | 4	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	3Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

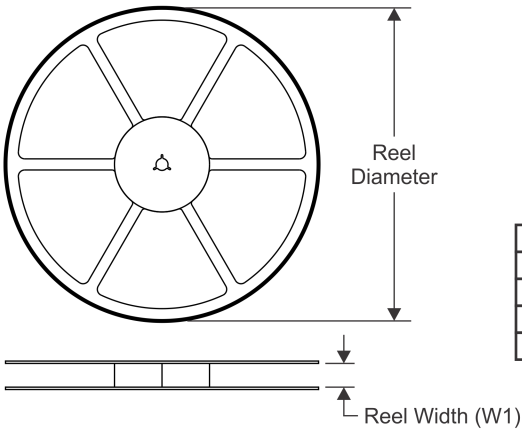
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

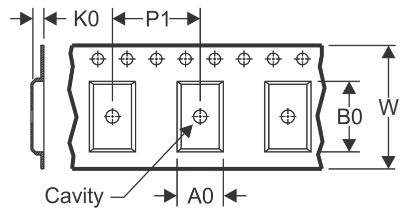
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

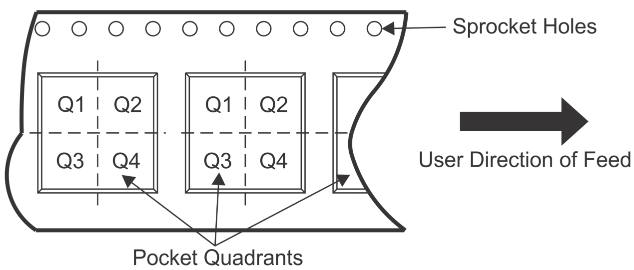


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

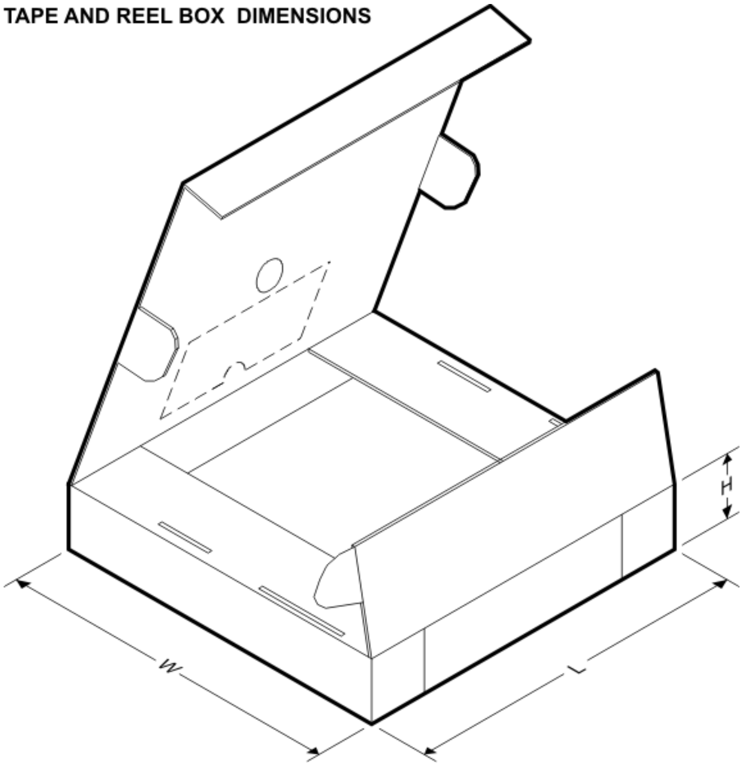
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22930AYZVR	DSBGA	YZV	4	3000	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1
TPS22930AYZVT	DSBGA	YZV	4	250	180.0	8.4	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22930AYZVR	DSBGA	YZV	4	3000	182.0	182.0	20.0
TPS22930AYZVT	DSBGA	YZV	4	250	182.0	182.0	20.0