TPS22965 5.7-V, 6-A, 16-mΩ On-Resistance Load Switch

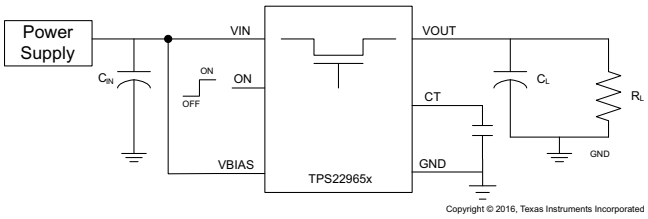
1 Features

- Integrated Single Channel Load Switch
- Input Voltage Range: 0.8 V to 5.7 V
- Ultra-Low On Resistance (R_{ON})
  - R_{ON} = 16 mΩ at VIN = 5 V (VBIAS = 5 V)
  - R_{ON} = 16 mΩ at VIN = 3.6 V (VBIAS = 5 V)
  - R_{ON} = 16 mΩ at VIN = 1.8 V (VBIAS = 5 V)
- 6-A Maximum Continuous Switch Current
- Low Quiescent Current (50 µA)
- Low Control Input Threshold Enables Use of 1.2-, 1.8-, 2.5-, and 3.3-V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD) (Optional)
- SON 8-pin Package With Thermal Pad
- ESD Performance Tested per JESD 22
  - 2000-V HBM and 1000-V CDM

2 Applications

- Ultrabook™
- Notebooks and Netbooks
- Tablet PC
- Consumer Electronics
- Set-top Boxes and Residential Gateways
- Telecom Systems
- Solid State Drives (SSDs)

Simplified Schematic



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3 Description

The TPS22965x is a single channel load switch that provides configurable rise time to minimize inrush current. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 5.7 V and can support a maximum continuous current of 6 A. The switch is controlled by an on and off input (ON), which is capable of interfacing directly with low-voltage control signals. In the TPS22965, a 225-Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The TPS22965x is available in a small, space-saving 2-mm × 2-mm 8-pin SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to +105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22965 TPS22965N	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

On-Resistance vs Input Voltage (V_{BIAS} = 5 V, I_{OUT} = –200 mA)

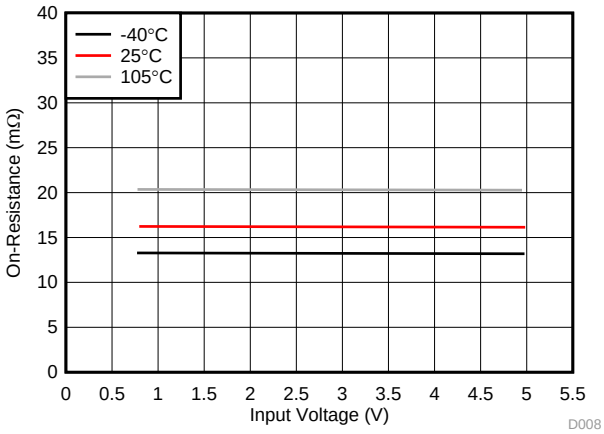

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Table of Contents

4 Revision History

Changes from Revision E (May 2016) to Revision F — **Page**

- Updated all *Typical Characteristics* Graphs ... 9

Changes from Revision D (March 2015) to Revision E — **Page**

- Changed QOD from "*TPS22965 Only*" to "*Optional*" in *Features* section ... 1

Changes from Revision C (February 2015) to Revision D — **Page**

- Added TPS22965N part number ... 1
- Updated Thermal Information table ... 6
- Updated typical AC timing parameters (tables, graphs and scope captures) ... 12

Changes from Revision B (June 2014) to Revision C — **Page**

- Extended Recommended Operating free-air temperature range maximum to 105°C. ... 1
- Added temperature operations to *Electrical Characteristics, V_{BIAS} = 5 V* ... 6
- Added temperature operations to *Electrical Characteristics, V_{BIAS} = 2.5 V* ... 7

Changes from Revision A (August 2013) to Revision B — **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed MAX value of "V_{IN}" from 5.5 V to 5.7 V. ... 5
- Changed MAX value of "V_{BIAS}" from 5.5 V to 5.7 V. ... 5
- Changed MAX value of "V_{ON}" from 5.5 V to 5.7 V ... 5

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- Added *Thermal Information* table 6

Changes from Original (August 2012) to Revision A **Page**

- Updated VON MAX value to fix typo that restricted operating range. Changed MAX value from "VIN" to "5.5" to align with rest of document. 5

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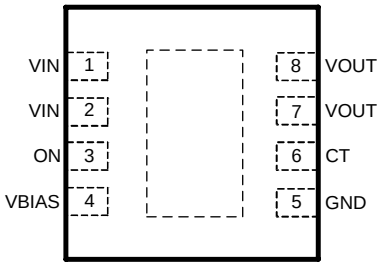
5 Device Comparison Table

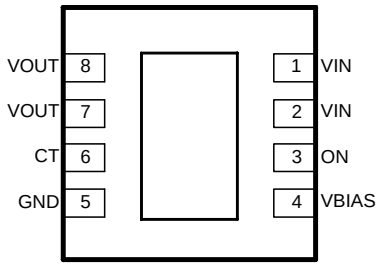
DEVICE	R_{ON} AT 3.3 V (TYP)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22965	16 mΩ	Yes	6 A	Active high
TPS22965N	16 mΩ	No	6 A	Active high

6 Pin Configuration and Functions

DSG PACKAGE
8-Pin WSON
Top View



DSG PACKAGE
8-Pin WSON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
No.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Adjustable Rise Time* section for more information
7	VOUT	O	Switch output
8			
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout Example* section for layout guidelines

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	On voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		6	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		8	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.7	V
V_{ON}	ON voltage		0	5.7	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	1.1	5.7	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	0	0.5	V
C_{IN}	Input capacitor		1(1)		µF
T_A	Operating free-air temperature(2)		–40	105	°C

(1) See the *Application Information* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the equation: $T_{A\ (max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

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7.4 Thermal Information

THERMAL METRIC[1]		TPS22965x DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	96.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specification in the following table applies where **V_{BIAS} = 5 V**. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{VBIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 5 V		–40°C to +105°C		50	75	µA
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +105°C		0.005	5	µA
			V_{IN} = 3.3 V	–40°C to +105°C		0.002	3	
			V_{IN} = 1.8 V	–40°C to +105°C		0.002	2	
			V_{IN} = 0.8 V	–40°C to +105°C		0.001	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5 V	V_{IN} = 5 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 3.3 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.8 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.5 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.2 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 0.8 V	25°C		16	21	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
R_{PD} [1]	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V, I_{OUT} = 15 mA		–40°C to +105°C		225	300	Ω

(1) TPS22965 only

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7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies where **V_{BIAS} = 2.5 V**. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_Q V_{VBIAS}	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		–40°C to +105°C		20	30	µA
I_{SD} V_{BIAS}	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		–40°C to +105°C			2	µA
I_{SD} V_{IN}	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +105°C		0.005	3	µA
			V_{IN} = 1.8 V	–40°C to +105°C		0.002	2	
			V_{IN} = 1.2 V	–40°C to +105°C		0.002	2	
			V_{IN} = 0.8 V	–40°C to +105°C		0.001	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		20	24	mΩ
				–40°C to +85°C			27	
				–40°C to +105°C			28	
			V_{IN} = 1.8 V	25°C		19	23	mΩ
				–40°C to +85°C			26	
				–40°C to +105°C			28	
			V_{IN} = 1.5 V	25°C		18	23	mΩ
				–40°C to +85°C			25	
				–40°C to +105°C			27	
			V_{IN} = 1.2 V	25°C	0	18	23	mΩ
				–40°C to +85°C			25	
				–40°C to +105°C			27	
			V_{IN} = 0.8 V	25°C		17	22	mΩ
				–40°C to +85°C			25	
				–40°C to +105°C			27	
R_{PD} (1)	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		–40°C to +105°C		275	325	Ω

(1) TPS22965 only

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7.7 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1600		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		9		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1985		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		3		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		660		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		730		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		100		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		380		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		8		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		560		
V_{IN} = 2.5 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2435		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		9		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2515		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		4		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1230		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1565		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		70		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		930		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		8		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1110		

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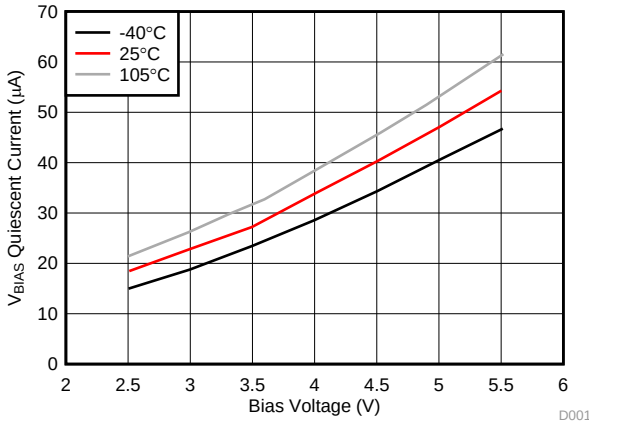
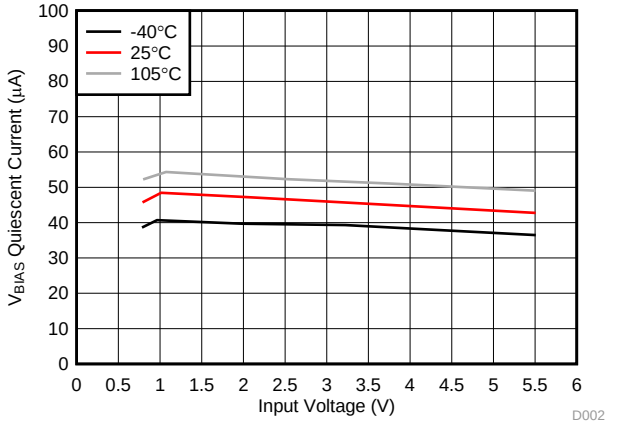
7.8 Typical DC Characteristics



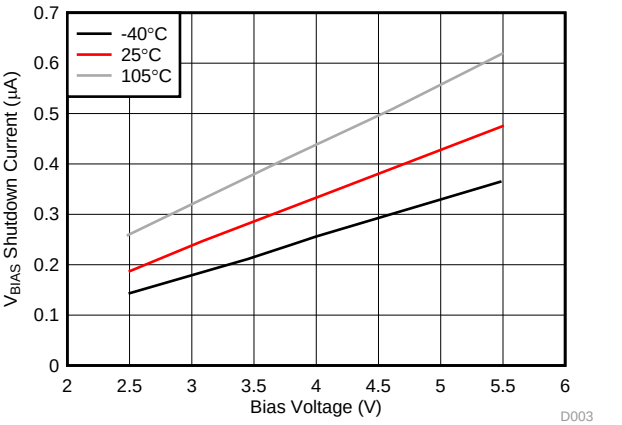
V_{IN} = 1.8 V V_{ON} = 5 V V_{OUT} = 0 V

Figure 1. V_{BIAS} Quiescent Current vs Bias Voltage



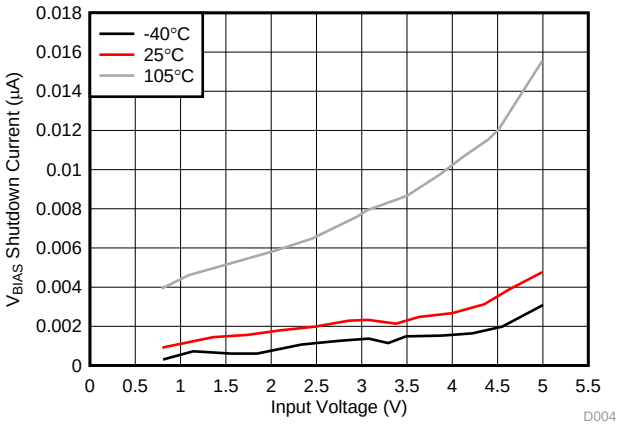
V_{BIAS} = 5 V V_{ON} = 5 V V_{OUT} = 0 V

Figure 2. V_{BIAS} Quiescent Current vs Input Voltage



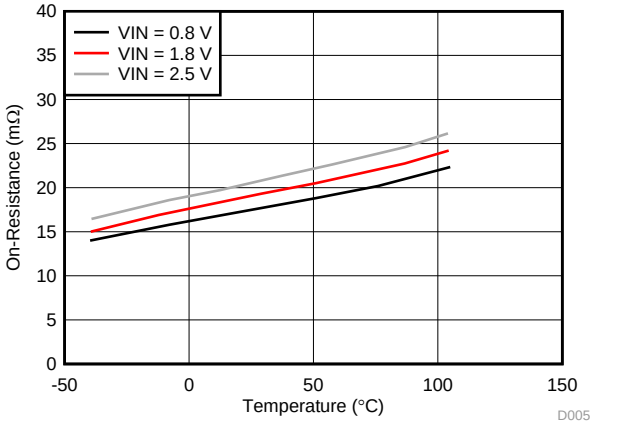
V_{IN} = 5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 3. V_{BIAS} Shutdown Current vs Bias Voltage



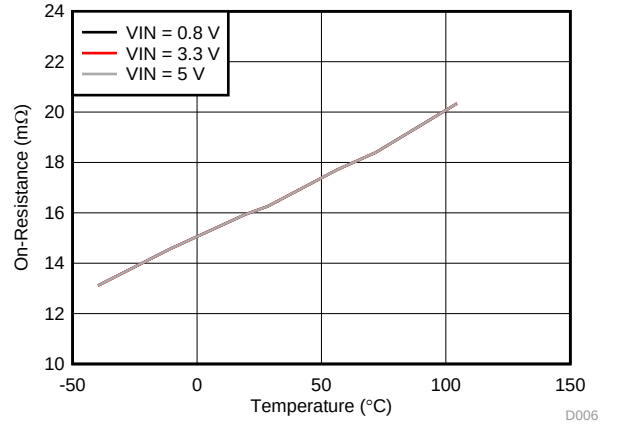
V_{BIAS} = 5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 4. V_{BIAS} Shutdown Current vs Input Voltage



V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 5. On-Resistance vs Ambient Temperature



V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

Figure 6. On-Resistance vs Ambient Temperature

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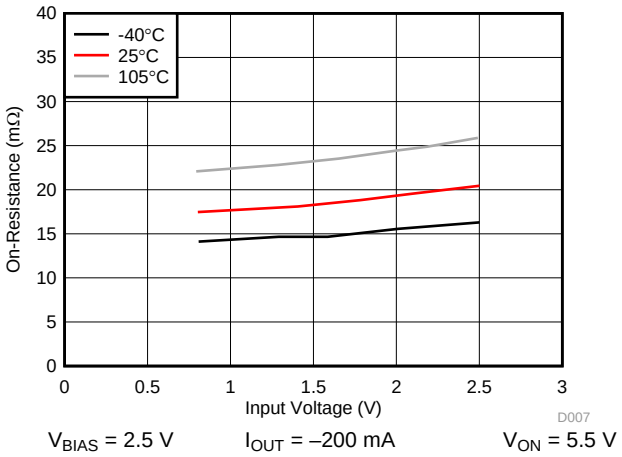
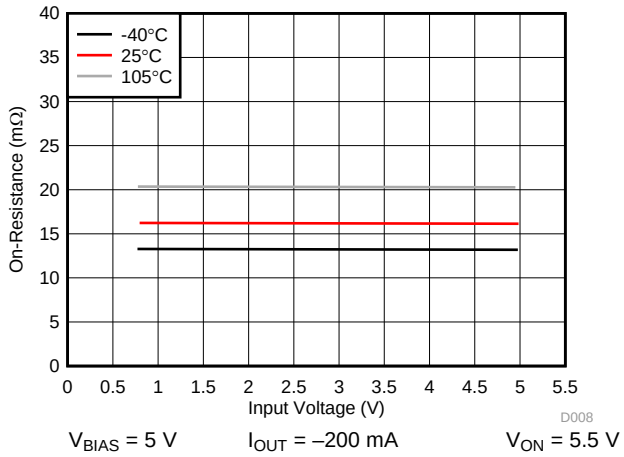
Typical DC Characteristics (continued)



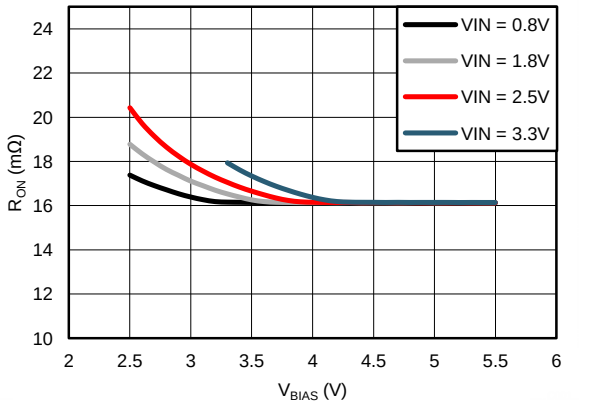
V_{BIAS} = 2.5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 7. On-Resistance vs Input Voltage



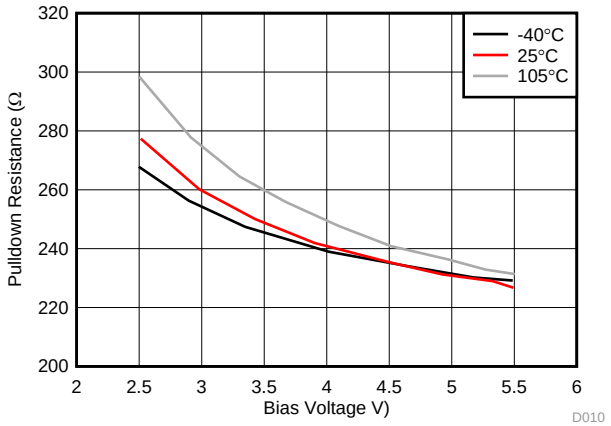
V_{BIAS} = 5 V I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 8. On-Resistance vs Input Voltage



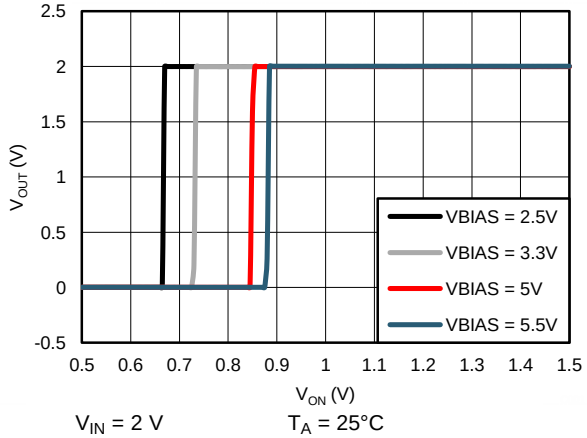
T_A = 25°C I_{OUT} = –200 mA V_{ON} = 5.5 V

Figure 9. On-Resistance vs Bias Voltage



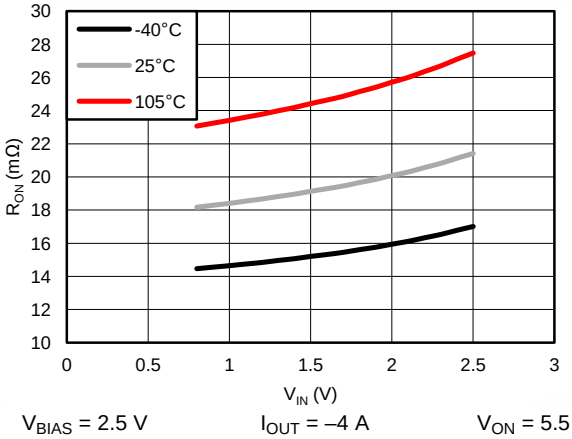
V_{IN} = 1.8 V V_{ON} = 0 V

Figure 10. Pulldown Resistance vs Bias Voltage



V_{IN} = 2 V T_A = 25°C

Figure 11. Output Voltage vs ON Voltage



V_{BIAS} = 2.5 V I_{OUT} = –4 A V_{ON} = 5.5 V

Figure 12. On-Resistance vs Input Voltage

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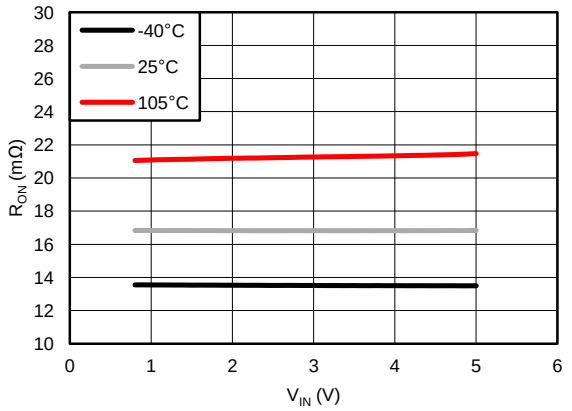
Typical DC Characteristics (continued)

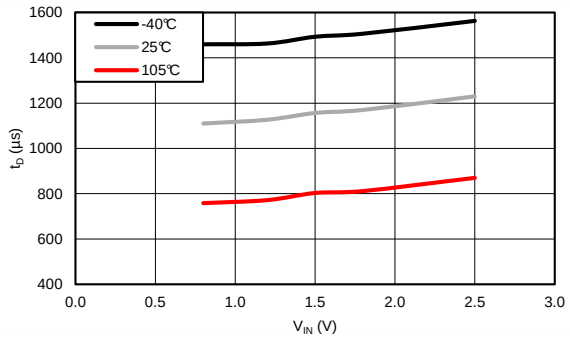


V_{BIAS} = 5 V I_{OUT} = –4 A V_{ON} = 5.5 V

Figure 13. On-Resistance vs Input Voltage

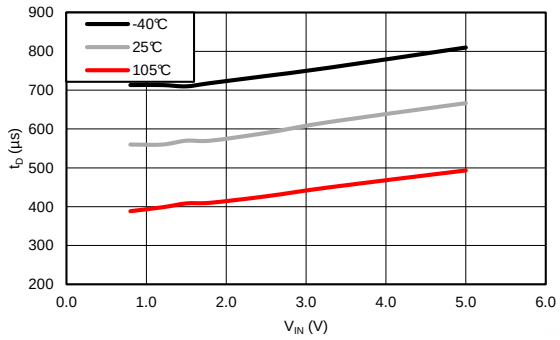
7.9 Typical Switching Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



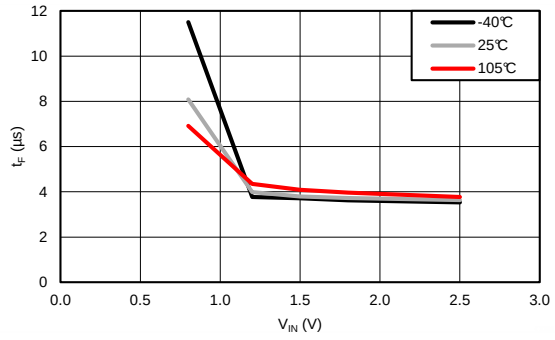
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 14. Delay Time vs Input Voltage



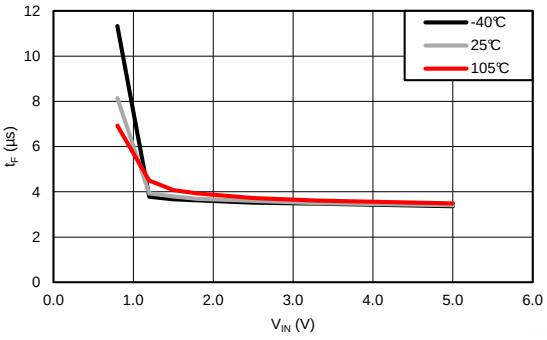
V_{BIAS} = 5 V CT = 1000 pF

Figure 15. Delay Time vs Input Voltage



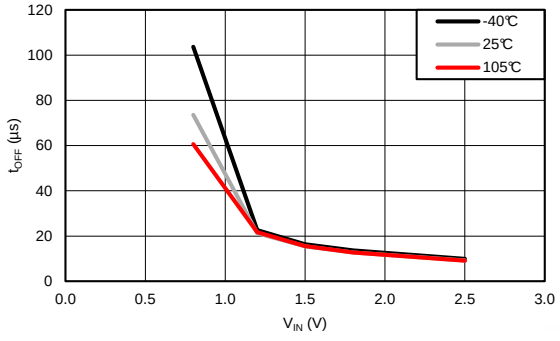
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 16. Fall Time vs Input Voltage



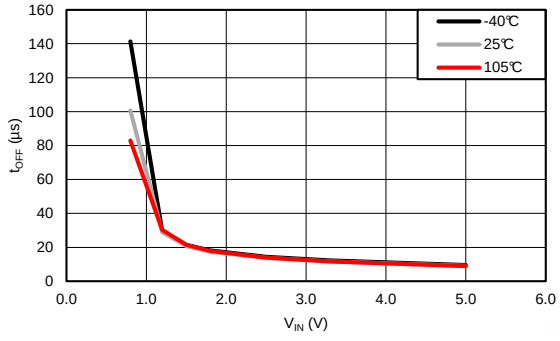
V_{BIAS} = 5 V CT = 1000 pF

Figure 17. Fall Time vs Input Voltage



V_{BIAS} = 2.5 V CT = 1000 pF

Figure 18. Turnoff Time vs Input Voltage



V_{BIAS} = 5 V CT = 1000 pF

Figure 19. Turnoff Time vs Input Voltage

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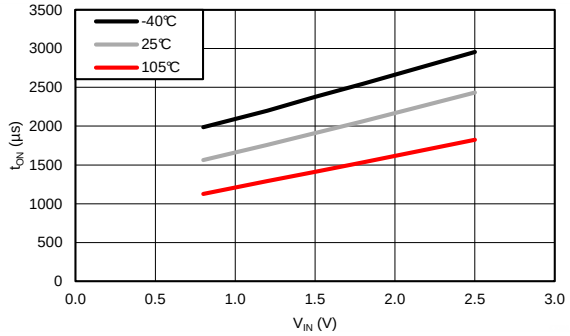
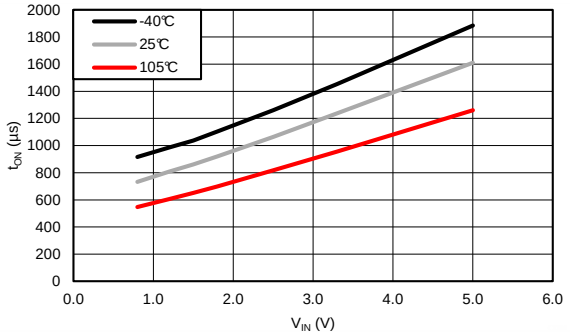
Typical Switching Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



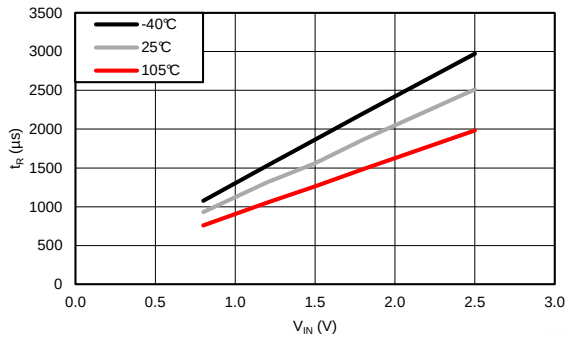
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 20. Turnon Time vs Input Voltage



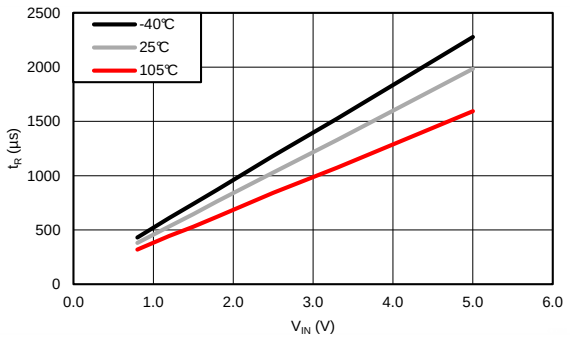
V_{BIAS} = 5 V CT = 1000 pF

Figure 21. Turnon Time vs Input Voltage



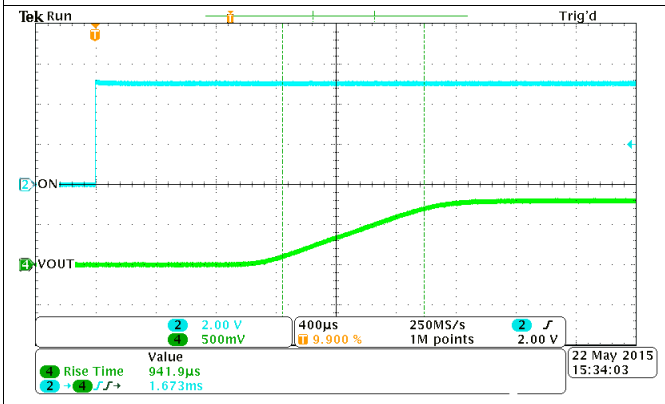
V_{BIAS} = 2.5 V CT = 1000 pF

Figure 22. Rise Time vs Input Voltage



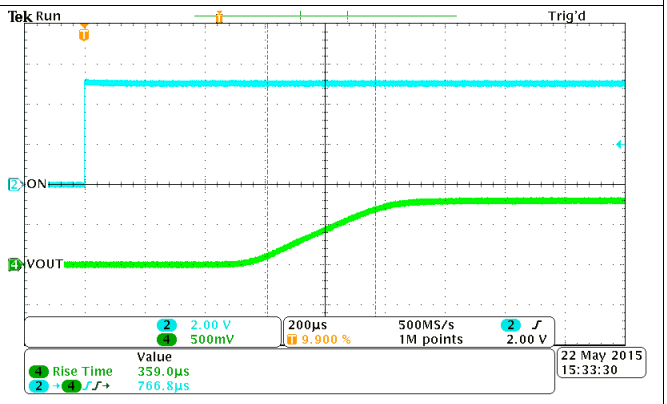
V_{BIAS} = 5 V CT = 1000 pF

Figure 23. Rise Time vs Input Voltage



V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 24. Turnon Response Time



V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 25. Turnon Response Time

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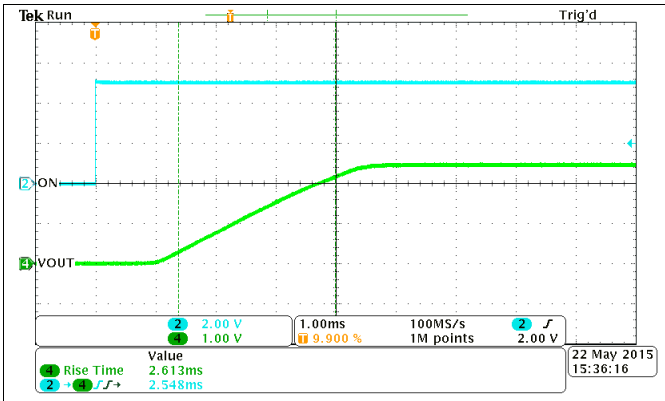
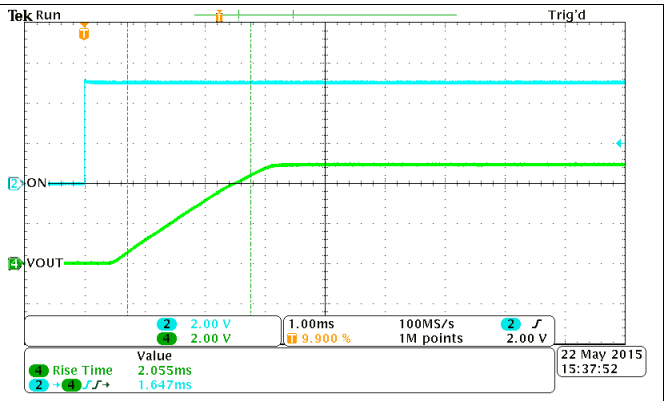
Typical Switching Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



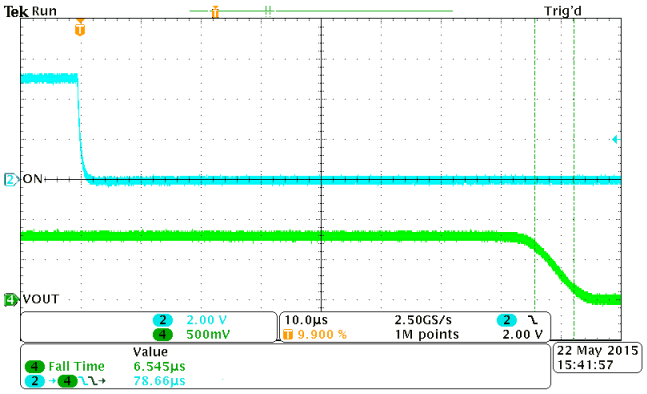
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF,
C_L = 0.1 µF R_L = 10 Ω

Figure 26. Turnon Response Time



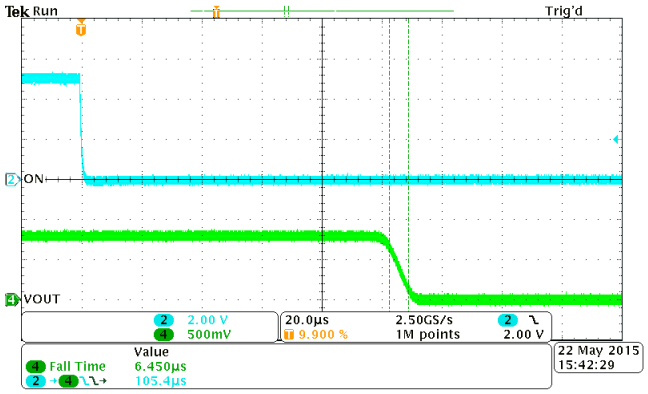
V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 27. Turnon Response Time



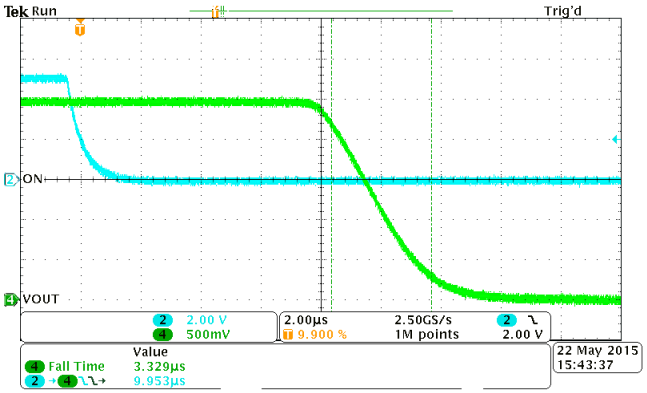
V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 28. Turnoff Response Time



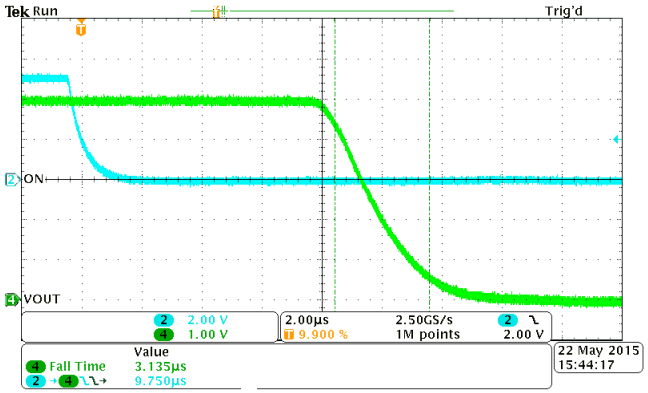
V_{IN} = 0.8 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 29. Turnoff Response Time



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 30. Turnoff Response Time



V_{IN} = 5 V V_{BIAS} = 5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω)

Figure 31. Turnoff Response Time

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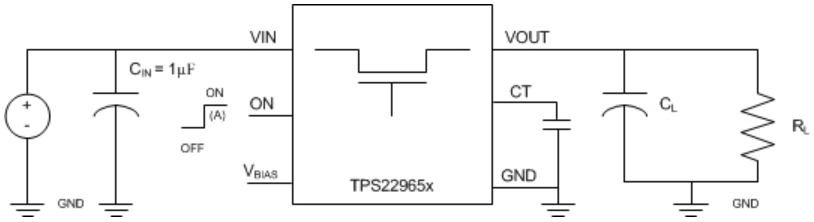
8 Parameter Measurement Information



A. Rise and fall times of the control signal is 100 ns.

Figure 32. Test Circuit

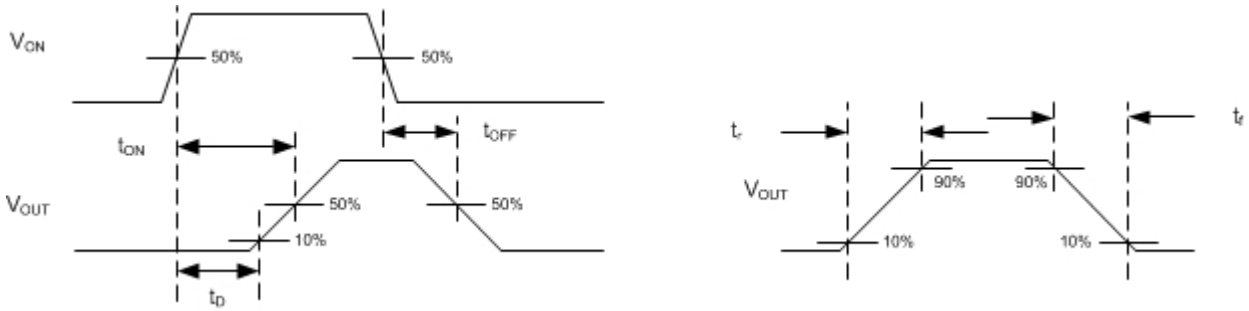


Figure 33. t_{ON} and t_{OFF} Waveforms

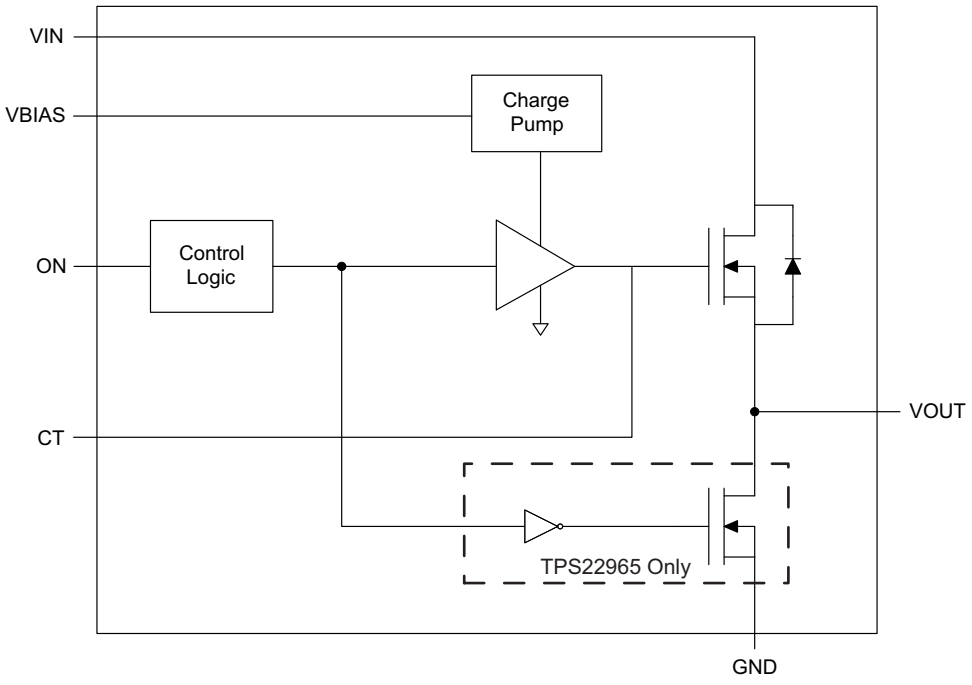
9 Detailed Description

9.1 Overview

The TPS22965x device is a single channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 12 V; therefore, the minimum voltage rating for the CT capacitor must be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0 pF. Use Table 1 to determine rise times for when CT = 0 pF.

$$SR = 0.38 \times CT + 34 \quad (1)$$

where

- SR is the slew rate (in µs/V)
- CT is the the capacitance value on the CT pin (in pF)
- The units for the constant 34 are µs/V. The units for the constant 0.38 are µs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown in Table 1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time vs CT Capacitor

CT (pF)	TYPICAL VALUES at 25°C with a 25 V X7R 10% CERAMIC CAPACITOR on CT(1)						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	180	136	94	84	74	70	60
220	547	378	232	202	173	157	129
470	962	654	386	333	282	252	206
1000	1983	1330	765	647	533	476	382
2200	4013	2693	1537	1310	1077	959	766
4700	8207	5490	3137	2693	2200	1970	1590
10000	17700	11767	6697	5683	4657	4151	3350

(1) Rise time (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V

9.3.2 Quick Output Discharge (QOD) (Optional)

The TPS22965 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

9.3.3 Low Power Consumption During Off State

The I_{SD} V_{IN} supply current is 0.01 µA typical at 1.8 VIN. Typically, the downstream loads must have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

9.4 Device Functional Modes

The Table 2 lists the VOUT pin states as determined by the ON pin.

Table 2. VOUT Connection

ON	TPS22965	TPS22965N
L	GND	Open
H	VIN	VIN

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 ON and OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.3 Output Capacitor (Optional)

Becuase of the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.1.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 5 V* table. See Figure 34 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

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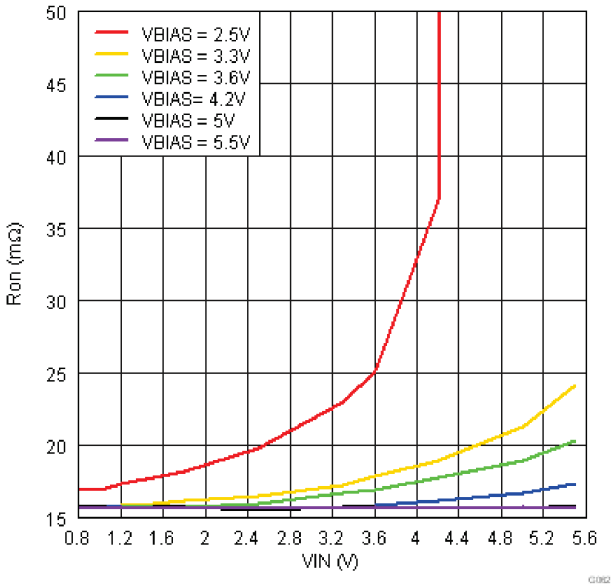
Application Information (continued)



T_A = 25 °C I_{OUT} = –200 mA

Figure 34. R_{ON} vs V_{IN}

10.2 Typical Application

This application demonstrates how the TPS22965x can be used to power downstream modules.

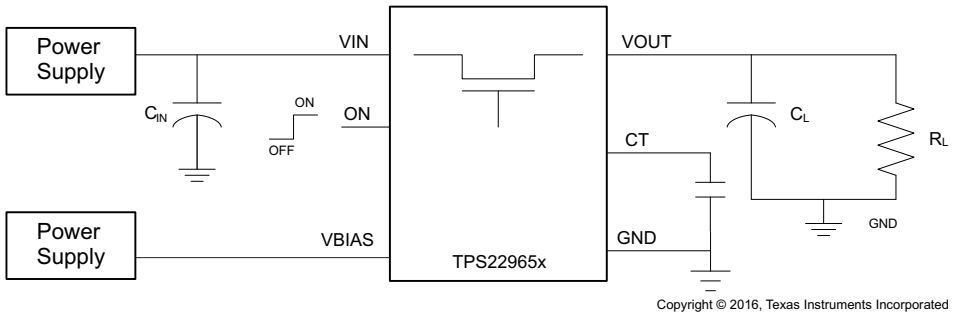


Figure 35. Powering a Downstream Module

10.2.1 Design Requirements

Table 3 shows the design parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2.

Inrush Current = C × dV/dt

where

- C is the output capacitance
- dV is the output voltage
- dt is the rise time (2)

The TPS22965x offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation. See Equation 3 and Equation 4.

400 mA = 22 µF × 3.3 V/dt (3)

dt = 181.5 µs (4)

To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.2.2 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 5 as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22965x)
- T_A is the ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout. (5)

See Figure 38, notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

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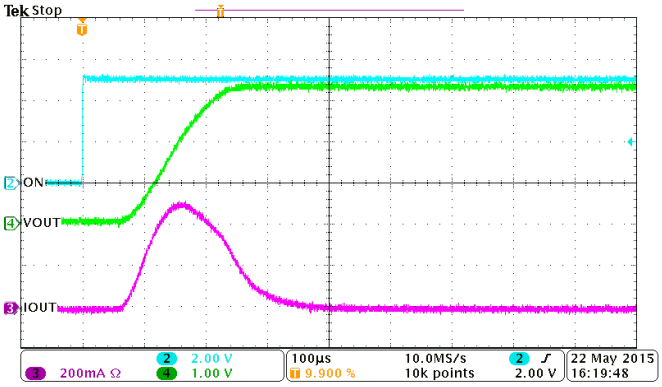
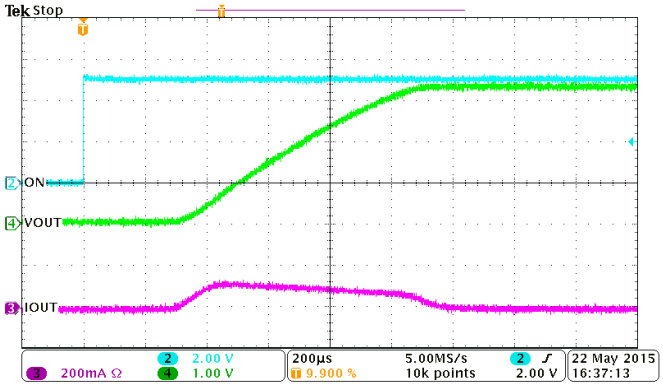
10.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 36. Inrush Current with CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 37. Inrush Current with CT = 220 pF

11 Power Supply Recommendations

The device is designed to operate from a VBIAS range of 2.5 V to 5.7 V and a VIN range of 0.8 V to VBIAS.

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12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to avoid parasitic capacitance.

12.2 Layout Example

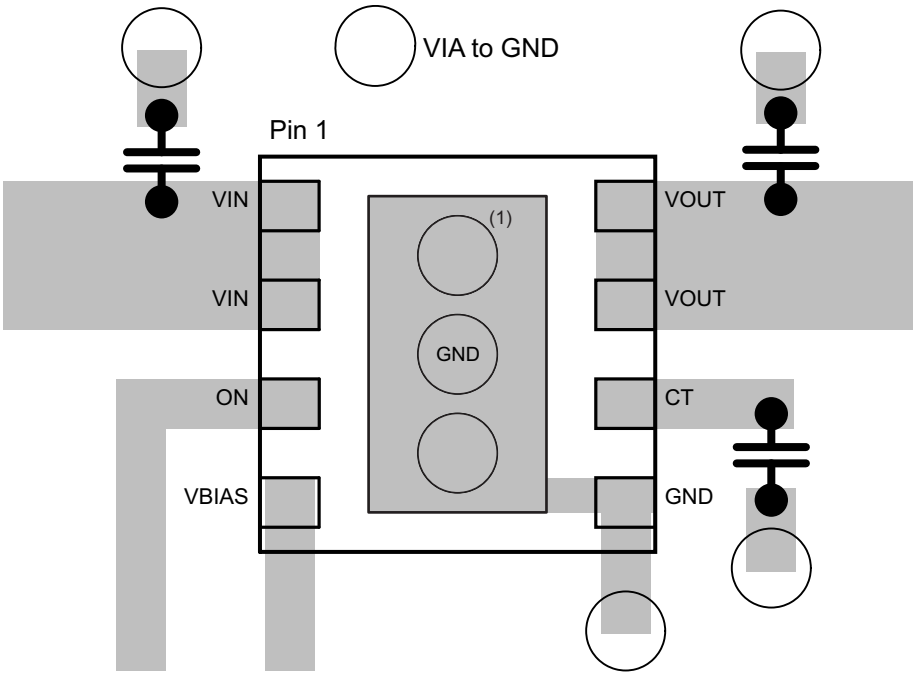

Figure 38. Layout Recommendation

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *Managing Inrush Current*
- *TPS22965EVM-023 Single 6A Load Switch*
- *Load Switch Thermal Considerations*
- *TPS22965NEVM User's Guide*
- *TPS22965WDSGQ1EVM User's Guide*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22965DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0	Samples
TPS22965DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0	Samples
TPS22965NDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS22965 :

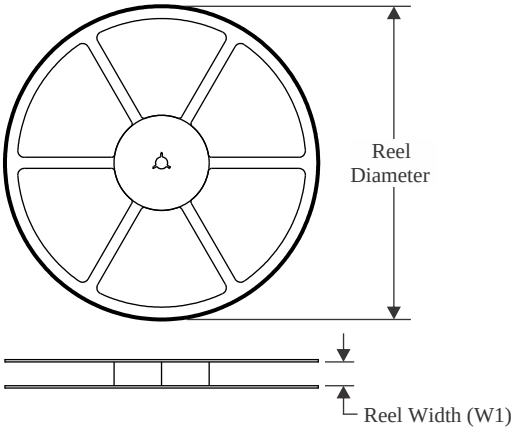
- Automotive : TPS22965-Q1

NOTE: Qualified Version Definitions:

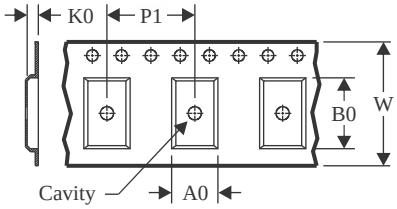
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

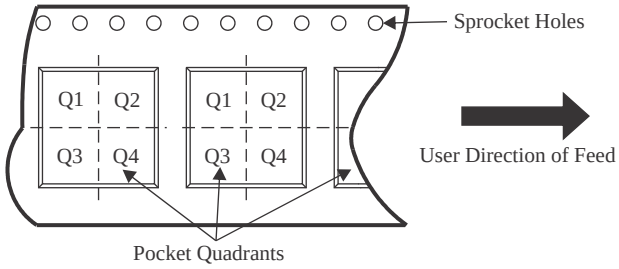


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

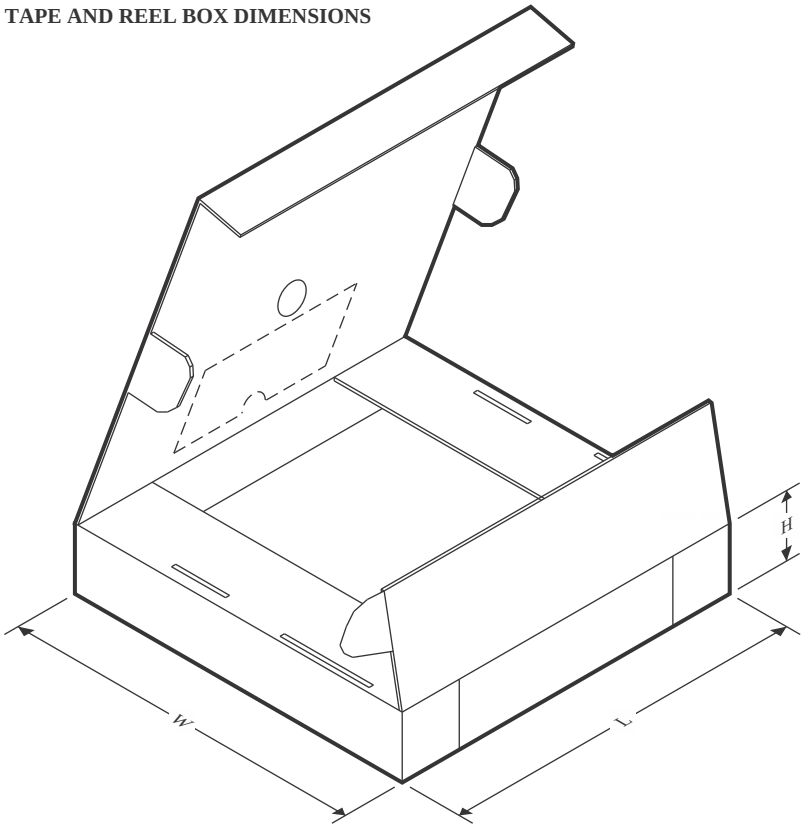
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22965DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22965NDSGR	WSON	DSG	8	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

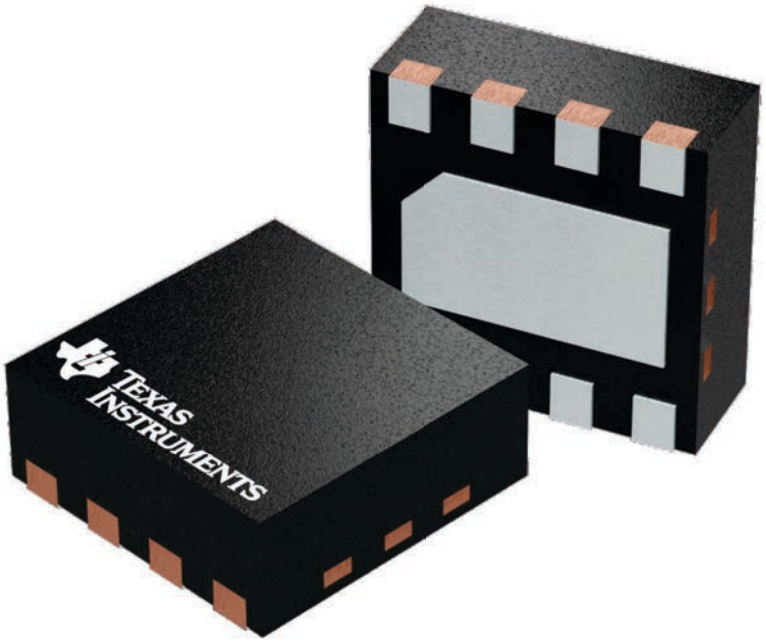
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



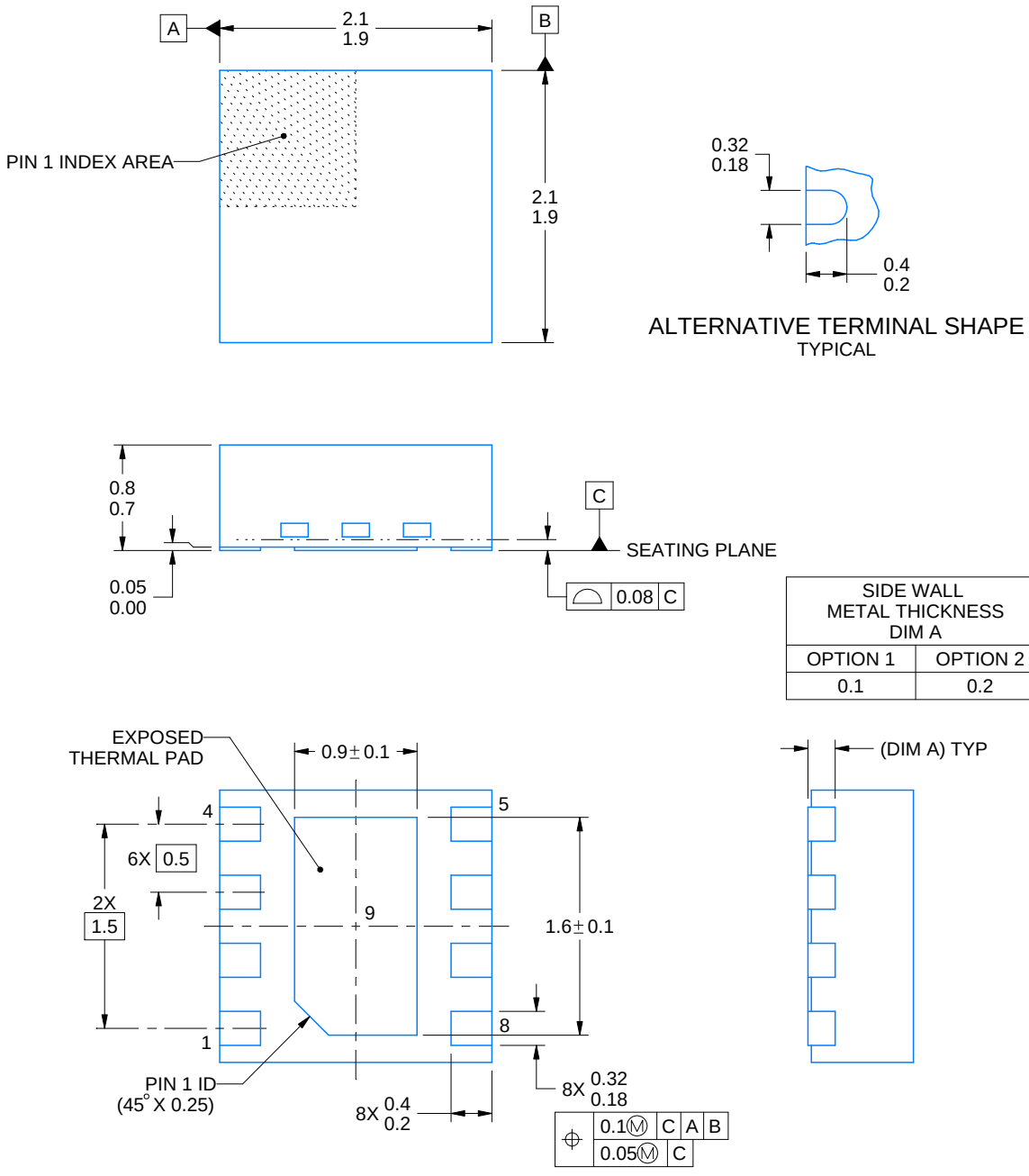
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

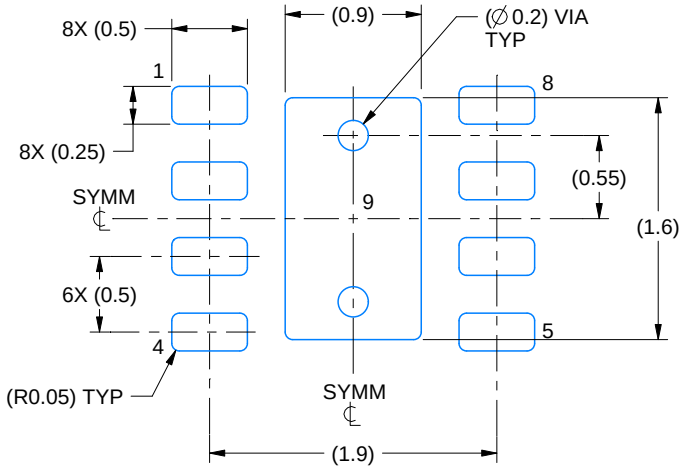
PLASTIC SMALL OUTLINE - NO LEAD



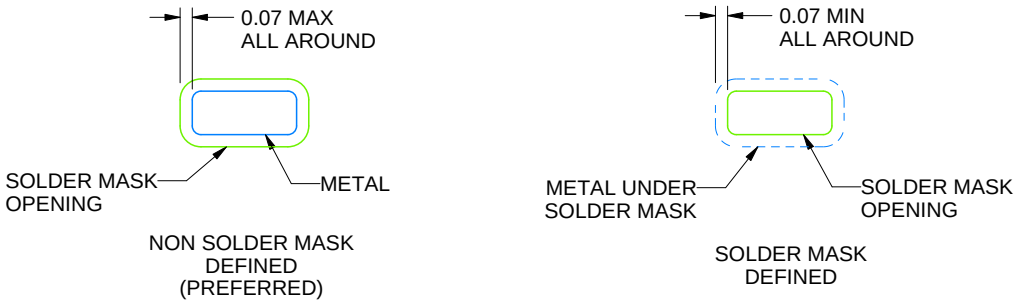
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

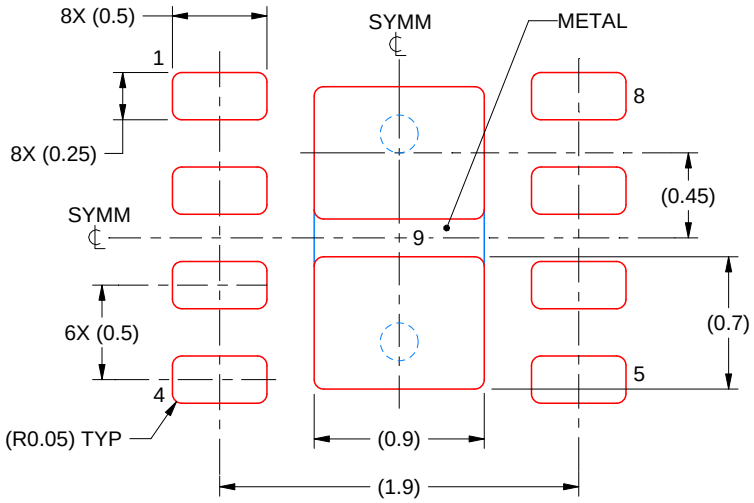


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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