TPS54334 4.2-V to 28-V Input Voltage, 3-A Output Current Synchronous Step-Down Voltage Converter

1 Features

- Two 128mΩ/84mΩ MOSFETs for 3A Continuous Output Current
- Power Good
- Low 2 µA Shutdown Quiescent Current
- 0.8 V Internal Voltage Reference with ±1.5% Accuracy Over Temperature
- Fixed-Frequency Current Mode Control
- Pulse Skipping Boosts Efficiency at Light Loads
- Overcurrent Protection for Both MOSFETs with Hiccup Mode for Severe Fault Conditions
- Thermal and Overvoltage Transient Protection
- Available in Easy-to-Use 8-Pin SOIC PowerPAD™ and 10-Pin SON
- Monotonic Start-Up into Pre-biased Outputs

2 Applications

- Consumer Applications such as a Digital TV (DTV), Set Top Box (STB, DVD/Blu-ray Player), LCD Display, CPE (Cable Modem, WiFi Router), DLP Projectors, Smart Meters
- Battery Chargers
- Industrial and Car Audio Power Supplies
- 5V,12 and 24V Distributed Power Bus Supply

3 Description

The TPS54334 is a 28-V, 3-A, low quiescent supply current (I_Q), synchronous monolithic buck converter with integrated MOSFETs.

The TPS54334 enables small designs by integrating the MOSFETs and implementing current mode control to reduce external component count.

Efficiency is maximized through the integrated 128mΩ/84mΩ MOSFETs, low quiescent supply current and pulse skipping at light loads. Using the enable pin, shutdown supply current is reduced to 2 µA by entering a shutdown mode.

The TPS54334 provides accurate regulation for a variety of loads with an accurate 1.5% voltage reference over temperature.

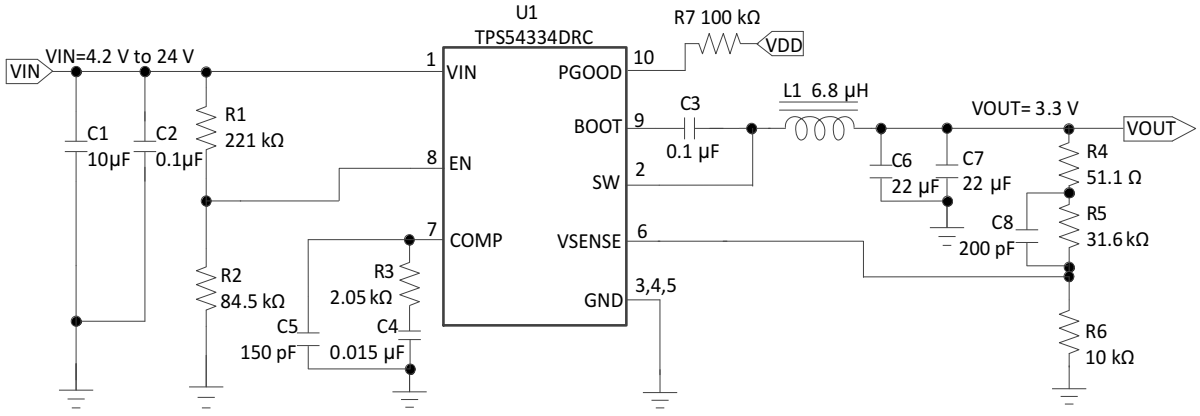
Cycle by cycle current limiting on the high-side fet protects the TPS54334 in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Hiccup protection will be triggered if the overcurrent condition has persisted for longer than the preset time. Thermal hiccup protection disables the part when die temperature exceeds thermal shutdown temperature and enables the part again after the built-in thermal hiccup time.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54334	SO (8 Pin)	4.89 mm × 3.90 mm
	VSON (10 Pin)	3.0 mm × 3.0 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

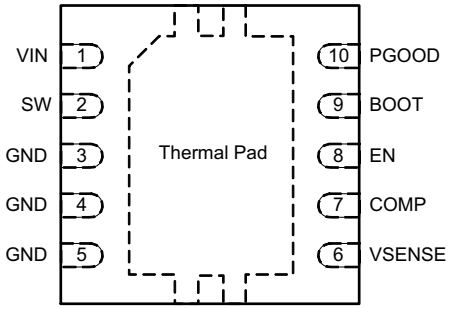
DATE	REVISION	NOTES
May 2015	*	Initial release.

Changes from Original (May 2015) to Revision A **Page**

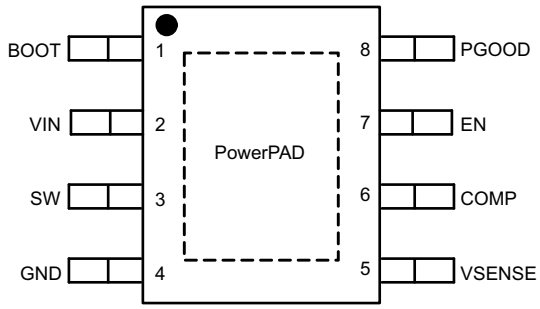
- Deleted SWIFT™ from the data sheet title ... 1

5 Pin Configuration and Functions

DRC Package
10 Pin VSON
Top View



DDA Package
8 Pin SO
Top View



Pin Functions

PIN NAME	NUMBER		I/O	DESCRIPTION
	DDA	DRC		
BOOT	1	9	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is refreshed.
COMP	6	7	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	7	8	I	Enable pin. Float to enable.
GND	4	3, 4, 5	–	Ground.
PGOOD	8	10	O	PGOOD open drain output. Connect a pull-up resistor with a value of 100kΩ to this pin.
SW	3	2	O	The source of the internal high side power MOSFET.
Vin	2	1	–	Input supply voltage, 4.2 V to 28 V.
VSENSE	5	6	I	Inverting node of the gm error amplifier.
PowerPad (SO only)			–	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.
Thermal pad (VSON only)				

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	30	V
	EN	–0.3	6	V
	BOOT	–0.3	(SW+7.5)	V
	VSENSE	–0.3	3	V
	COMP	–0.3	3	V
	PGOOD	–0.3	6	V
Output Voltage	BOOT-SW	0	7.5	V
	SW	–1	30	V
	SW 10ns Transient	–3.5	30	V
Vdiff(GND to Exposed Thermal Pad)		–0.2	0.2	V
Source Current	EN		100	µA
	SW	Current Limit		A
Sink Current	SW	Current Limit		A
	COMP	200	200	µA
	PGOOD	–0.1	5	mA
Operating Junction Temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{SS}	Supply input voltage	4.2	28	V
V_{OUT}	Output voltage	0.8	24	V
I_{OUT}	Output current	0	3	A
T_J	Operating junction temperature(1)	–40	150	°C

(1) The device must operate within 150°C to ensure continuous function and operation of the device.

6.4 Thermal Information

THERMAL METRIC(1)		TPS54334		UNIT
		DDA (8 PINS)	DRC (10 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.1	43.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.9	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	18.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.5	19.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it. T_J = –40°C to 150°C, VIN =4.2 to 28V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND UVLO (VIN PIN)					
Operating input voltage		4.2		28	V
Input UVLO threshold	Rising Vin		3.9	4.2	V
Input UVLO hysteresis			180	400	mV
VIN Shutdown Supply Current	EN = 0V		2	10	µA
VIN Operating– non switching supply current	VSENSE=810mV		310	800	µA
ENABLE (EN PIN)					
Enable threshold	Rising		1.21	1.28	V
Enable threshold	Falling	1.1	1.17		V
Input current	EN=1.1V		1.15		µA
Hysteresis current	EN=1.3V		3.3		µA
VOLTAGE REFERENCE					
Reference	T_J = 25°C	0.792	0.8	0.808	V
		0.788	0.8	0.812	V
MOSFET					
High side switch resistance(1)	BOOT-SW = 3V		160	290	mΩ
	BOOT-SW = 6V		128	240	mΩ
Low side switch resistance(1)			84	170	mΩ
ERROR AMPLIFIER					
Error amplifier transconductance (gm)	–2 µA < ICOMP < 2 µA V(COMP)=1V		1300		µmhos
Error amplifier source/sink	V(COMP)=1V, 100 mV Overdrive		100		µA
Start switching peak current threshold			0.5		A
COMP to Iswitch gm			8		A/V
CURRENT LIMIT					
High side switch current limit threshold		4	5.2	6.5	A
Low side switch sourcing current limit		3.5	4.7	6.1	A
Low side switch sinking current limit			0		A
Hiccup wait time			512		Cycles
Hiccup time before re-start			16384		Cycles

(1) Measured at pins.

Electrical Characteristics (continued)

The Electrical Ratings specified in this section will apply to all specifications in this document unless otherwise noted. These specifications will be interpreted as conditions that will not degrade the device's parametric or functional specifications for the life of the product containing it. T_J = –40°C to 150°C, VIN =4.2 to 28V, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown			165		°C
Thermal shutdown hysterisis			10		°C
Thermal shutdown hiccup time			32768		Cycles
SW (SW PIN)					
Minimum on time	Measured at 90% to 90% of VIN, I_{SW} = 2A		94	145	ns
Minimum off time	BOOT-SW ≥ 3V		0%		
BOOT (BOOT PIN)					
BOOT-SW UVLO			2.2	3	V
SLOW START					
Internal slow start time			2		ms
SWITCHING FREQUENCY					
Internal switching frequency		456	570	684	kHz
POWER GOOD (PGOOD PIN)					
VSENSE falling (Fault)			84		% Vref
VSENSE rising (Good)			90		% Vref
VSENSE rising (Fault)			116		% Vref
VSENSE falling (Good)			110		% Vref
Output high leakage	VSENSE = Vref, V(PGOOD) = 5.5 V		30	500	nA
Output low	I(PGOOD) = 0.35 mA			0.3	V
Minimum VIN for valid output(2)	V(PGOOD) < 0.5V at 100 µA		0.6	1	V
MAXIMUM OUTPUT VOLTAGE UNDER MINIMUM VIN(2)					
Maximum output voltage	VIN = 4.2V, Iout = 3A		2.9		V
	VIN = 4.2V, Iout = 2.5A		3.2		
	VIN = 4.2V, Iout = 2A		3.4		
	VIN = 4.2V, Iout = 1.5A		3.5		

(2) Not tested for mass production.

6.6 Typical Characteristics

VIN = 12 V, unless otherwise specified.

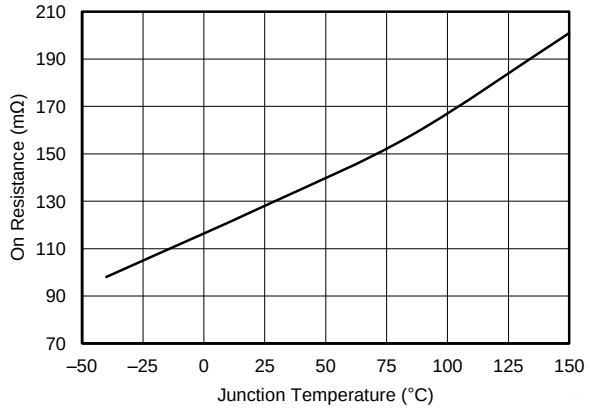


Figure 1. High-Side Resistance vs Junction Temperature

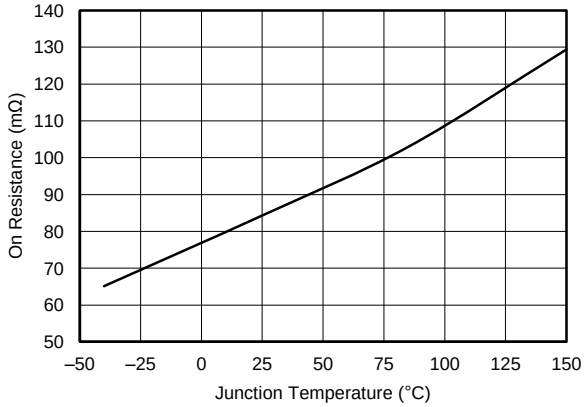


Figure 2. Low-Side Resistance vs Junction Temperature

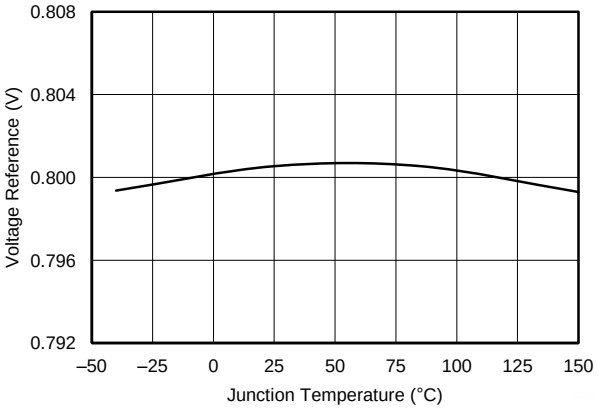


Figure 3. Reference Voltage vs Junction Temperature

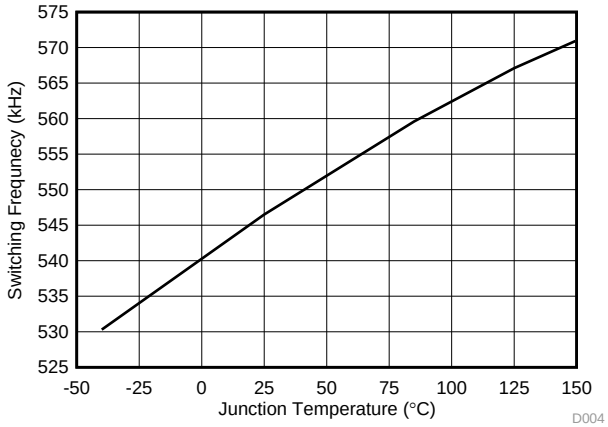


Figure 4. Switching Frequency vs Junction Temperature

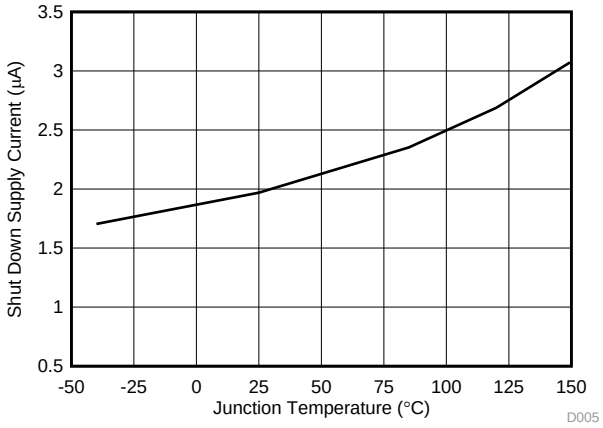


Figure 5. Shutdown Current vs Junction Temperature

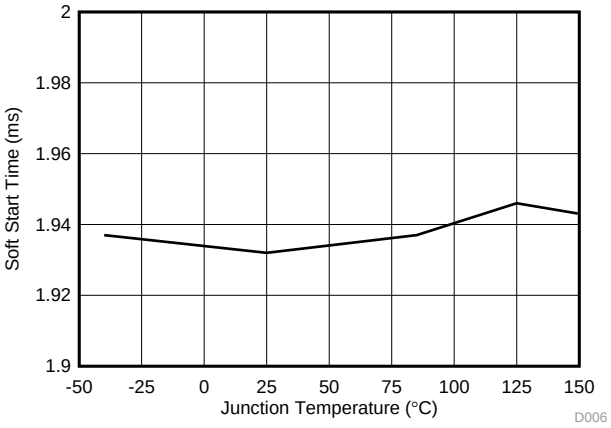


Figure 6. Softstart Time vs Junction Temperature

Typical Characteristics (continued)

VIN = 12 V, unless otherwise specified.

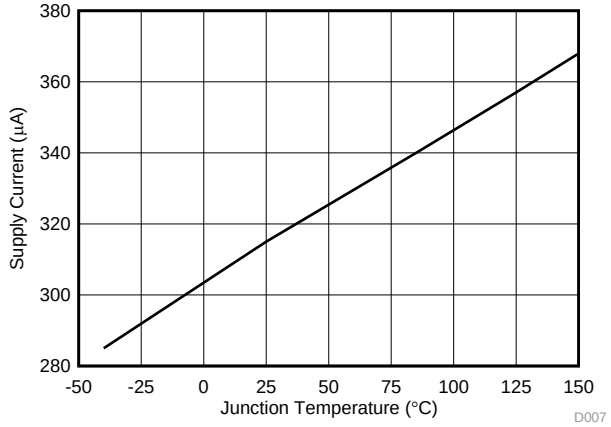


Figure 7. Non-Switching Operating Quiescent Current vs Junction Temperature

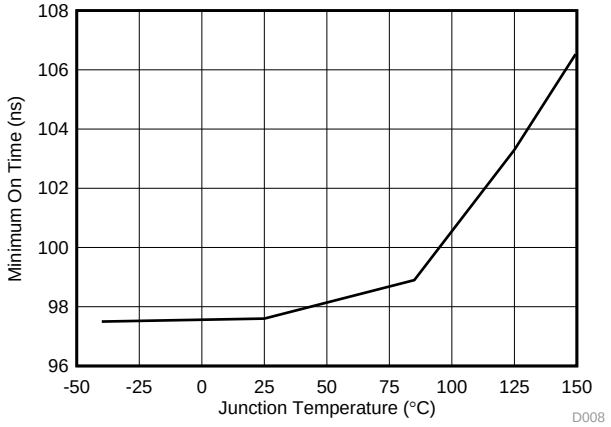


Figure 8. Minimum On Time vs Junction Temperature

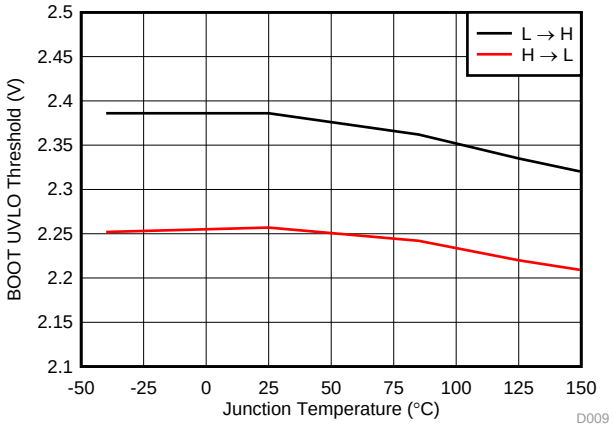


Figure 9. BOOT-SW UVLO Threshold vs Junction Temperature

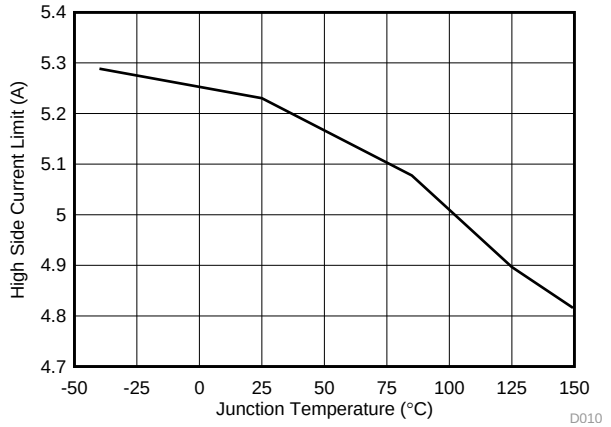


Figure 10. High-Side Current Limit Threshold vs Junction Temperature

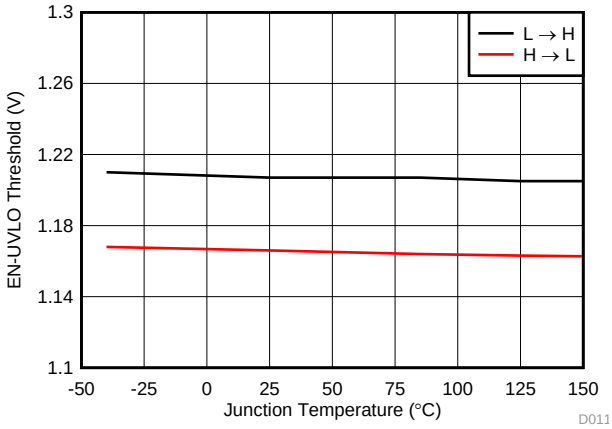


Figure 11. EN Threshold vs Junction Temperature

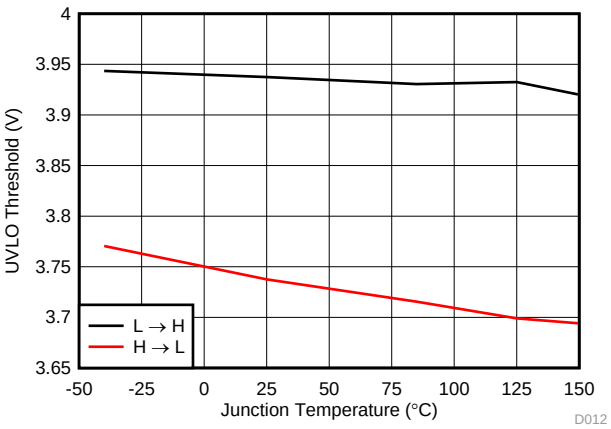


Figure 12. VIN UVLO Threshold vs Junction Temperature

7 Detailed Description

7.1 Overview

The device is a 28-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design.

The device is designed for safe monotonic startup into pre-biased loads. It has a typical default start up voltage of 3.9 V. The EN pin has an internal pull-up current source that can provide a default condition when the EN pin is floating for the device to operate. The total operating current for the device is typically 310µA when not switching and under no load. When the device is disabled, the supply current is less than 5µA.

The integrated 128mΩ/84mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 3 amperes.

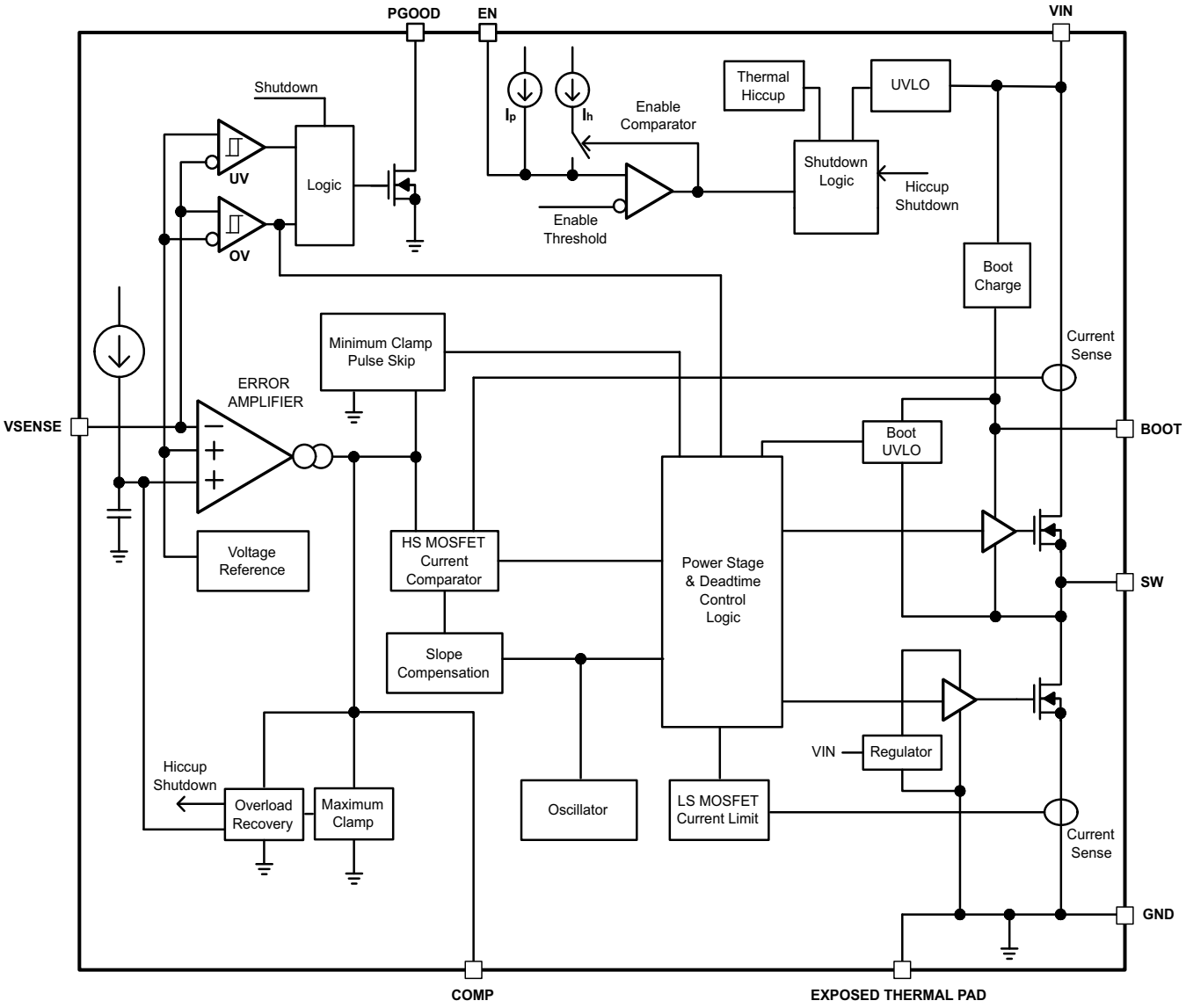
The device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and SW pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. The output voltage can be stepped down to as low as the 0.8 V reference.

The device has a power good comparator (PGOOD) with hysteresis which monitors the output voltage through the VSENSE pin. The PGOOD pin is an open drain MOSFET which is pulled low when the VSENSE pin voltage is less than 84% or greater than 116% of the reference voltage Vref and asserts high when the VSENSE pin voltage is 90% to 110% of the Vref.

The device minimizes excessive output over-voltage transients by taking advantage of the over-voltage power good comparator. When the regulated output voltage is greater than 116% of the nominal voltage, the over-voltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 110%.

The TPS54334 operating frequency is fixed at 570 kHz and at 2 ms slow start time.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The device uses a fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the COMP voltage level the high side power switch is turned off and the low side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

7.3.2 Light Load Operation

The device monitors the peak switch current of the high-side MOSFET. Once the peak switch current is lower than typically 0.5A, the device stops switching to boost the efficiency until the peak switch current is again higher than typically 0.5A.

Feature Description (continued)

7.3.3 Slope Compensation and Output Current

The device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

7.3.4 Bootstrap Voltage (BOOT) and Low Dropout Operation

The device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and SW pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

When the voltage between BOOT and SW pins drops below the BOOT-SW UVLO threshold, which is 2.2 V (typical), the high-side MOSFET turns off and the low-side MOSFET turns on, allowing the boot capacitor to recharge.

The device may work at 100% duty ratio as long as the BOOT-SW voltage is higher than the BOOT-SW UVLO threshold; but, do not operate the device at 100% duty ratio with no load.

7.3.5 Error Amplifier

The device has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the internal slow start voltage or the internal 0.8 V voltage reference. The transconductance of the error amplifier is 1300µA/V typically. The frequency compensation components are placed between the COMP pin and ground.

7.3.6 Voltage Reference

The voltage reference system produces a precise ±1.5% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

7.3.7 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 10 kΩ for the R1 resistor and use the Equation 1 to calculate R2. To improve efficiency at light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (1)$$

7.3.8 Enable and Undervoltage Lockout

The EN pin provides electrical on/off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the low-quiescent (I_Q) state.

The EN pin has an internal pull-up current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 180mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 13. When using the external UVLO function it is recommended to set the hysteresis to be greater than 500mV.

The EN pin has a small pull-up current Ip which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function since it increases by I_h once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 2, and Equation 3.

Feature Description (continued)

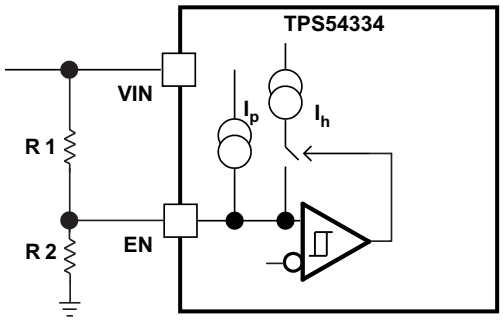


Figure 13. Adjustable VIN Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENfalling}}{V_{ENrising}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R1(I_p + I_h)} \quad (3)$$

where

- I_P = 1.15 µA
- I_H = 3.3 µA
- $V_{ENfalling}$ = 1.17 V
- $V_{ENrising}$ = 1.21 V

7.3.9 Slow Start

The internal 2-ms soft-start time is implemented to minimize inrush currents. If during normal operation, the VIN goes below the UVLO, EN pin pulled below 1.21 V, or a thermal shutdown event occurs, the device stops switching and the internal slow start voltage is discharged to 0 volts before reinitiating a powering up sequence.

7.3.10 Safe Start-up into Pre-Biased Outputs

The device is designed to prevent the low-side MOSFET from discharging a pre-biased output. During monotonic pre-biased startup, both high-side and low-side MOSFETs are not allowed to be turned on until the internal soft-start voltage is higher than VSENSE pin voltage.

7.3.11 Power Good (PGOOD)

The PGOOD pin is an open drain output. Once the VSENSE pin is between 90% and 110% of the internal voltage reference the PGOOD pin pull-down is de-asserted and the pin floats. It is recommended to use a pull up resistor between the values of 10kΩ and 100kΩ to a voltage source that is 5.5V or less. The PGOOD is in a defined state once the VIN input voltage is greater than 1V but with reduced current sinking capability. The PGOOD achieves full current sinking capability once the VIN input voltage is above 4.2V.

The PGOOD pin is pulled low when VSENSE is lower than 84% or greater than 116% of the nominal internal reference voltage. Also, the PGOOD is pulled low, if the input UVLO or thermal shutdown is asserted, the EN pin is pulled low.

7.4 Device Functional Modes

7.4.1 Overcurrent/Overvoltage/Thermal Protection

The device is protected from output overvoltage, overload and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the Vref. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections which help control the inductor current and avoid current runaway. If the overcurrent condition has lasted for more than the hiccup wait time, the device will shut down and re-start after the hiccup time. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. When the junction temperature drops 10°C typically below the thermal shutdown trip point, the built-in thermal shutdown hiccup timer is triggered. The device will be restarted under control of the slow start circuit automatically after the thermal shutdown hiccup time is over.

Furthermore, if the overcurrent condition has lasted for more than the hiccup wait time which is programmed for 512 switching cycles, the device will shut down itself and re-start after the hiccup time which is set for 16384 cycles. The hiccup mode helps to reduce the device power dissipation under severe overcurrent conditions.

7.4.2 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 165°C typically. Once the junction temperature drops below 155°C typically, the internal thermal hiccup timer will start to count. The device reinitiates the power up sequence after the built-in thermal shutdown hiccup time (32768 cycles) is over.

7.4.3 Small Signal Model for Loop Response

Figure 14 shows an equivalent model for the device control loop which can be modeled in a circuit simulation program to check frequency response and transient responses. The error amplifier is a trans conductance amplifier with a gm of 1300µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_{oea} (3.07 MΩ) and capacitor C_{oea} (20.7 pF) model the open loop gain and frequency response of the error amplifier. The 1-mV ac voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c and c/b show the small signal responses of the power stage and frequency compensation respectively. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

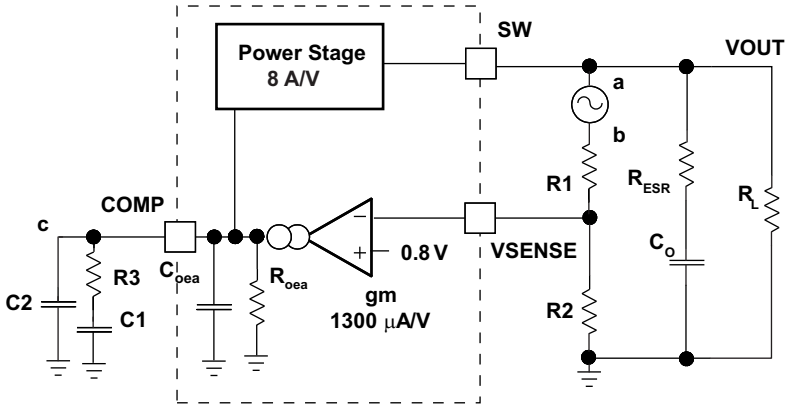


Figure 14. Small Signal Model for Loop Response

7.4.4 Small Signal Model for Peak Current Mode Control

Figure 15 is a simple small signal model that can be used to understand how to design the frequency compensation. The device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 4 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 14) is the power stage trans

Device Functional Modes (continued)

conductance (gm_{ps}) which is 8 A/V for the device. The DC gain of the power stage is the product of gm_{ps} and the load resistance, R_L, as shown in Equation 6 with resistive loads. As the load current increases, the DC gain decreases. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 6). The combined effect is highlighted by the dashed line in Figure 16. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

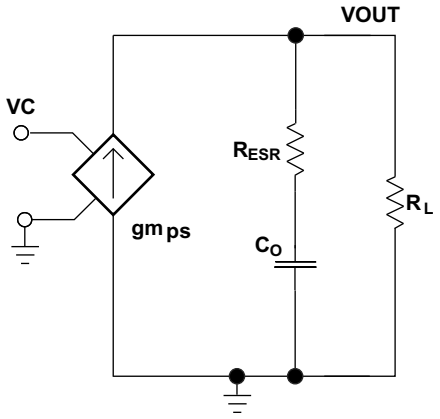


Figure 15. Small Signal Model for Peak Current Mode Control

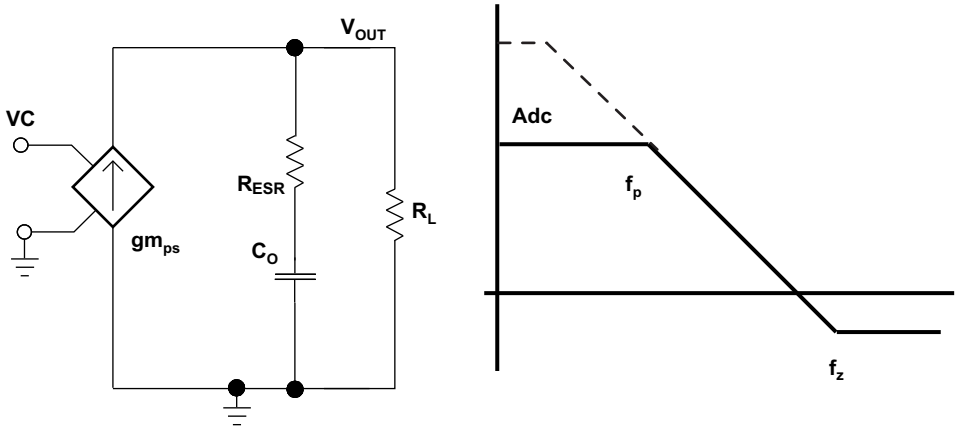


Figure 16. Simplified Frequency Response for Peak Current Mode Control

$$\frac{VOUT}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_z}\right)}{\left(1 + \frac{s}{2\pi \times f_p}\right)} \quad (4)$$

$$Adc = gm_{PS} \times R_L \quad (5)$$

$$f_p = \frac{1}{C_O \times R_L \times 2\pi} \quad (6)$$

$$f_z = \frac{1}{Co \times R_{ESR} \times 2\pi} \quad (7)$$

Where

gm_{ea} is the GM amplifier gain (1300µA/V)
gm_{PS} is the power stage gain (8A/V)

Device Functional Modes (continued)

R_L is the load resistance
C_O is the output capacitance
R_{ESR} is the equivalent series resistance of the output capacitors

7.4.5 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used Type II compensation circuits and a Type III frequency compensation circuit, as shown in Figure 17. In Type 2A, one additional high frequency pole, C6, is added to attenuate high frequency noise. In Type III, one additional capacitor, C11, is added to provide a phase boost at the crossover frequency. See *Designing Type III Compensation for Current Mode Step-Down Converters* (SLVA352) for a complete explanation of Type III compensation.

The design guidelines below are provided for advanced users who prefer to compensate using the general method. The below equations only apply to designs whose ESR zero is above the bandwidth of the control loop. This is usually true with ceramic output capacitors.

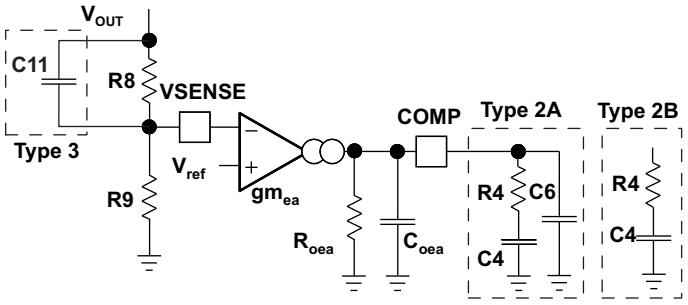


Figure 17. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency, f_c. A good starting point is 1/10th of the switching frequency, f_{sw}.

2. R4 can be determined by:

$$R4 = \frac{2\pi \times f_c \times V_{OUT} \times C_o}{gm_{ea} \times V_{ref} \times gm_{PS}} \quad (8)$$

where

- gm_{ea} is the GM amplifier gain (1300µA/V)
- gm_{PS} is the power stage gain (8A/V)
- V_{ref} is the reference voltage (0.8V)

3. Place a compensation zero at the dominant pole:

$$f_p = \frac{1}{C_O \times R_L \times 2\pi} \quad (9)$$

4. C4 can be determined by:

$$C4 = \frac{R_L \times C_O}{R4} \quad (10)$$

5. C6 is optional. It can be used to cancel the zero from the ESR of the output capacitor Co

$$C6 = \frac{R_{ESR} \times C_O}{R4} \quad (11)$$

6. Type III compensation can be implemented with the addition of one capacitor, C11. This allows for slightly higher loop bandwidths and higher phase margins. If used, C11 can be estimated from Equation 12.

Device Functional Modes (continued)

$$C11 = \frac{1}{2\pi \times R8 \times f_C} \quad (12)$$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following design procedure can be used to select component values for the TPS54334. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process using the TPS54334.

8.2 Typical Applications

8.2.1 TPS54334 Application

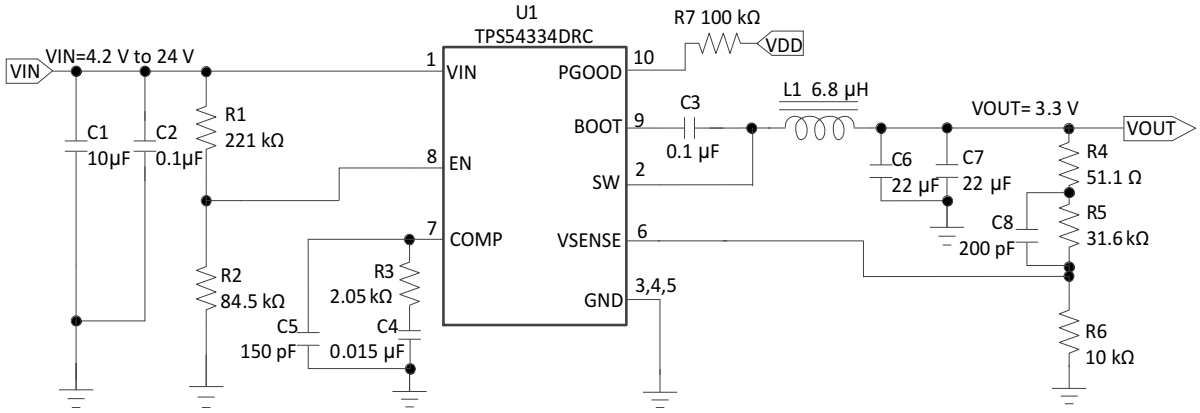


Figure 18. Typical Application Schematic, TPS54334

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.2 to 24 V
Output voltage	3.3 V
Transient response, 1.5-A load step	ΔV_O = ±5 %
Input ripple voltage	400 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating Frequency	570 kHz

8.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS54334. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process using the TPS54334 device.

For this design example, use the input parameters listed in Table 1.

8.2.1.2.1 Switching Frequency

The switching frequency of the TPS54334 device is set at 570 kHz to match the internally set frequency of the TPS54334 device for this design.

8.2.1.2.2 Output Voltage Set Point

The output voltage of the TPS54334 device is externally adjustable using a resistor divider network. In the application circuit of Figure 18, this divider network is comprised of R5 and R6. Use Equation 13 and Equation 14 to calculate the relationship of the output voltage to the resistor divider.

$$R6 = \frac{R5 \times V_{ref}}{V_{OUT} - V_{ref}} \tag{13}$$

$$V_{OUT} = V_{ref} \times \left[\frac{R5}{R6} + 1\right] \tag{14}$$

Select a value of R5 to be approximately 31.6 kΩ. Slightly increasing or decreasing R5 can result in closer output-voltage matching when using standard value resistors. In this design, R5 = 31.6 kΩ and R6 = 10 kΩ which results in a 3.328-V output voltage. The 51.1-Ω resistor, R4, is provided as a convenient location to break the control loop for stability testing.

8.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) set point can be adjusted using the external-voltage divider network of R1 and R2. R1 is connected between the VIN and EN pins of the TPS54334 device. R2 is connected between the EN and GND pins. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the minimum input voltage is 4.2V, so the start-voltage threshold is set to 4.1 V and the stop-voltage threshold is set to VIN UVLO (3.7V). Use Equation 2 and Equation 3 to calculate the values for the upper and lower resistor values of R1 and R2.

8.2.1.2.4 Input Capacitors

The TPS54334 device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF. A high-quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. A smaller value can be used as long as all other requirements are met; however a 10-µF capacitor has been shown to work well in a wide variety of circuits. Additionally, some bulk capacitance may be needed, especially if the TPS54334 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but should be rated to handle the maximum input voltage including ripple voltage, and should filter the output so that input ripple voltage is acceptable. For this design, a 10-µF, X7R dielectric capacitor rated for 35 V is used for the input decoupling capacitor. The ESR is approximately 2 mΩ, and the current rating is 3 A. Additionally, a small 0.1-µF capacitor is included for high frequency filtering.

Use Equation 15 to calculate the input ripple voltage (ΔV_{IN}).

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{SW}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \tag{15}$$

where

- C_{BULK} is the bulk capacitor value
- f_{SW} is the switching frequency
- $I_{OUT(MAX)}$ is the maximum load current
- ESR_{MAX} is the maximum series resistance of the bulk capacitor

The maximum RMS (root mean square) ripple current must also be checked. For worst case conditions, use Equation 16 to calculate $I_{CIN(RMS)}$.

$$I_{CIN(RMS)} = \frac{I_{O(MAX)}}{2} \tag{16}$$

In this case, the input ripple voltage is 138 mV and the RMS ripple current is 1.5 A.

NOTE

The actual input-voltage ripple is greatly affected by parasitics associated with the layout and the output impedance of the voltage source.

Design Requirements shows the actual input voltage ripple for this circuit which is larger than the calculated value. This measured value is still below the specified input limit of 400 mV. The maximum voltage across the input capacitors is $V_{IN(MAX)} + \Delta V_{IN} / 2$. The selected bypass capacitor is rated for 35 V and the ripple current capacity is greater than 3 A. Both values provide ample margin. The maximum ratings for voltage and current must not be exceeded under any circumstance.

8.2.1.2.5 Output Filter Components

Two components must be selected for the output filter, the output inductor (L_O) and C_O. Because the TPS54334 device is an externally compensated device, a wide range of filter component types and values can be supported.

8.2.1.2.5.1 Inductor Selection

Use Equation 17 to calculate the minimum value of the output inductor (L_{MIN}).

$$L_{MIN} = \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times K_{IND} \times I_{OUT} \times f_{SW}} \tag{17}$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

In general, the value of K_{IND} is at the discretion of the designer; however, the following guidelines may be used. For designs using low-ESR output capacitors, such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.3. The minimum inductor value is calculated as 5.6 µH. For this design, a standard value of 6.8 µH was selected for L_{MIN}.

For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 18 to calculate the RMS inductor current ($I_{L(RMS)}$).

$$I_{L(RMS)} = \sqrt{I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times 0.8} \right)^2} \tag{18}$$

Use Equation 19 to calculate the peak inductor current ($I_{L(PK)}$).

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times f_{SW}} \quad (19)$$

For this design, the RMS inductor current is 3.01 A and the peak inductor current is 3.459 A. The selected inductor is a Vishay 6.8 µH, IHLP-4040DZ-01. Smaller or larger inductor values can be used depending on the amount of ripple current the designer wants to allow so long as the other design requirements are met. Larger value inductors have lower AC current and result in lower output voltage ripple. Smaller inductor values increase AC current and output voltage ripple. In general, for the TPS54334 device, use inductors with values in the range of 0.68 µH to 100 µH.

8.2.1.2.5.2 Capacitor Selection

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of drop in the output voltage. Use Equation 20 to calculate the minimum required output capacitance.

$$C_O > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the switching frequency of the regulator
- ΔV_{OUT} is the allowable change in the output voltage (20)

For this example, the transient load response is specified as a 5% change in the output voltage, V_{OUT}, for a load step of 1.5 A. For this example, ΔI_{OUT} = 1.5 A and ΔV_{OUT} = 0.05 × 3.3 = 0.165 V. Using these values results in a minimum capacitance of 31.9 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 21 calculates the minimum output capacitance required to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, Equation 21 yields 3.65 µF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{OUTripple}}{I_{ripple}}}$$

where

- f_{SW} is the switching frequency
- $V_{OUTripple}$ is the maximum allowable output voltage ripple
- I_{ripple} is the inductor ripple current (21)

Use Equation 22 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 22 indicates the ESR should be less than 40.9 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 40.9 mΩ.

$$R_{ESR} < \frac{V_{OUTripple}}{I_{ripple}} \quad (22)$$

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, two 22-µF 25-V X7R ceramic capacitors with 3 mΩ of ESR are used. Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 23 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 23 yields 106 mA for each capacitor.

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left(\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times f_{SW} \times N_C} \right) \quad (23)$$

8.2.1.2.6 Compensation Components

Several possible methods exist to design closed loop compensation for DC-DC converters. For the ideal current-mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and begins to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees which is one decade above the modulator pole frequency. Use Equation 24 to calculate the simple modulator pole (f_{p_mod}).

$$f_{p\_mod} = \frac{I_{OUT}\,max}{2\pi \times V_{OUT} \times C_{OUT}} \quad (24)$$

For the TPS54334 device, most circuits have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics deviate from the ideal approximations. The phase loss of the power stage will now approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it requires a tedious calculation. Use the PSpice model to accurately model the power-stage gain and phase so that a reliable compensation circuit can be designed. Alternately, a direct measurement of the power stage characteristics can be used which is the technique used in this design procedure. For this design, the calculated values are as follows:

L1 = 6.8 µH

C6 and C7 = 22 µF

ESR = 3 mΩ

Figure 19 shows the power stage characteristics.

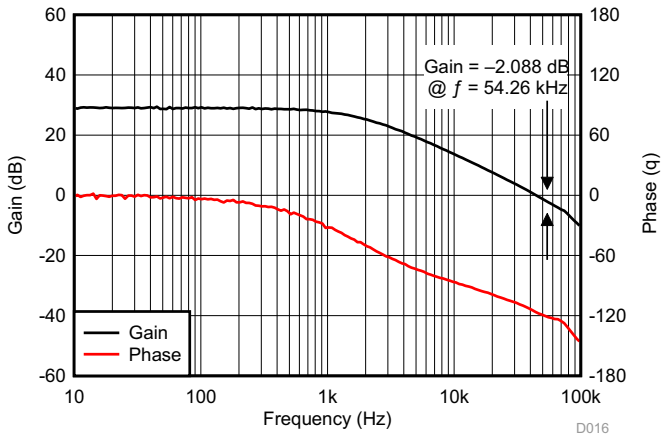


Figure 19. Power Stage Gain and Phase Characteristics

For this design, the intended crossover frequency is 54.26 kHz (an actual measured data point exists for that frequency). From the power stage gain and phase plots, the gain at 54.26 kHz is –2.088 dB and the phase is about –121 degrees. For 60 degrees of phase margin, additional phase boost from a feed-forward capacitor in parallel with the upper resistor of the voltage set point divider is needed. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. Use Equation 25 to calculate the required value of R3.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{ea}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \quad (25)$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 54.26 kHz. Use Equation 26 to calculate the required value for C4.

$$C4 = \frac{1}{2 \times \pi \times R3 \times \frac{f_{CO}}{10}} \quad (26)$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 54.26 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. Use Equation 27 to calculate the value of C5.

$$C5 = \frac{1}{2 \times \pi \times R3 \times 10 \times f_{CO}} \quad (27)$$

To Maximize Phase margin, use Type-lll compensation to provide a zero around the desired crossover frequency (f_{co}) with R5, V_{OUT} and V_{REF}.

$$C8 = \frac{1}{2\pi \times R5 \times f_{CO}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \quad (28)$$

For this design the calculated values for the compensation components are as follows:

R3 = 2.05 kΩ
C4 = 0.015 µF
C5 = 150 pF
C8 = 200 pF

8.2.1.2.7 Bootstrap Capacitor

Every TPS54334 design requires a bootstrap capacitor, C3. The bootstrap capacitor value must 0.1 µF. The bootstrap capacitor is located between the SW and BOOT pins. The bootstrap capacitor should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

8.2.1.2.8 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode operations. These formulas should not be used if the device is working in the discontinuous conduction mode (DCM) or pulse-skipping Eco-mode™.

The device power dissipation includes:

1. Conduction loss:

   $P_{CON} = I_{OUT}^2 \times r_{DS(on)} \times V_{OUT} / V_{IN}$

   where

   - I_{OUT} is the output current (A)
   - $r_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
   - V_{OUT} is the output voltage (V)
   - V_{IN} is the input voltage (V) (29)

2. Switching loss:

   $E = 0.5 \times 10^{-9} \times V_{IN}^2 \times I_{OUT} \times f_{SW}$

   where

   - f_{SW} is the switching frequency (Hz) (30)

3. Gate charge loss:

   $P_G = 22.8 \times 10^{-9} \times f_{SW}$ (31)

4. Quiescent current loss:

   $P_Q = 0.31 \times 10^{-3} \times V_{IN}$ (32)

Therefore:

$$P_{tot} = P_{CON} + E + P_G + P_Q$$

where

- P_{tot} is the total device power dissipation (W) (33)

For given T_A :

$$T_J = T_A + R_{th} \times P_{tot}$$

where

- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{th} is the thermal resistance of the package (°C/W) (34)

For given $T_J$max = 150°C:

$$T_A\text{max} = T_J\text{max} – R_{th} \times P_{tot}$$

where

- $T_A$max is the maximum ambient temperature (°C)
- $T_J$max is the maximum junction temperature (°C) (35)

8.2.1.3 Application Curves

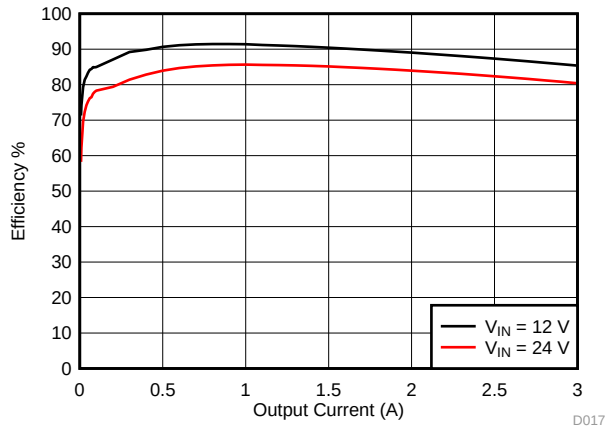


Figure 20. TPS54334 Efficiency

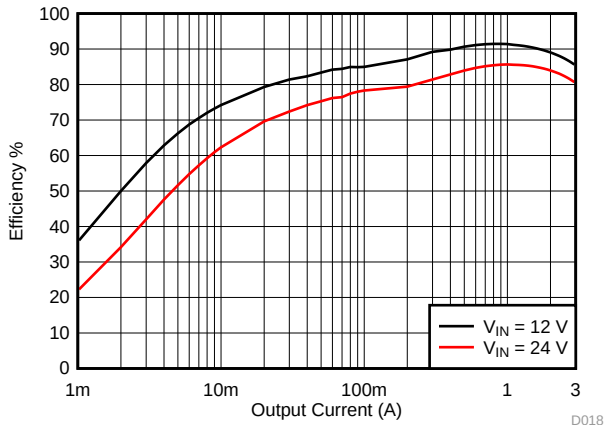


Figure 21. TPS54334 Low-Current Efficiency

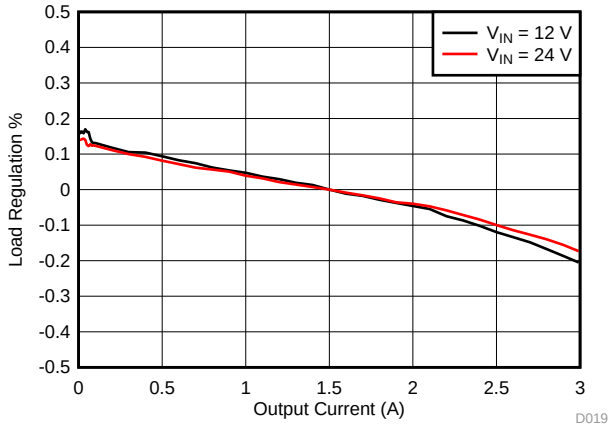


Figure 22. TPS54334 Load Regulation

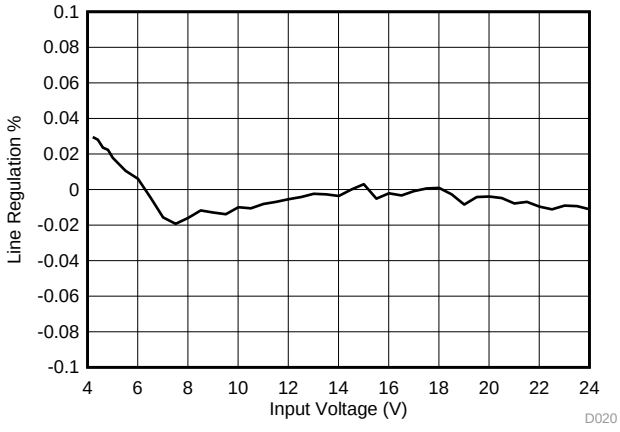


Figure 23. TPS54334 Line Regulation

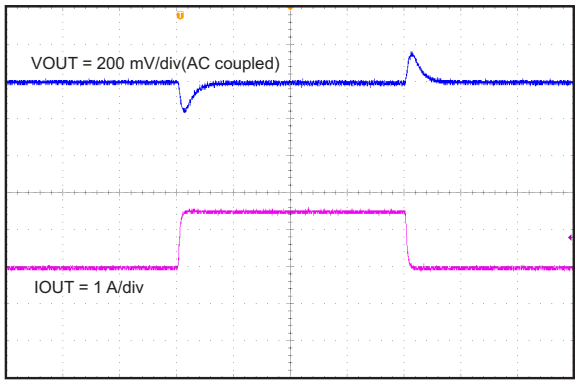


Figure 24. TPS54334 Transient Response

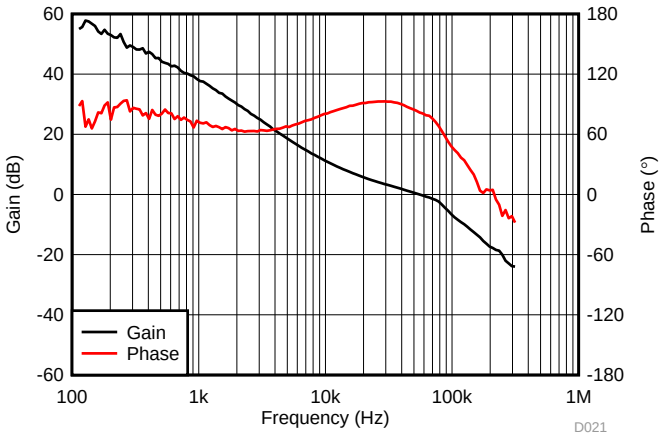


Figure 25. TPS54334 Loop Response

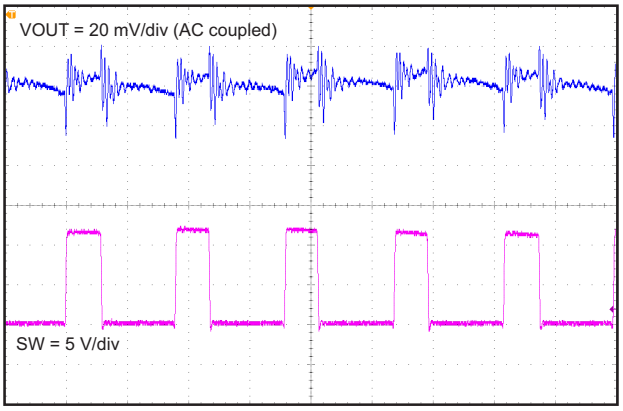


Figure 26. TPS54334 Full-Load Output Ripple

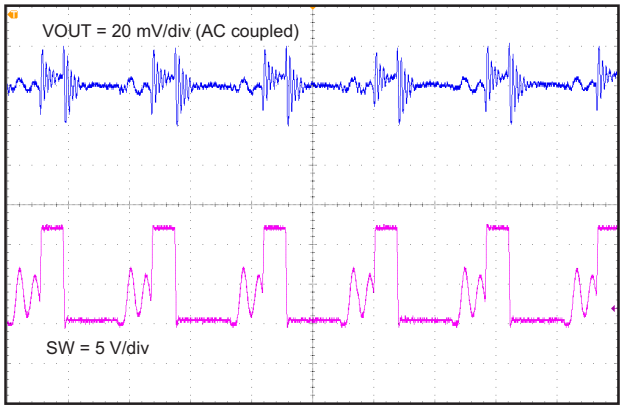


Figure 27. TPS54334 200-mA Output Ripple

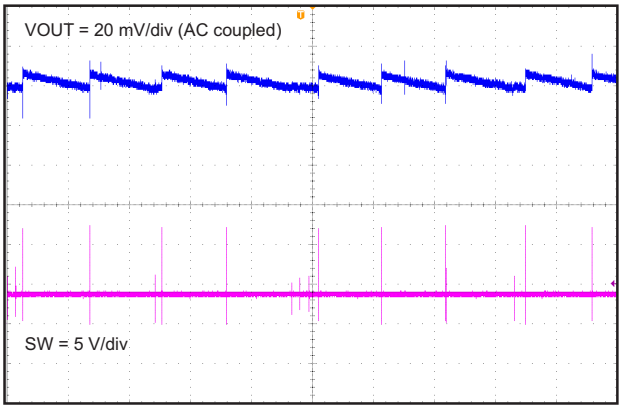


Figure 28. TPS54334 No-Load Output Ripple

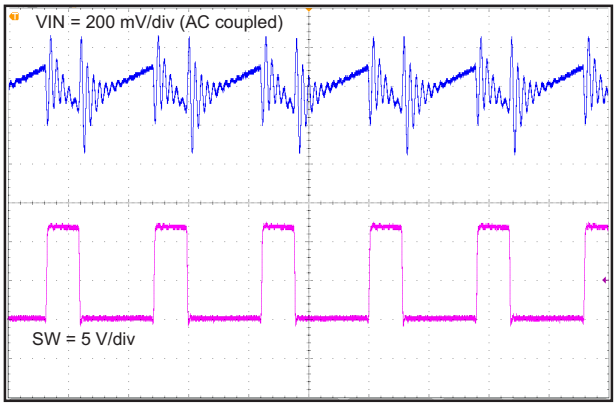


Figure 29. TPS54334 Full-Load Input Ripple

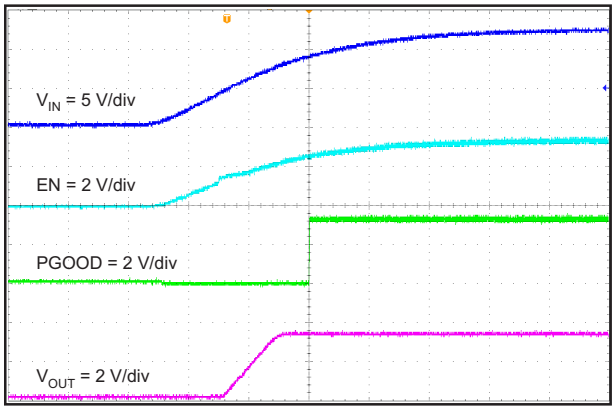


Figure 30. TPS54334 Startup Relative To VIN

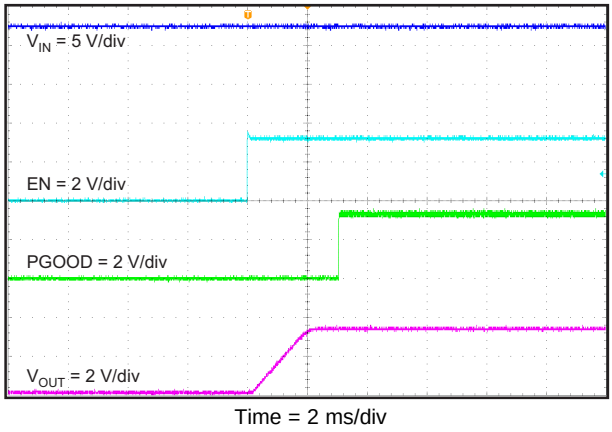


Figure 31. TPS54334 Startup Relative To Enable

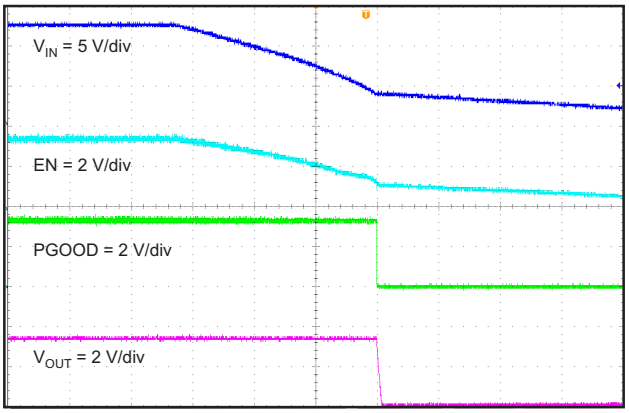


Figure 32. TPS54334 Shutdown Relative To VIN

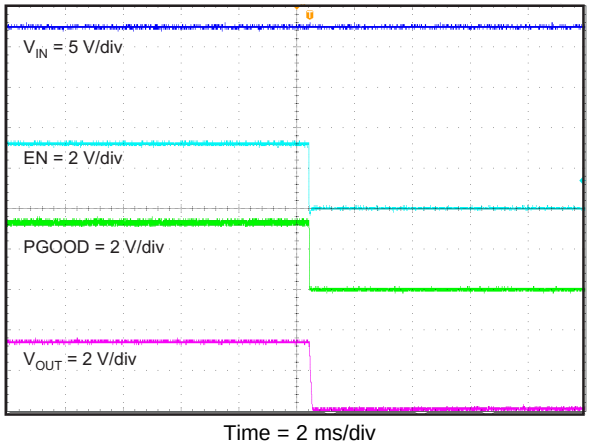


Figure 33. TPS54334 Shutdown Relative To EN

9 Power Supply Recommendations

The devices are designed to operate from an input supply ranging from 4.2 V to 28 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter an additional bulk capacitance, typically 100 µF, may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connection. the VIN pin, and the GND pin of the IC. The typical recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN and GND pins of the device. See Figure 34 for a PCB layout example. The GND pin should be tied to the PCB ground plane at the pin of the IC. To facilitate close placement of the input bypass capacitors, The SW pin should be routed to a small copper area directly adjacent to the pin. Use vias to rout the SW signal to the bottom side or an inner layer. If necessary you can allow the top side copper area to extend slightly under the body of the closest input bypass capacitor. Make the copper trace on the bottom or internal layer short and wide as practical to reduce EMI issues. Connect the trace with vias back to the top side to connect with the output inductor as shown after the GND pin. In the same way use a bottom or internal layer trace to rout the SW signal across the VIN pin to connect to the BOOT capacitor as shown. Make the circulating loop from SW to the output inductor, output capacitors and back to GND as tight as possible while preserving adequate etch width to reduce conduction losses in the copper.

Layout Guidelines (continued)

For operation at full rated load, the ground area near the IC must provide adequate heat dissipating area. Connect the exposed thermal pad to bottom or internal layer ground plane using vias as shown. Additional vias may be used adjacent to the IC to tie top side copper to the internal or bottom layer copper. The additional external components can be placed approximately as shown. Use a separate ground trace to connect the feedback, compensation, UVLO and RT returns. Connect this ground trace to the main power ground at a single point to minimize circulating currents. It may be possible to obtain acceptable performance with alternate layout schemes, however this layout has been shown to produce good results and is intended as a guideline.

10.2 Layout Example

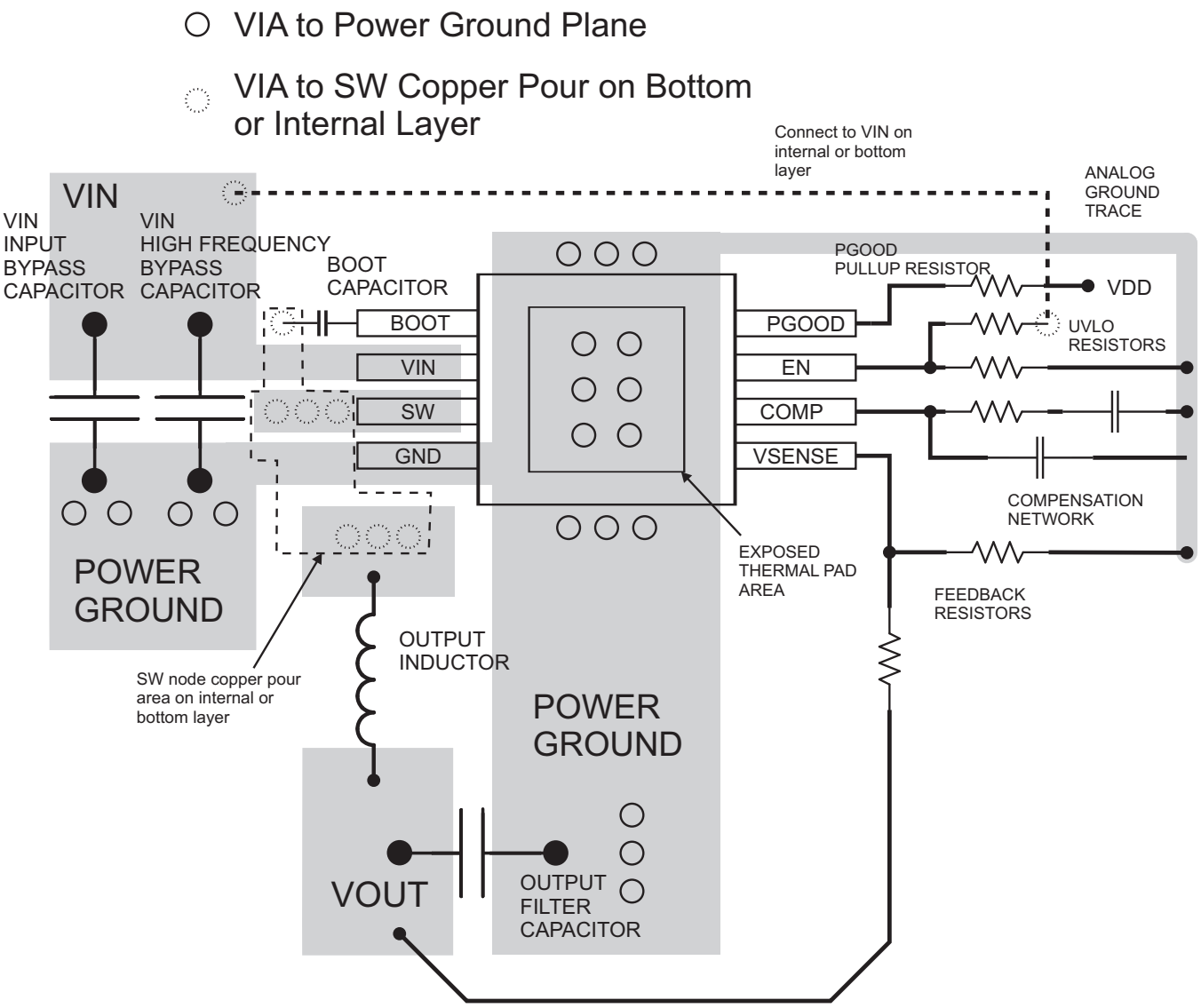


Figure 34. TPS54334DDA Board Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For the WEBENCH circuit design and selection simulation services, go to www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Designing Type III Compensation for Current Mode Step-Down Converters (SLVA352)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, Eco-mode, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54334DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	54334	Samples
TPS54334DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 150	54334	Samples
TPS54334DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54334	Samples
TPS54334DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	54334	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

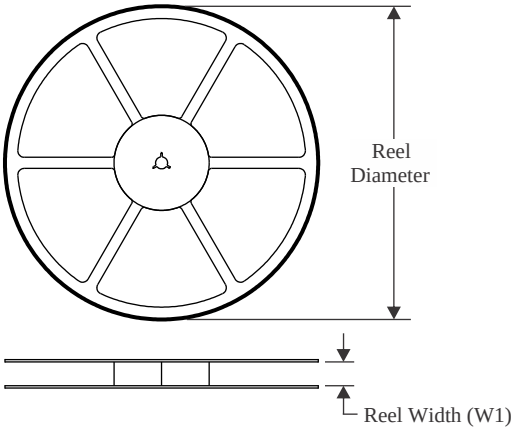
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

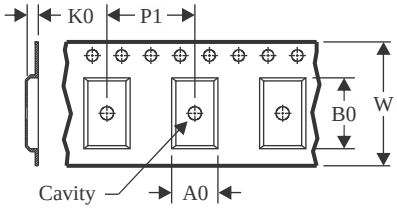
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

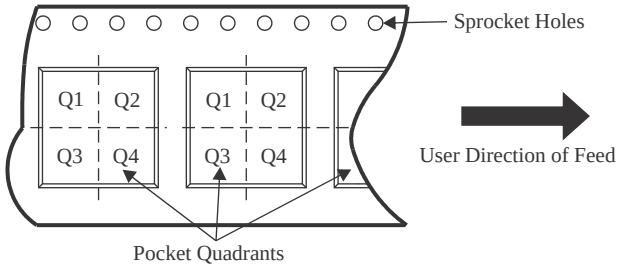


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

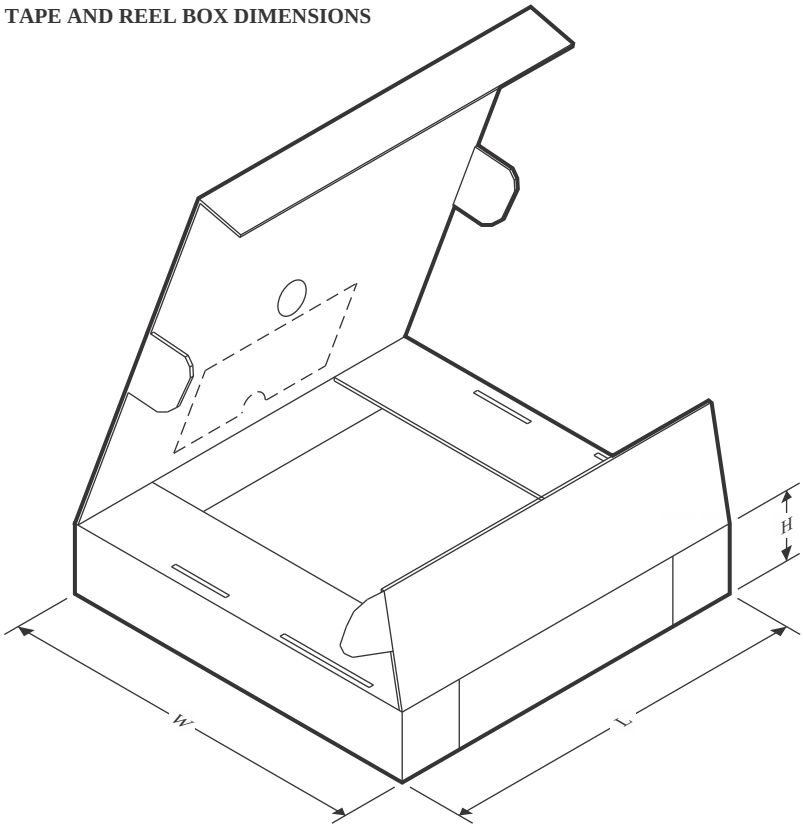
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54334DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS54334DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54334DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

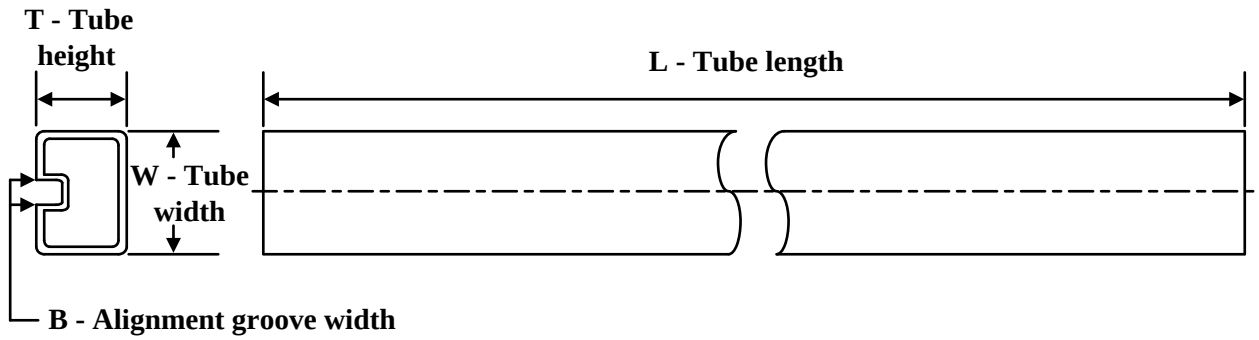
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54334DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS54334DRCR	VSON	DRC	10	3000	335.0	335.0	25.0
TPS54334DRCT	VSON	DRC	10	250	182.0	182.0	20.0

TUBE

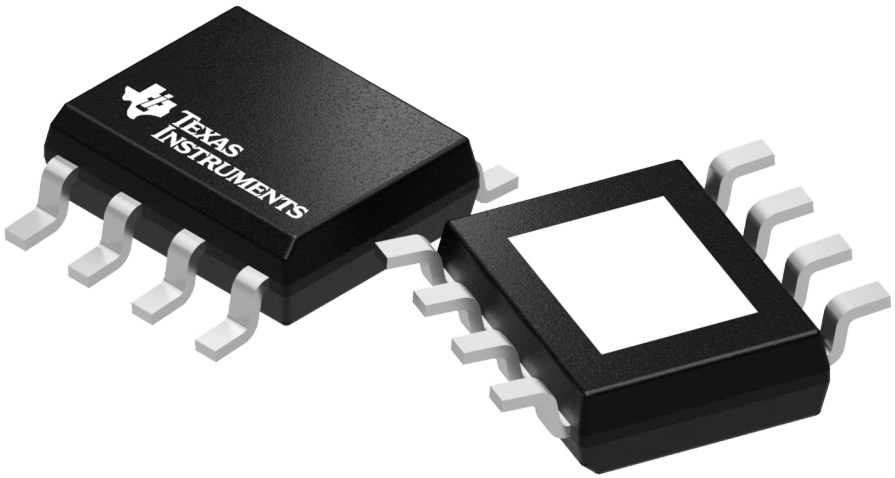


*All dimensions are nominal

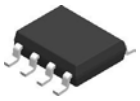
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS54334DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

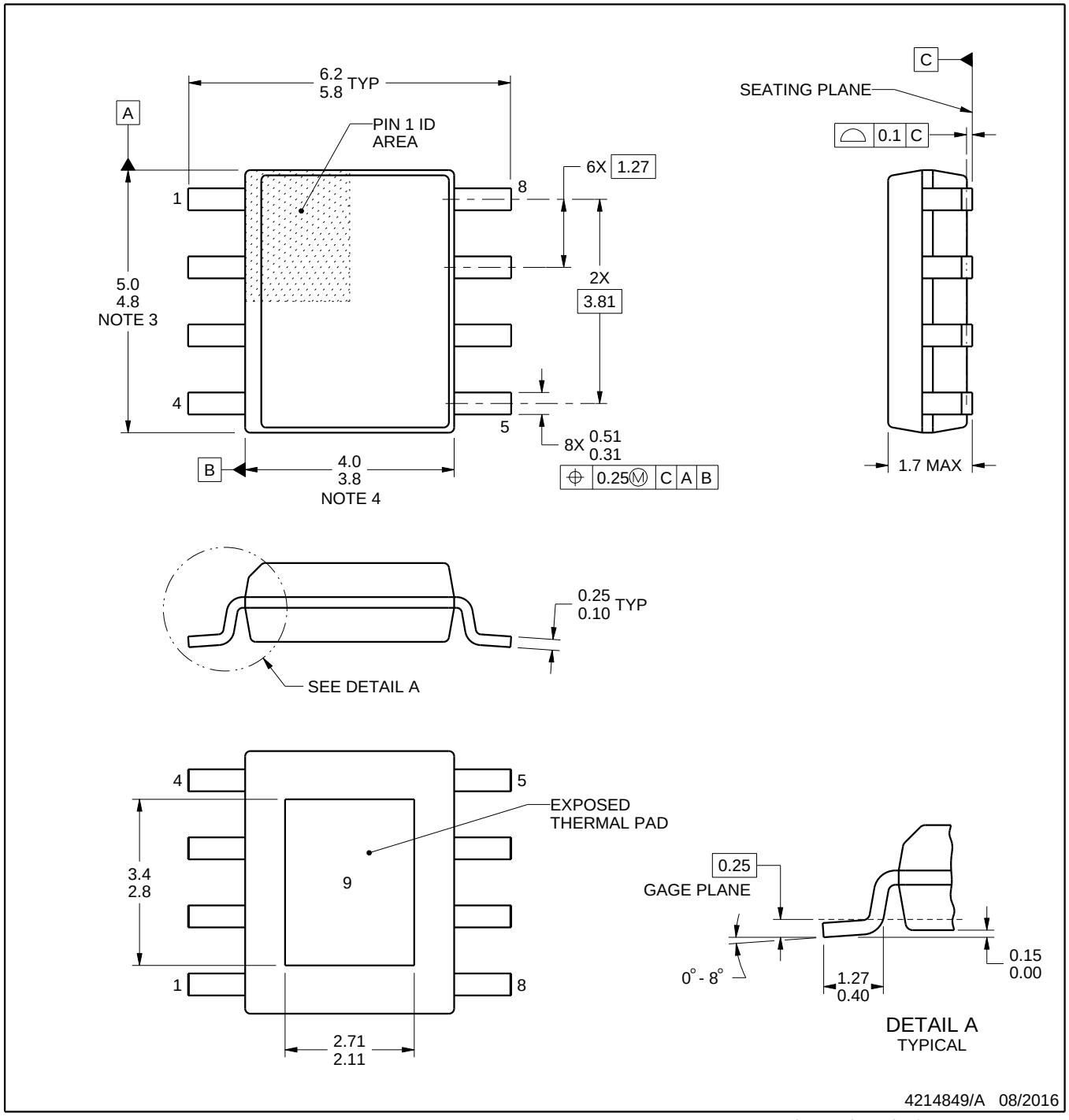


PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

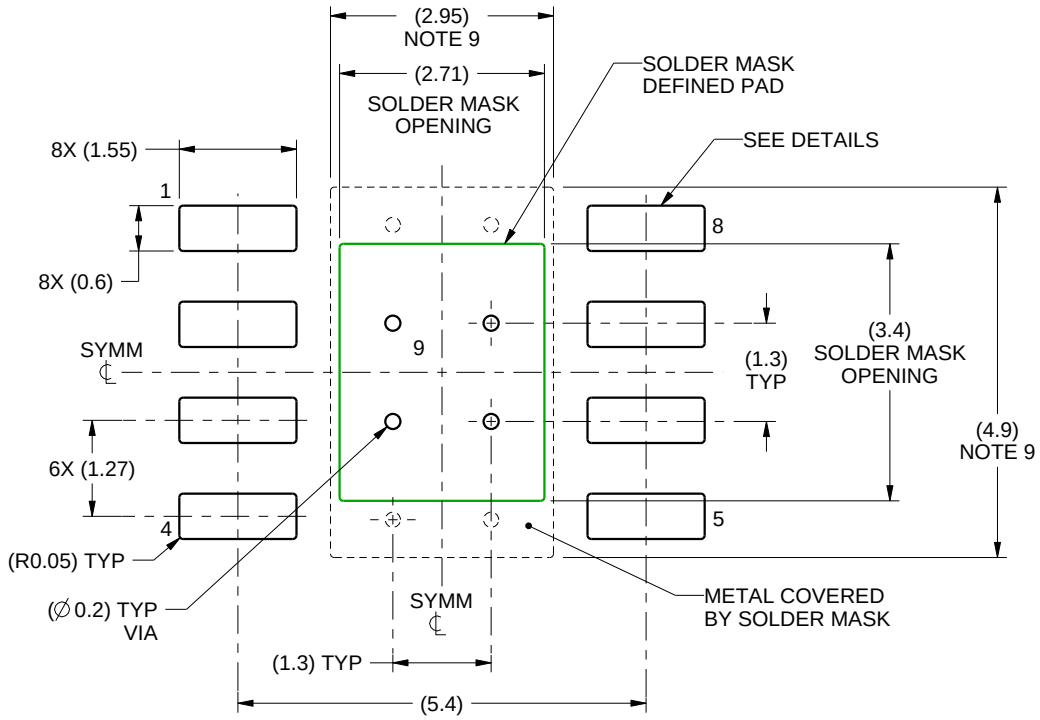
PLASTIC SMALL OUTLINE



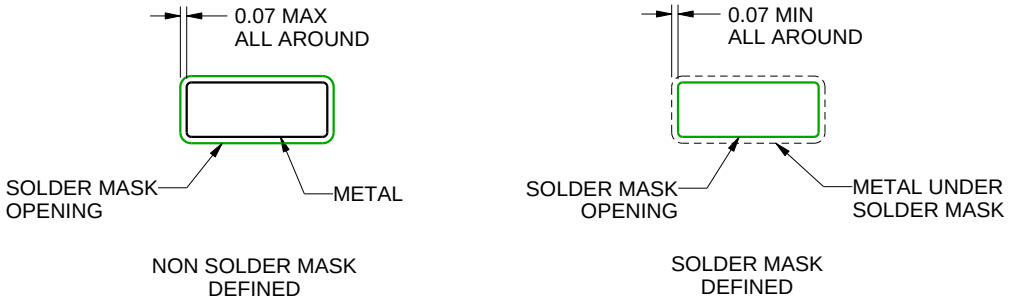
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

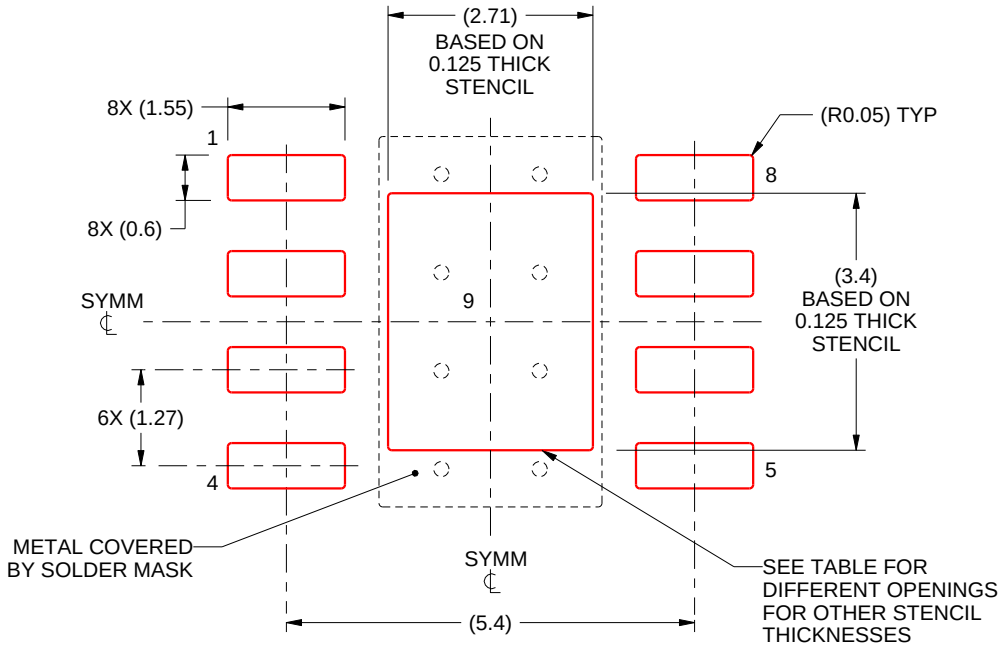
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

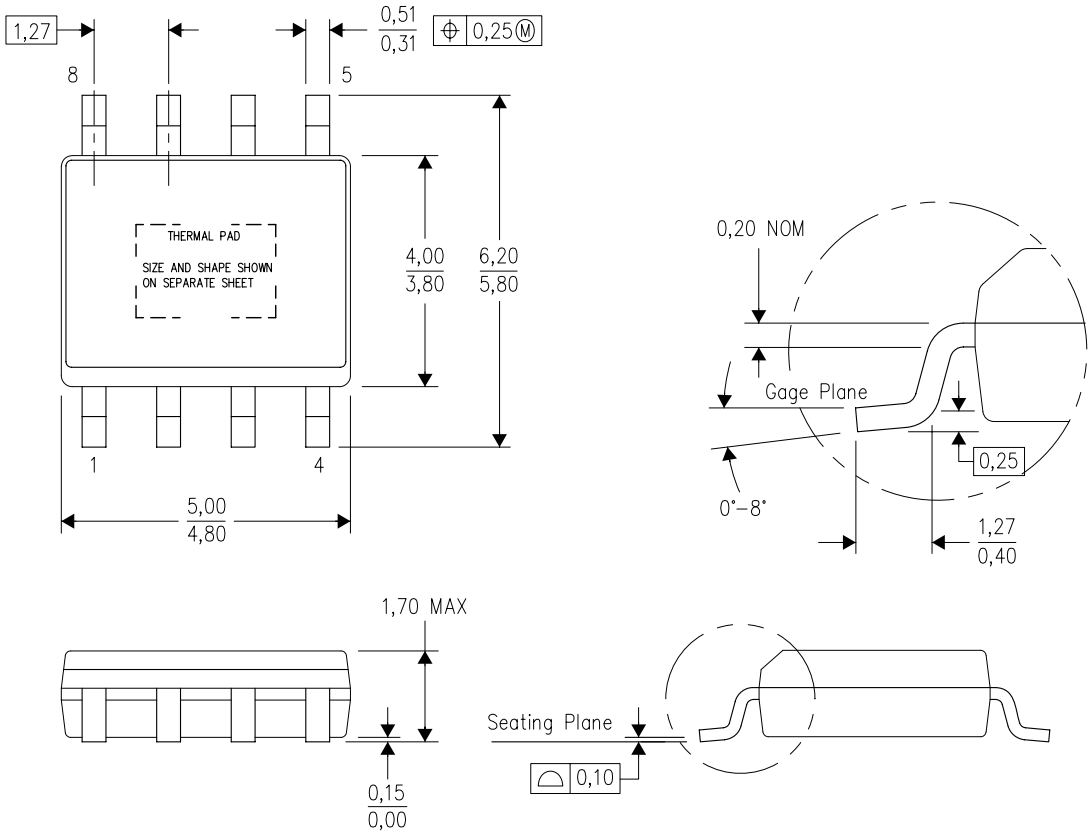
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

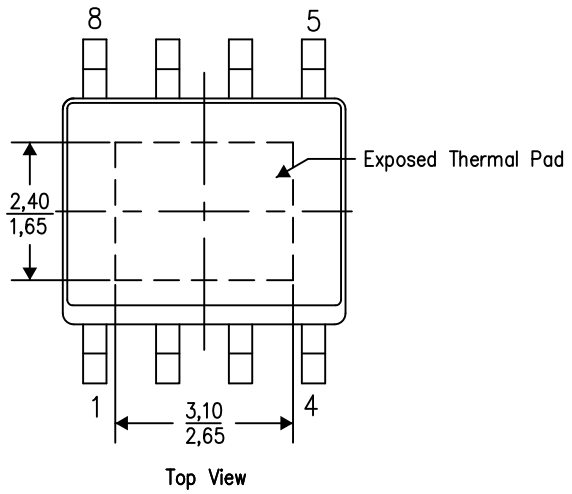
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



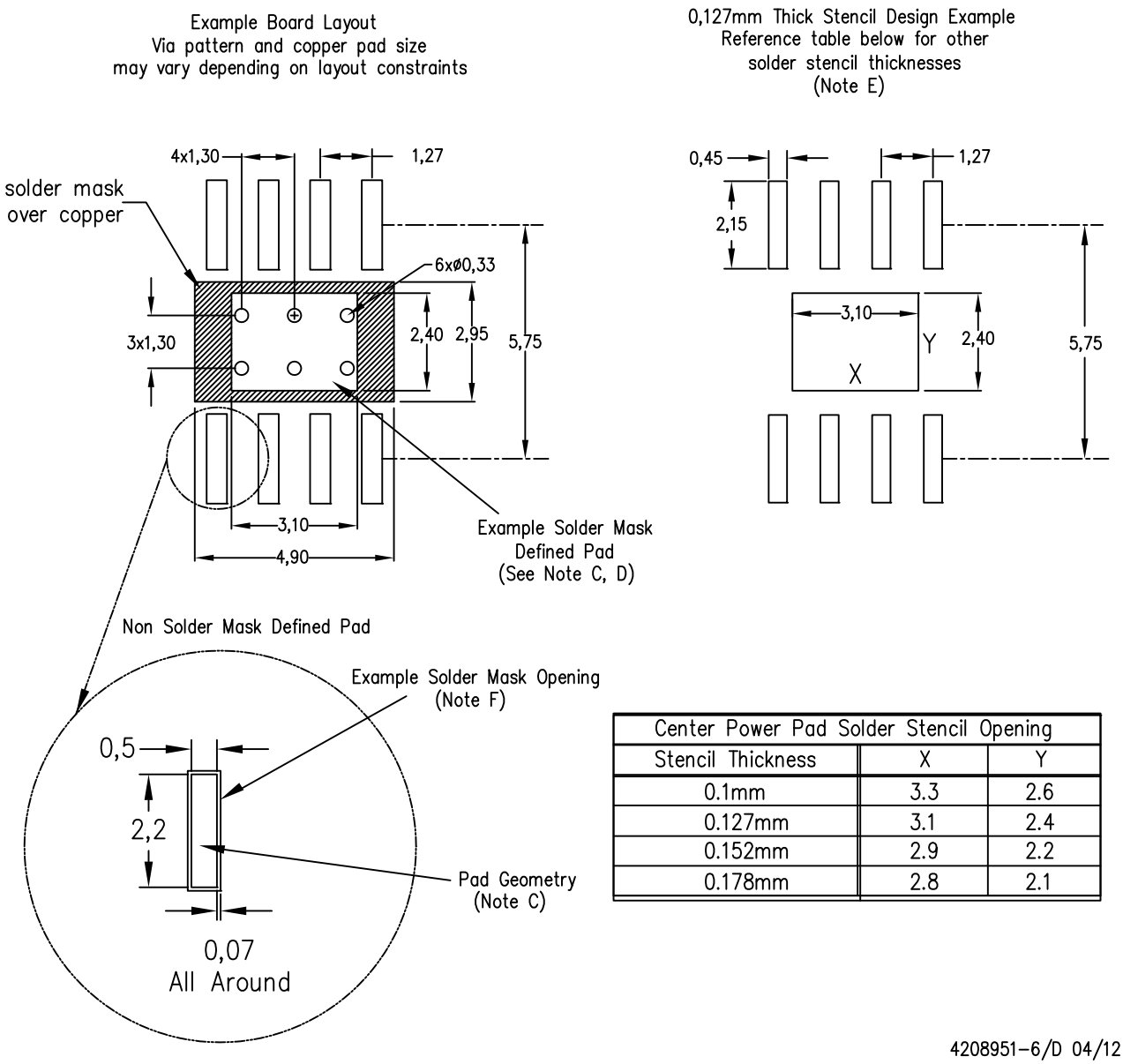
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

GENERIC PACKAGE VIEW

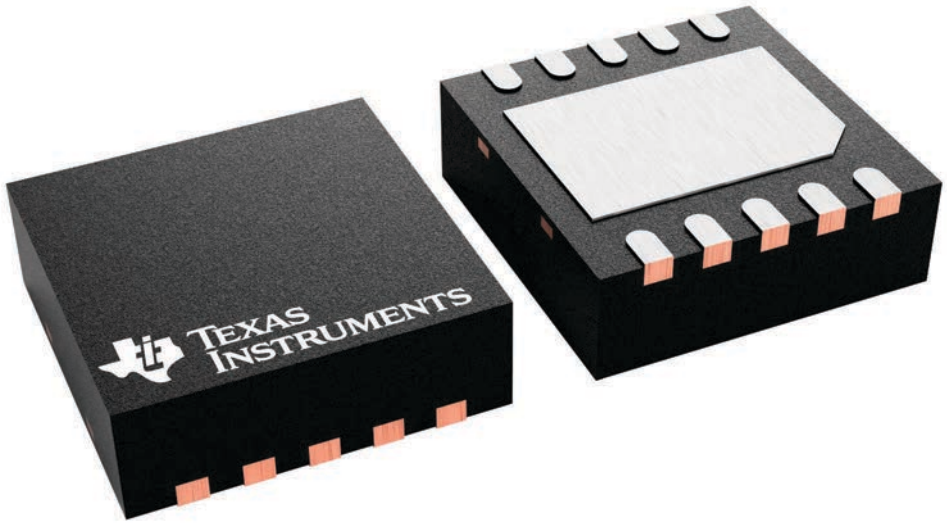
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226193/A

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