

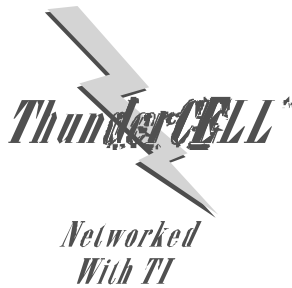
TNETA1570

ThunderCELL

HyperSAR

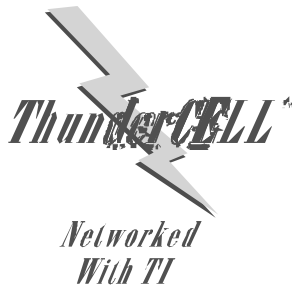
Networking Business Unit

4atm@msg.ti.com



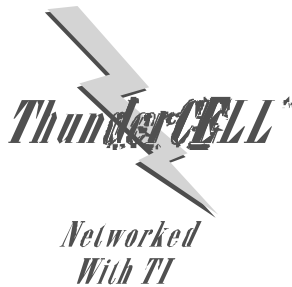
Agenda

- **Main Features**
- **Interfaces**
- **Architecture**
- **Applications**
- **Summary**



Design Objectives

- **Architecture provides for legacy LAN to asynchronous transfer mode (ATM) translation**
- **High performance (>200 Mbit/s) to support more LAN ports**
- **Direct interface to local switching fabric capability**
- **Efficient buffer chaining and data structures tailored for internetworking products**



Main Features

FEATURE

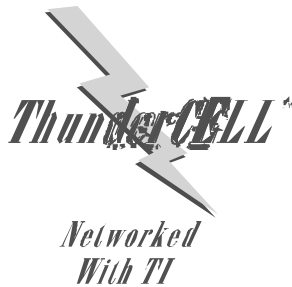
- **Supports 200 Mbit/s throughput full-duplex**
- **Early segmentation feature**
- **Integrated 32-/64-bit PCI interface**

- **Easy access to AAL5 trailer information**
- **Supports buffer scatter/gather (transmit/receive buffer chaining)**

BENEFIT

- **Can support a greater number of legacy LAN ports**
- **Provides cut-through capability**
- **Easily interfaced to 32- or 64-bit buses**

- **Makes it easier to support frame relay over ATM**
- **Makes more efficient use of memory**



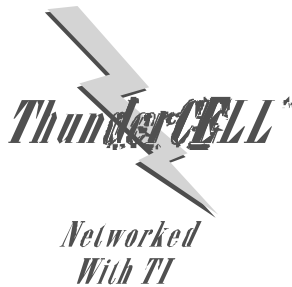
Main Features (cont.)

FEATURE

- Segmentation/reassembly of AAL5 packets
- Supports a transparent AAL
- High-priority transmit mechanism
- Supports full range of VPIs (12 bits) and 30,720 VCIs
- NNI/UNI option for handling VPIs

BENEFIT

- Full support in hardware for AAL5 processing
- Can be used to support other AALs or for proprietary control
- Hardware-oriented method to support CBR traffic
- Can be used for NNI (network-to-network interface) applications
- VPI bits masked by 1570 in UNI mode to reduce software overhead



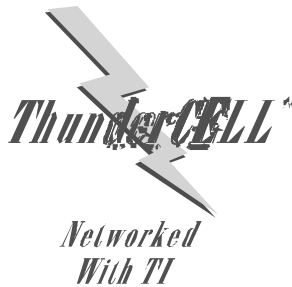
Main Features (cont.)

FEATURE

- **Simultaneous segmentation of up to 1,023 packets**
- **Reassembly of 30,720 packets**
- **Implements optional reassembly time-out for incoming packets**
- **MIB counters for:**
 - IETF; RFC1695
 - ATM Forum; UNI 3.1 ILMI

BENEFIT

- **Can support 1,023 transmit channels at any one time**
- **Can support 30,720 receive channels at any one time**
- **Allows early release of memory buffers and terminates a channel that has died**
- **Provides all the real-time MIB counters on chip to support management functions**



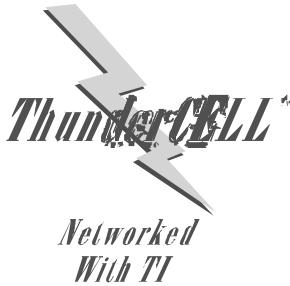
Main Features (cont.)

FEATURE

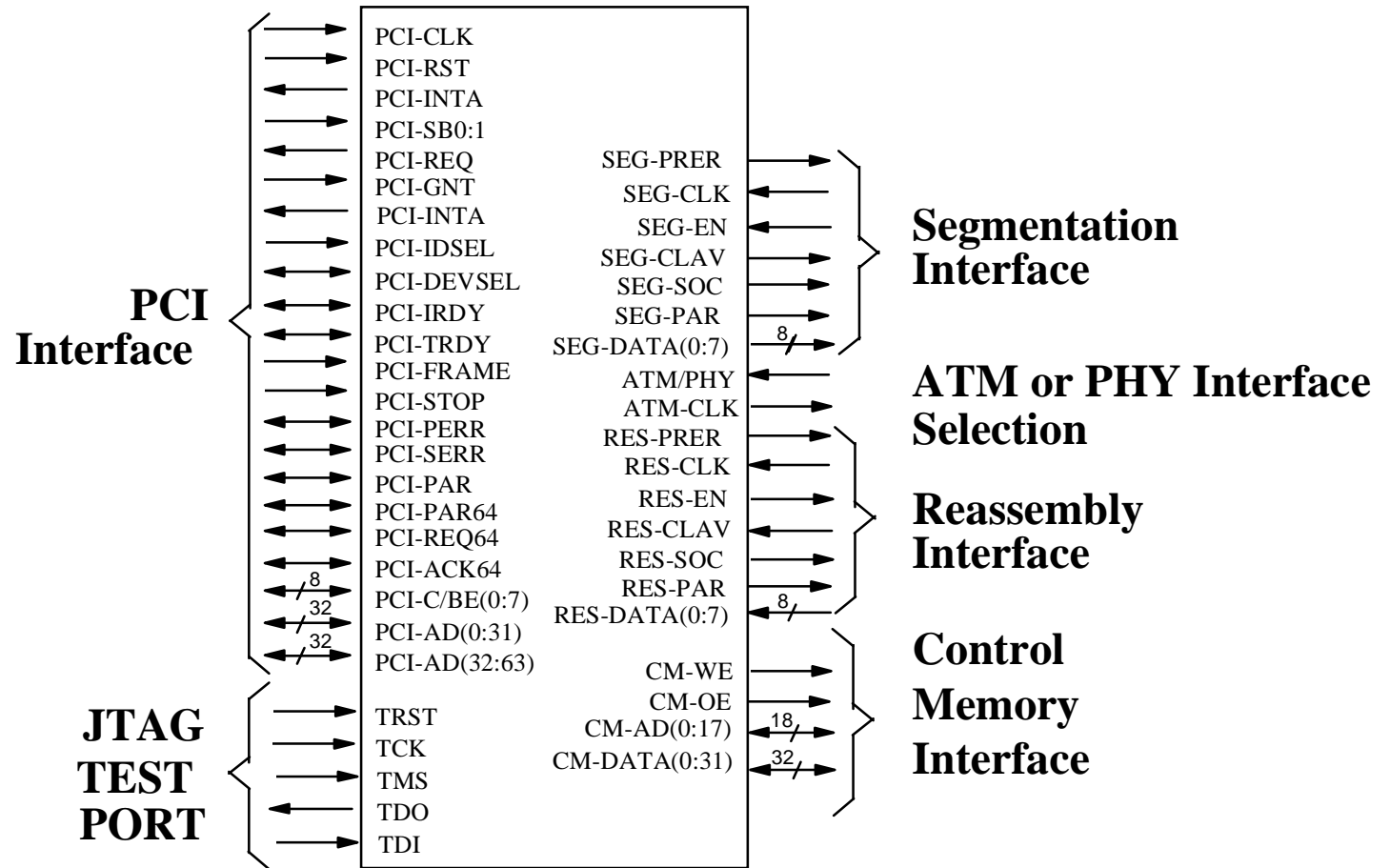
- UTOPIA Level 1, configurable for physical layer (PHY) or ATM device
- Calculates and checks HEC byte
- Provides internal loopback for transmit receive
- Supports JTAG boundary scan interface

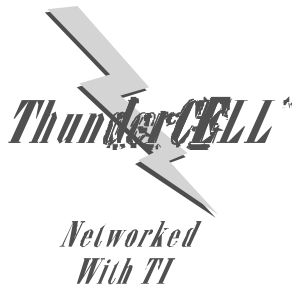
BENEFIT

- For local switching fabrics, saves cost of PHY devices and provides higher performance
- Allows the TNETA1570 to interface directly to switch core when nonATM traffic is coming into the part
- Provides system diagnostic capability
- Allows board-level testing



TNETA1570 HyperSAR Interfaces





PCI Host Interface

FEATURE

- **PCI revision 2.0 compliant host interface**
- **Supports single cycle data transfers in burst mode**
- **Operates as a 32-bit PCI slave device for accesses to configuration space, internal registers and control memory**

BENEFIT

- **Complies to industry standards**
- **Utilizes PCI capabilities for performance**
- **Ease of use**



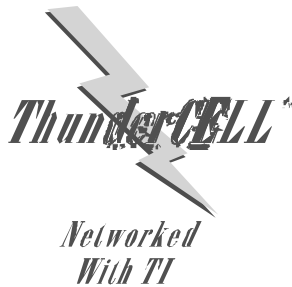
PCI Host Interface (cont.)

FEATURE

- Operates as a bus master device for accesses to data structures in host memory
- Performs 32- or 64-bit data transfers to/from host memory
- In 32-bit PCI mode, upper 32 bits are in quiet mode
- All configuration registers implemented in internal registers

BENEFIT

- Provides high performance throughput for data transfer
- Can interface to 64-bit systems
- Reduces system noise (ease of use)
- No external memory required for configuration of device



Control Memory Interface

FEATURE

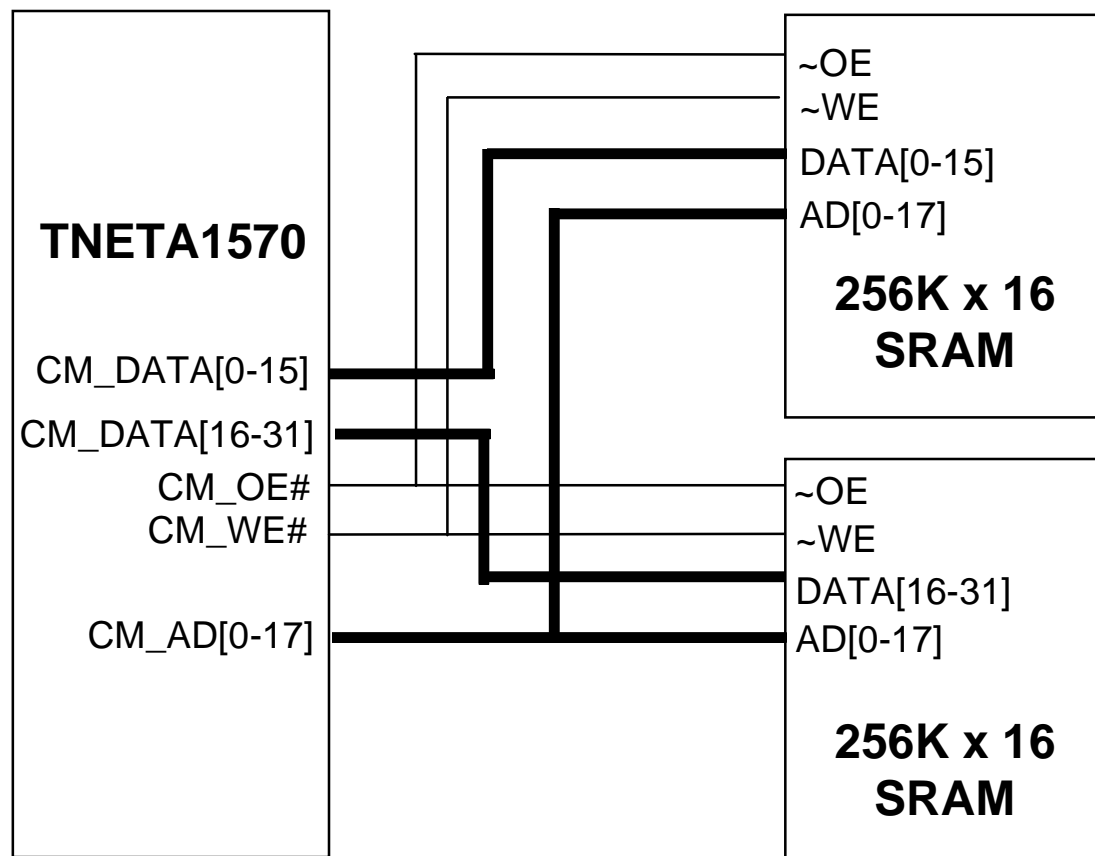
- Control memory interface provides a glueless interface to local SRAM (15 ns)
- Choice of two control memory maps via the configuration register:
 - Normal control memory map (32K-256K x 32 SRAM)
 - Small control memory map (16K x 32 SRAM)

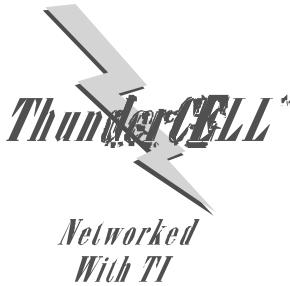
BENEFIT

- No external logic required (saves cost)
- Provides the flexibility to scale system features and save cost:
 - Allows control memory to handle maximum size of all the data structures
 - Restricts the size of data structures to reduce memory requirements



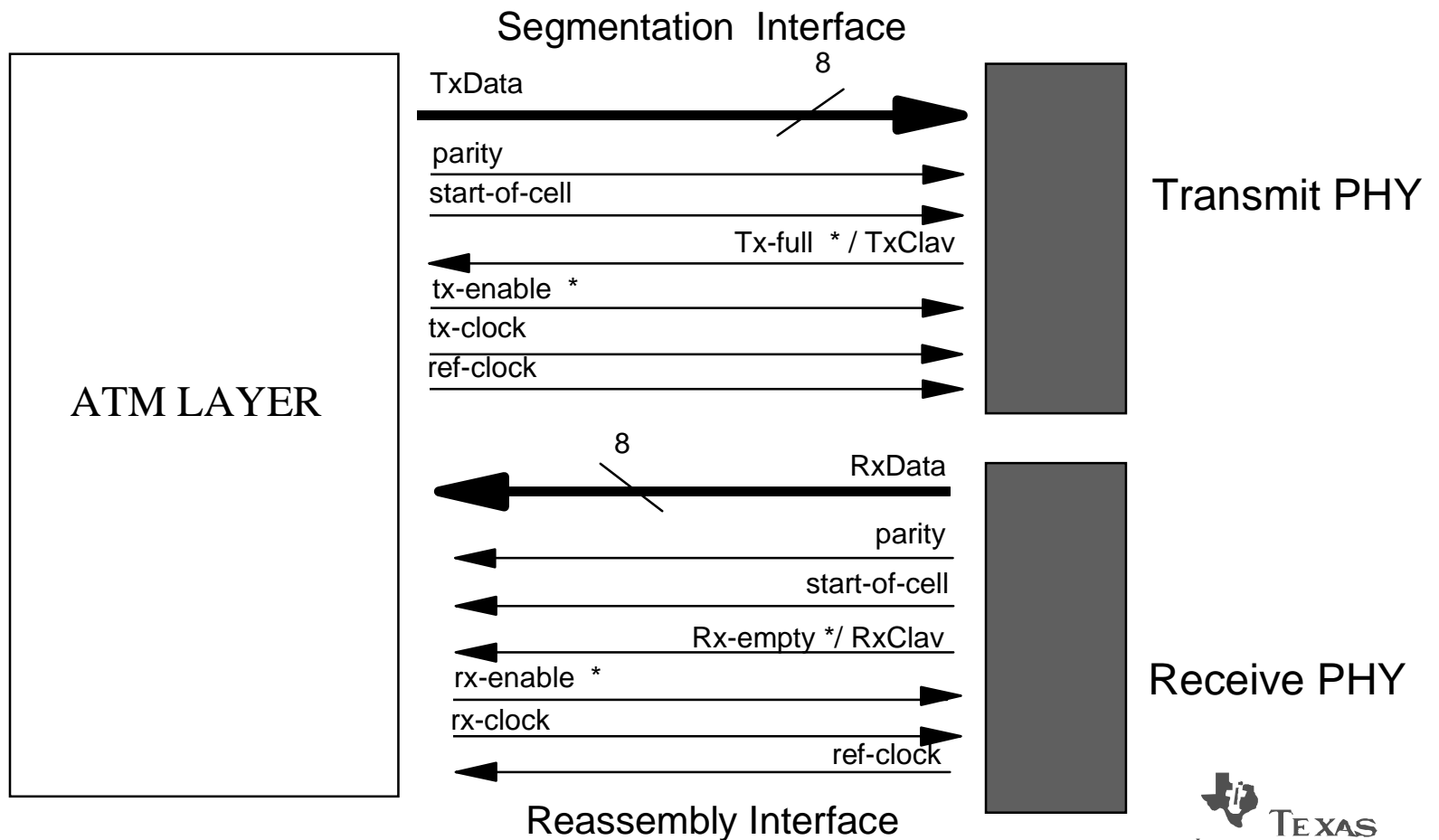
Control Memory Interface Block Diagram





ATM/PHY UTOPIA Interface Definition

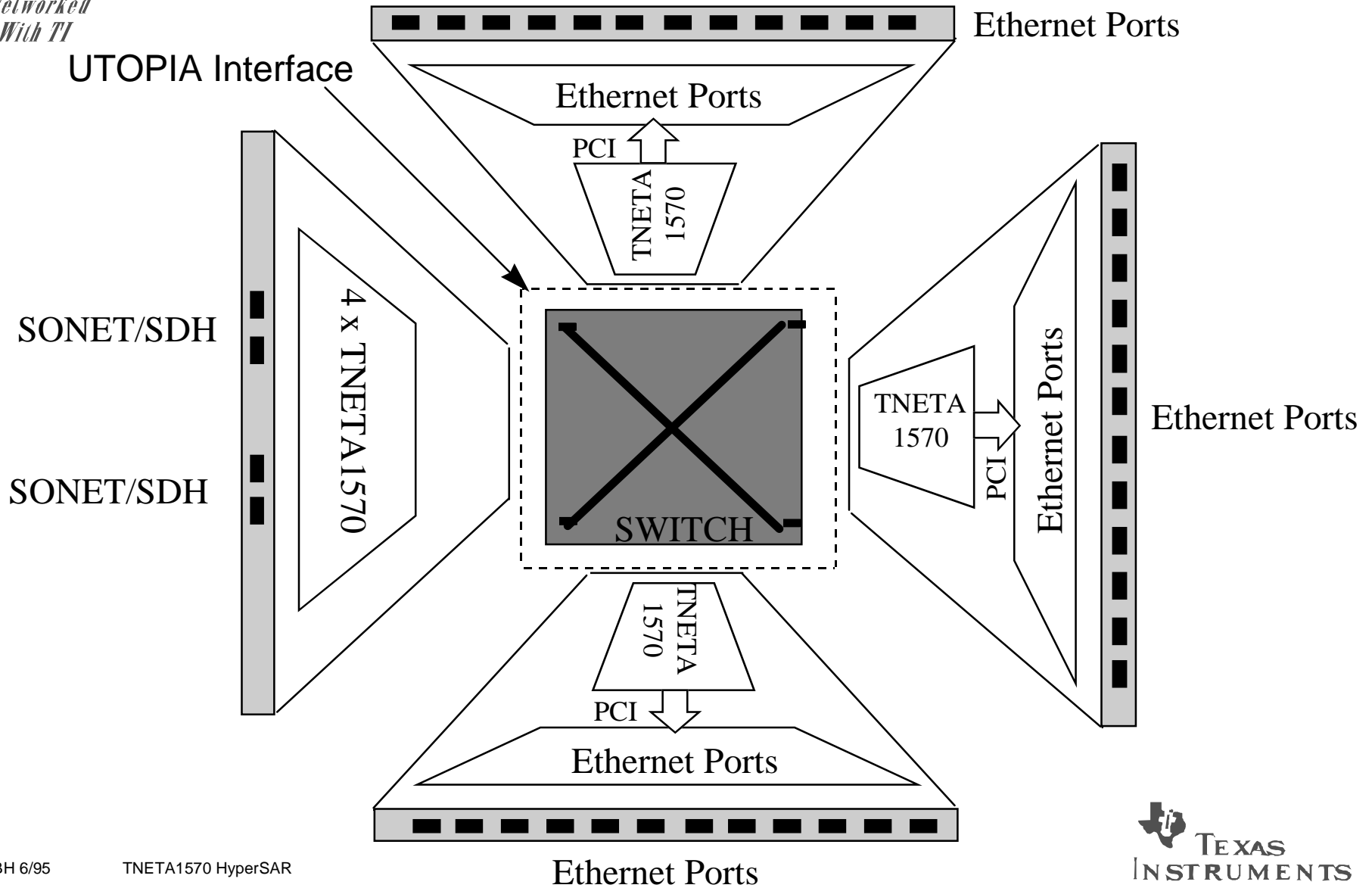
- Single pin to select between ATM/PHY modes.



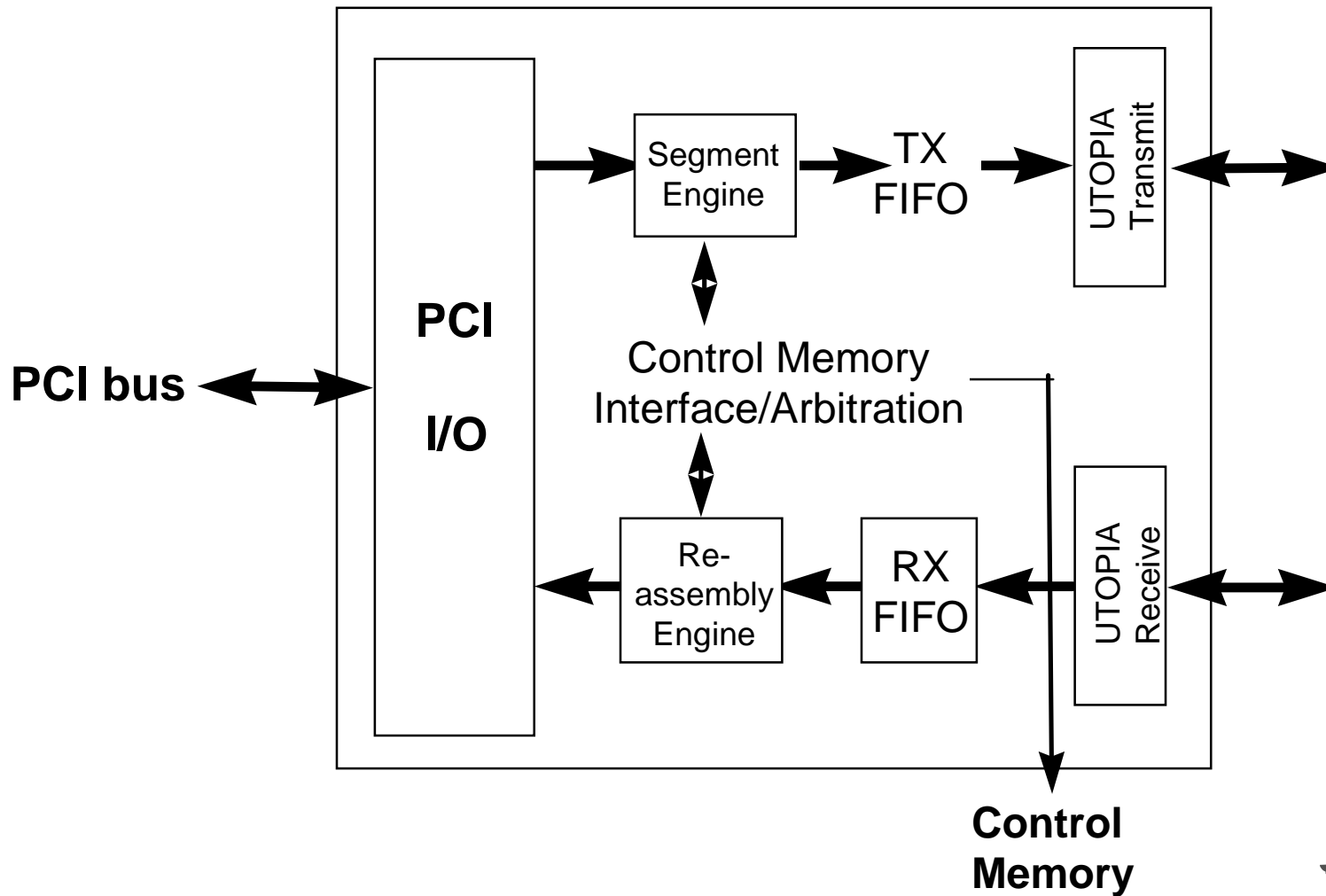


Networked
With TI

Interfacing to Local Switching Fabric



TNETA1570 Simplified Block Diagram





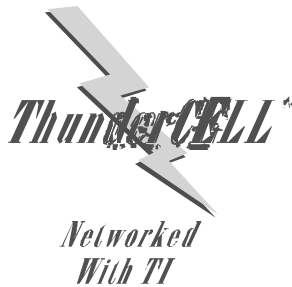
TNETA1570 HyperSAR Block Diagram

FEATURE

- Independent transmit and receive channels
- Segmentation based on buffers, not packets:
 - Allows early segmentation (cut-through capability)
- Control memory only used to store DMA state information
- Cells transferred directly from internal FIFOs to host memory and vice versa

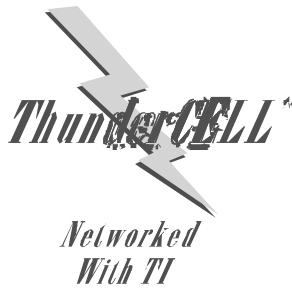
BENEFIT

- Provides full duplex operation and reduces internal thrashing of device
- Reduces latency (programmable buffer size 1 byte - 64 Kbytes)
- Improves performance by reducing accesses across PCI bus
- Improves performance by passing data directly to host



TNETA1570 Tools

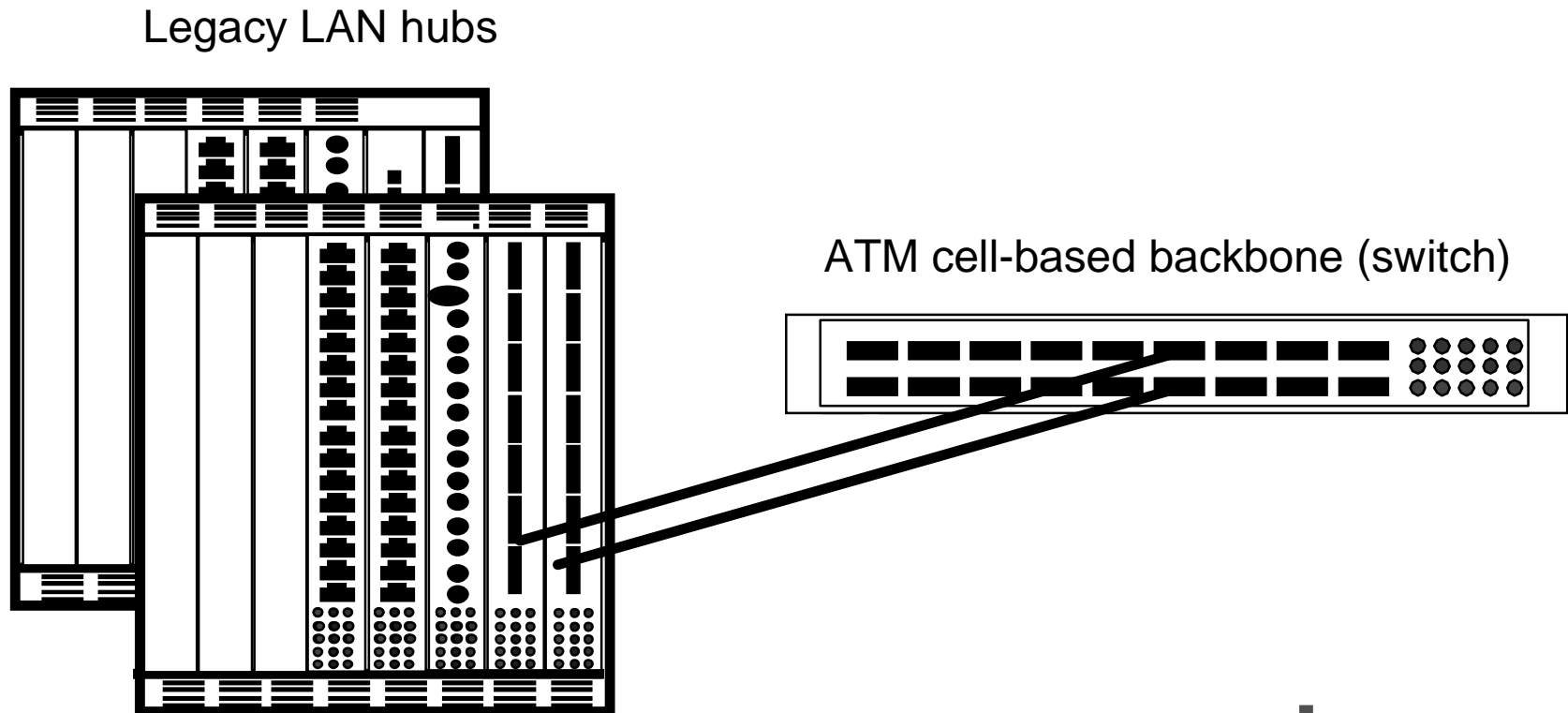
- **32-/64-bit PCI evaluation module**
 - Uses TNETA1570 and TNETA1500 SONET devices
 - Capability to exercise high-priority segmentation scheme
- **Windows-based software utility**
 - Transmits and receive ATM data
 - Monitors incoming traffic
 - Tries different configurations
 - Tests error and alarm conditions
- **Software drivers (third-party software)**
 - Provides turnkey solution of internetworking applications
 - Can work with any CPU
 - Improves time-to-market
- **Application note (1570/1500 interface)**

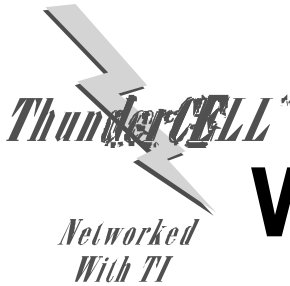


Applications

ATM Backbone

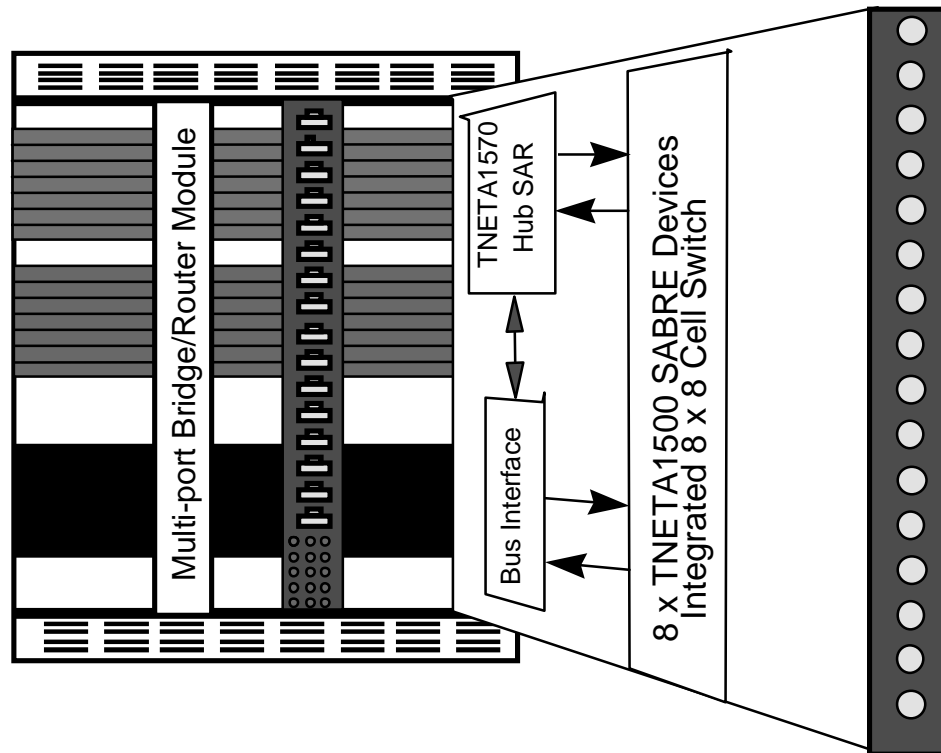
To connect to backbone switch, each HUB requires an ATM interface card.

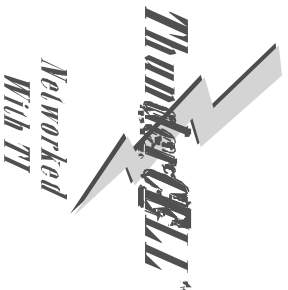




Enterprise Hub With Legacy LAN-based Backplane

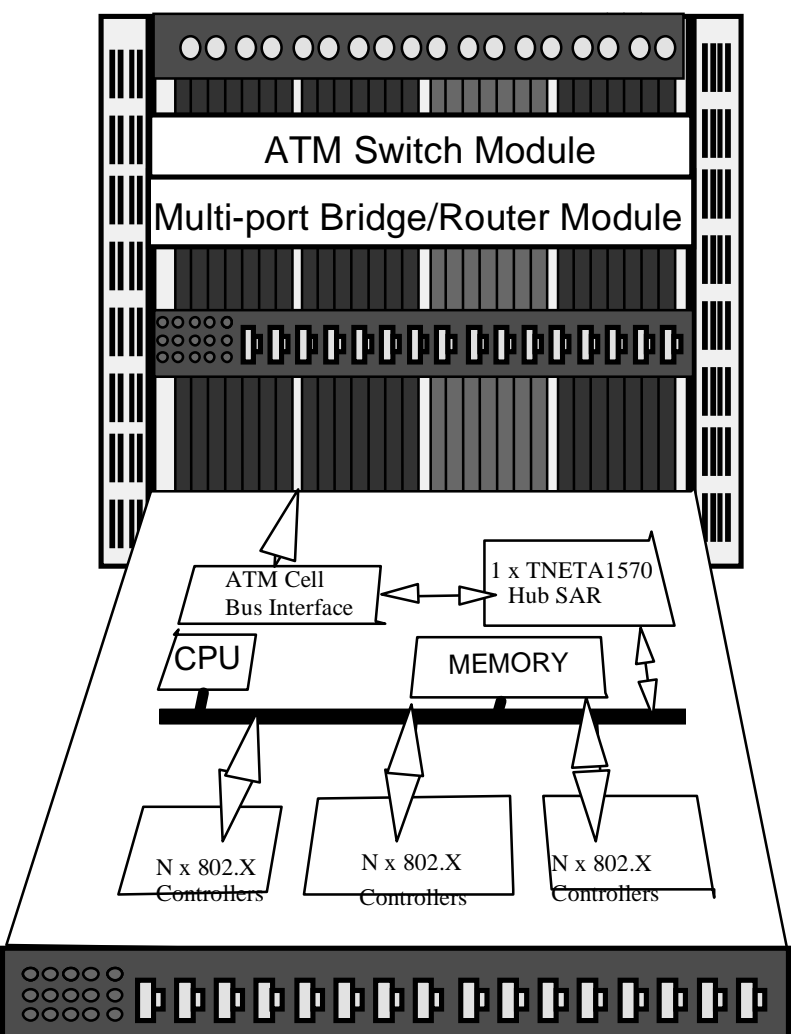
- Legacy LAN hub with ATM interface card
- Allows connection to backbone switch
- Provides interfaces for high-performance users

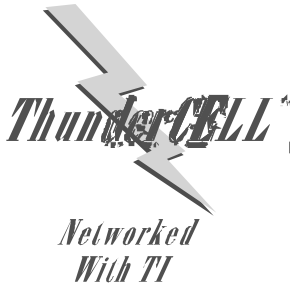




ATM Cell-based Backplane

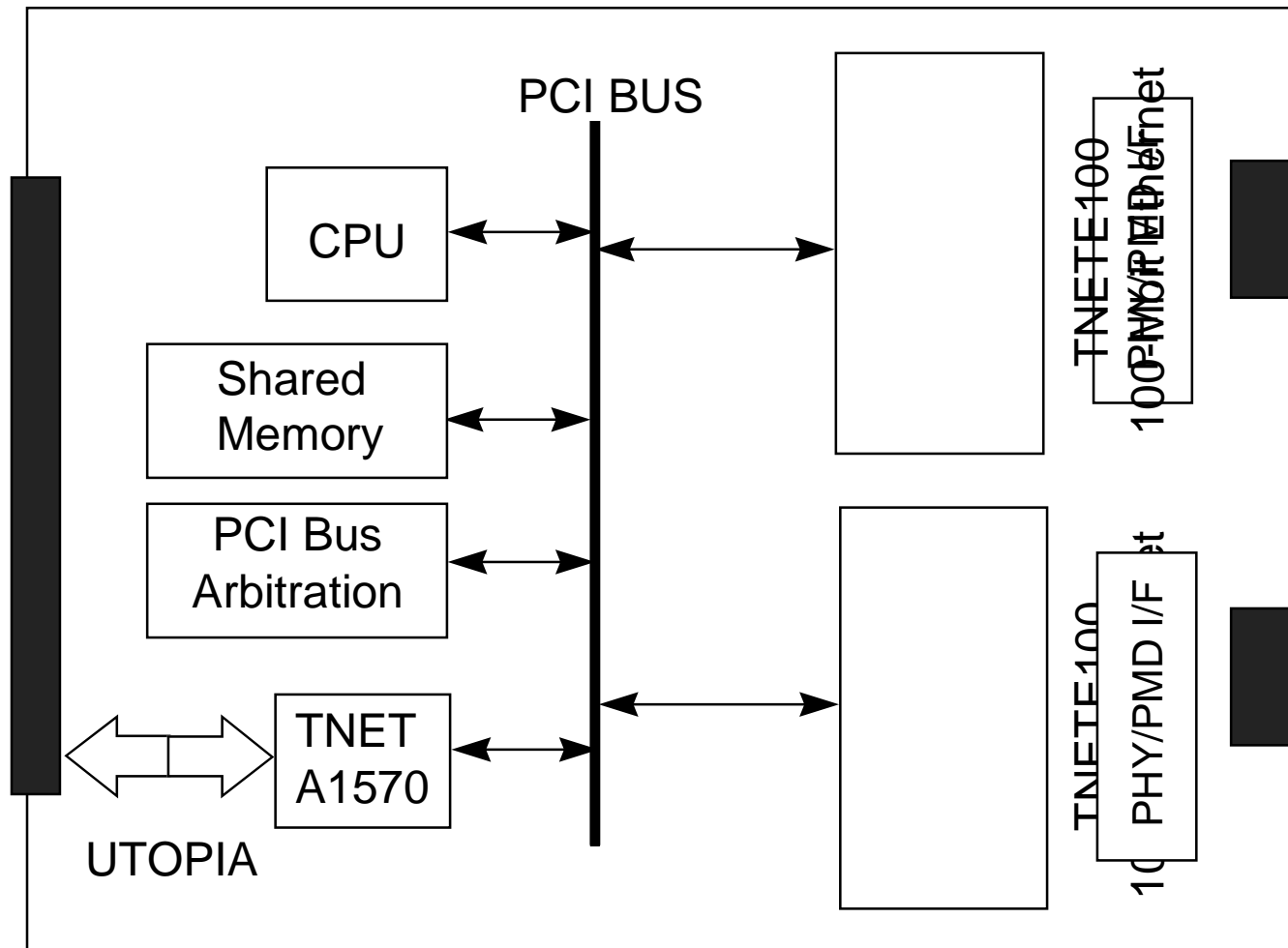
- More ATM backplanes are added.
- LAN backplanes move directly to interface cards.
- Hub can support switched virtual networks.



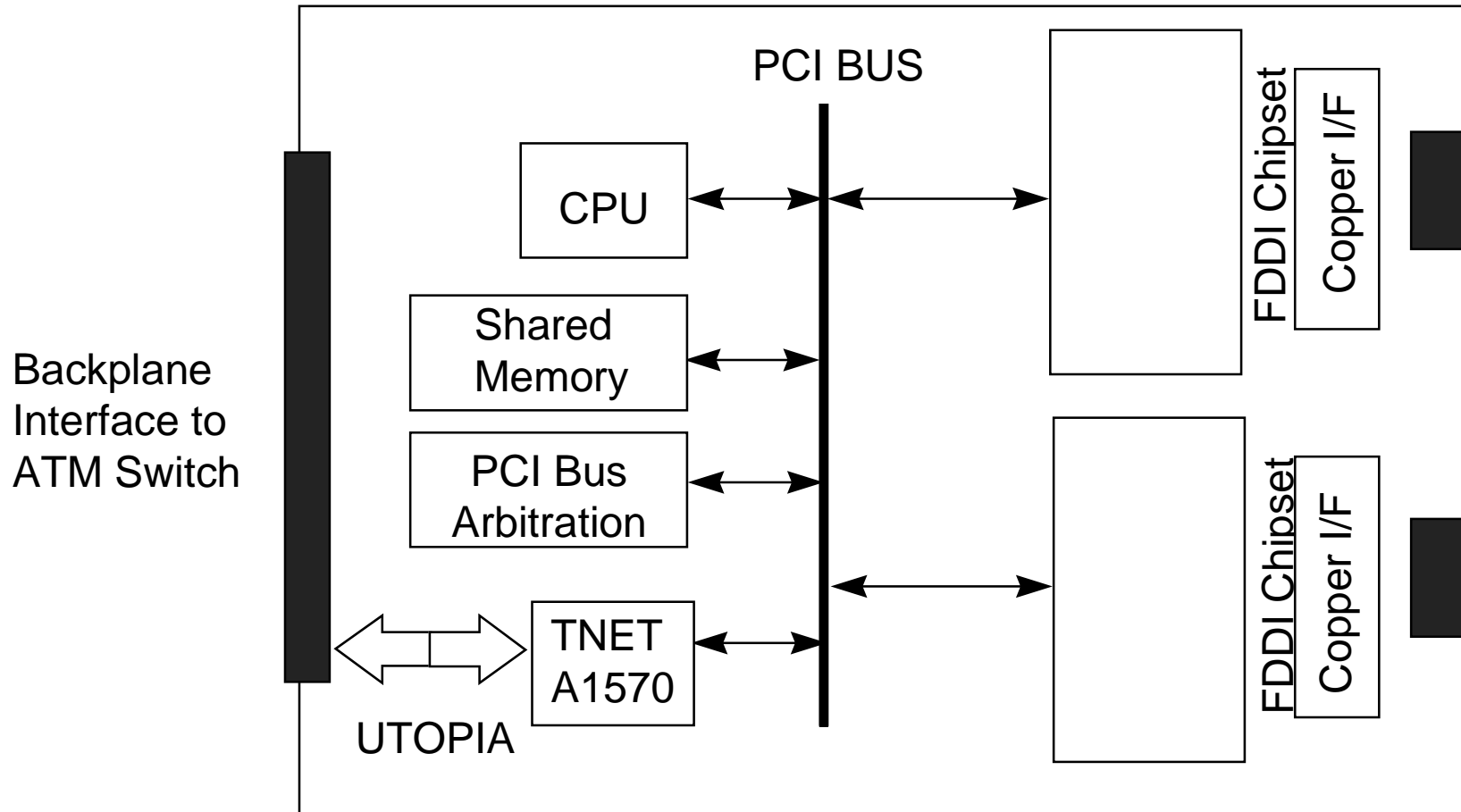


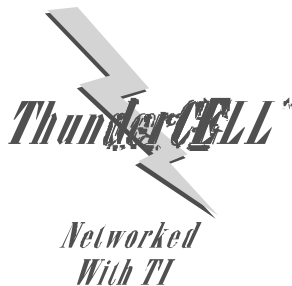
100Mbit/s Ethernet Interface Card

Backplane Interface to ATM Switch



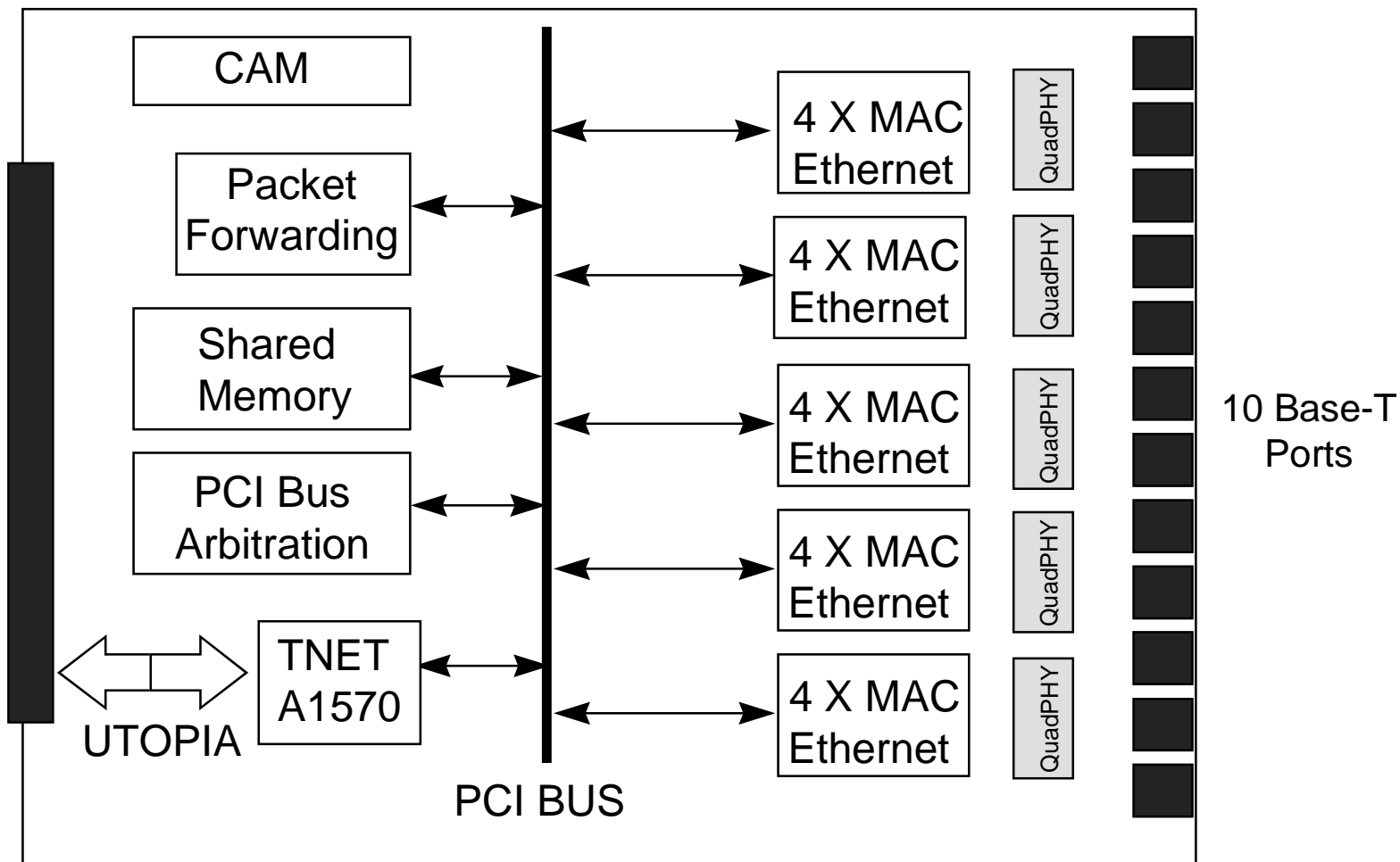
FDDI Interface Card

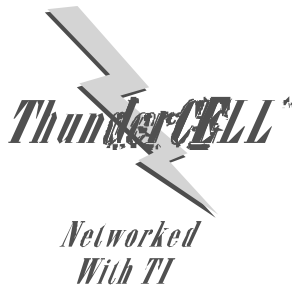




Switched/Dedicated Ethernet

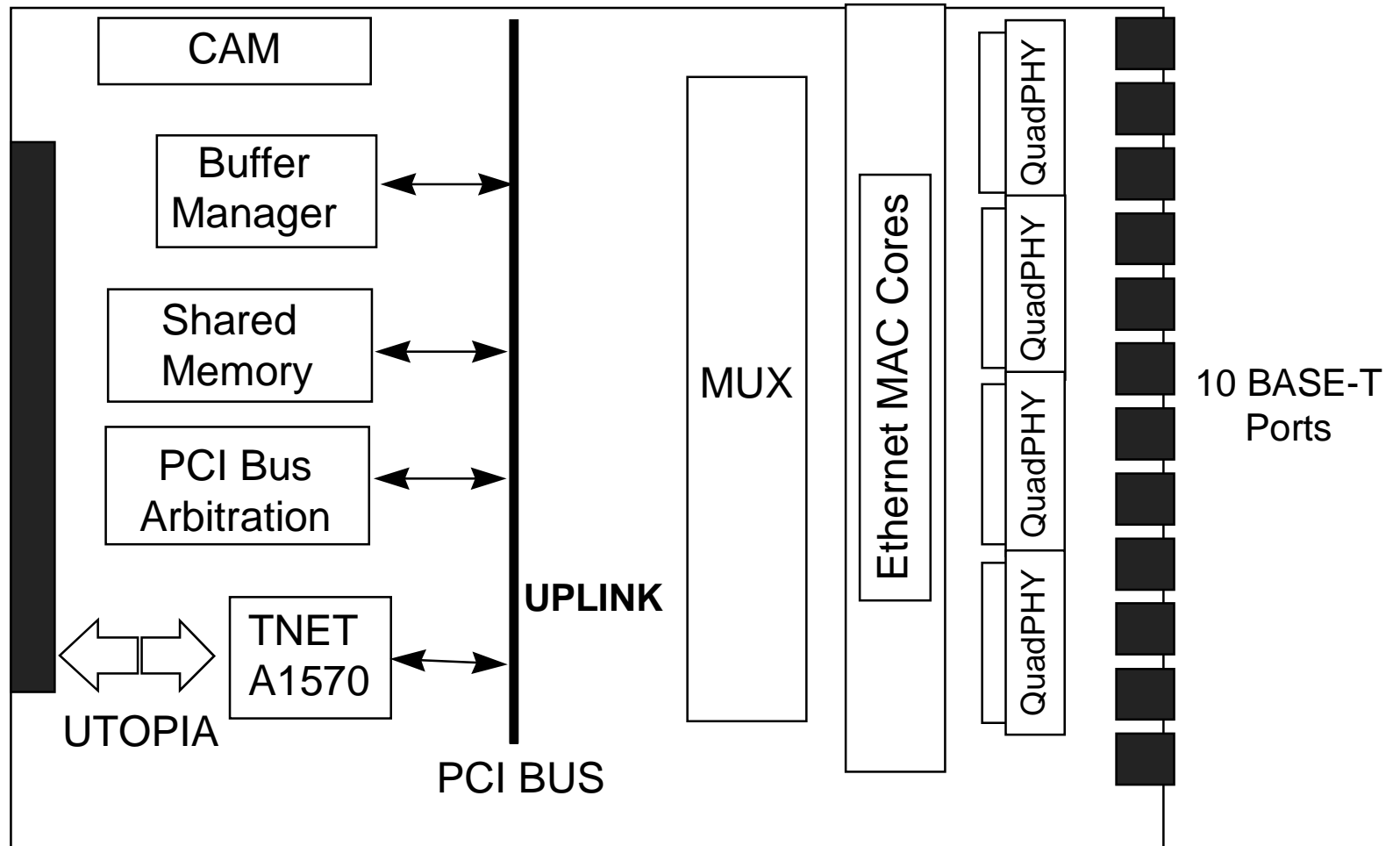
Backplane Interface to ATM Switch

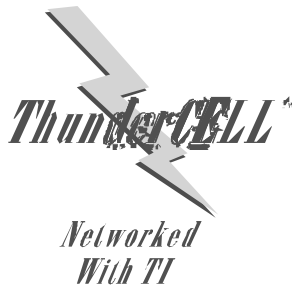




Switched/Dedicated Ethernet

Backplane Interface to ATM Switch





Summary

- **HyperSAR provides the highest performance solution for legacy LAN to ATM translation**
- **Samples available now**
- **Evaluation board and software available now**
- **S/W drivers for embedded systems also available (via third party) to reduce time-to-market**
- **Future proof (will provide upgrade to support ABR flow control)**