TI-RSLK MAX

Texas Instruments Robotics System Learning Kit

Texas Instruments

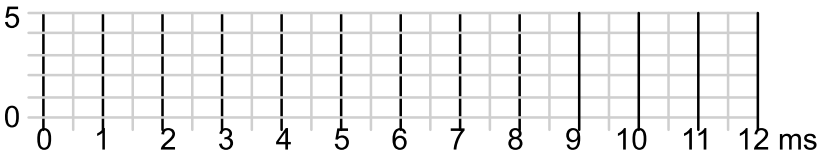
Module 18

Quiz: Serial Communication

Quiz: Serial Communication

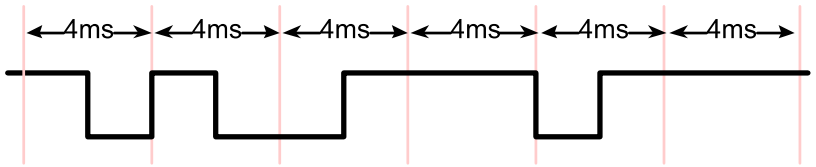
Q1 Serial protocol

Assuming the baud rate is 1000 bits/sec, draw the waveform on TxD as the data 0x27 is transmitted. Make the frame start at time = 1 ms.



Q2 Serial protocol

This was measured on RxD. Assuming it is one frame, what is the baud rate, and what is the data?



Q3 FIFO analysis

We will consider a number of scenarios for an input/output system using interrupts and FIFO buffering. For each scenario, classify the system as

1) I/O bound, meaning the bandwidth is limited by the speed of the I/O device. In other words, the bandwidth could be increased most by increasing the speed of the I/O device.
2) Well-balanced, meaning bandwidth is not limited specifically by either software execution speed or I/O speed.
3) CPU bound, meaning the bandwidth is limited by the speed of the software execution. In other words, the bandwidth could be increased most by increasing the speed of the software execution.

Part a) Consider an input device where an input data causes an interrupt and the data is put into a FIFO. The software in the main program gets data from the FIFO and processes the data. FIFO analysis yields the FIFO is usually empty.

Part b) Consider an input device where an input data causes an interrupt and the data is put into a FIFO. The software in the main program gets data from the FIFO and processes the data. FIFO analysis yields the FIFO is usually full.

Part c) Consider an output device where the software in the main program creates data and puts in into the FIFO. When the output device is idle it interrupts and the ISR gets data from the FIFO. The ISR writes data to the output device. FIFO analysis yields the FIFO is usually empty.

Part d) Consider an output device where the software in the main program creates data and puts in into the FIFO. When the output device is idle it interrupts and the ISR gets data from the FIFO. The ISR writes data to the output device. FIFO analysis yields the FIFO is usually full.

Q4 FIFO analysis

Consider an input device an input device where an input data causes an interrupt and the data is put into a FIFO. The software in the main program gets data from the FIFO and processes the data. Analysis shows the FIFO has an average of 10 data items in the queue. Assume you know data arrives into the system 1000 items per second. How long is the average response time (time from arrival of item until the time the item has been completed serviced).

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