Working with ADCs, OAs and the MSP430

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Agenda

• An Overview of the MSP430 Data Acquisition System

• SAR Converters
  ▪ The INS and OUTS of the SAR converter
  ▪ Useful Applications

• Using Op Amps
  ▪ Op Amp Configurations
  ▪ Driving SAR Converters
Where to Find ADCs and Op Amps

- Sensor Interface
- Voltage Reference Source
- Buffer
- Gain
- Difference Amplifier
- Instrumentation Amplifier
- Filter
- Level Shift

- Anti-Alias Filter
- Band-pass Filter
- Programmable Gain Amp
- Instrumentation Amp
- A/D Converter Driver

- Voltage Reference Source

- Actuator Driver
- Line Driver
- 4-20mA Driver

- Voltage Reference Source
- DDS Synthesis

- Microcontroller (μC)

- Power Amplifier

- Analog-to-Digital Converter (A/D)

- Digital-to-Analog Converter (D/A)
ADC Architectures

- There are many different ADC Architectures
  - Successive Approximation (SAR)
  - Sigma Delta (SD)
  - Slope or Dual Slope
  - Pipeline
  - Flash...as in quick, not memory

- All converters in the MSP430 chips are SAR and Sigma Delta types

- SAR determines the digital word
  - By approximating the input signal
  - Using an iterative process

- How the Sigma Delta converter determines the digital word
  - By oversampling
  - Applying Digital Filtering
Op Amp Architectures

• The Different Types Op Amp Architectures
  ▪ Single Supply
    – Rail to Rail In
    – Rail to Rail Out
    – CMOS or Bipolar
  ▪ Dual Supply

• All Op Amps (OAs) in the MSP430 chips are Single Supply, CMOS

• Our CMOS Op amp
  ▪ Easily Configured with the MSP430 Controller
    – General Purpose, Buffer, Comparator, PGA, Differential Amp
  ▪ Easily Programmed for
    – Optimized Gain
    – Bandwidth
    – etc
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The SAR ADC

• Most Serial ADCs are SARs or Sigma Deltas

• The MSP439 SAR Converter
  ▪ SAR ADC = Successive Approximation Register, Analog-to-Digital Converter
  ▪ ADC12 – 12-bit Analog-to-Digital Converter

• SARs are Best for General Purpose Apps
  ▪ Very Prevalent for Signal Level Applications: Data Loggers, Temp Sensors, Bridge Sensors, General Purpose

• In the Market SARs
  ▪ Can be 8 to 18 bits of resolution
  ▪ Speed range: >10 ksps to < 5 Msps

• Usually require a Low-pass Filter before Analog Input
System Integration Using an A/D

- Input Signal Source
- Amplifier (Amp)
- Filter
- SAR Analog to Digital Converter
- Micro-Controller Engine
- Output
- Filter
- DAC or PWM

MSP430

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SAR Converter – Block Diagram

Cap array is both the sample cap and a DAC

Shift Register

Control Logic

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Successive Approximation Concept

Analog input

Vin

3/4FS

1/2FS

1/4FS

0

FS

DAC Output

Digital Output Code = 1010

Time

Bit = 1

Bit = 0

Bit = 1

Bit = 0

TEST MSB

TEST MSB -1

TEST MSB -2

TEST LSB
ADC Ideal Transfer Function

Digital Output Code

Analog Input Voltage

Ideal transfer function
ADC with Offset and Gain Error

- $y = a + (1+b)x$
  - where
  - $y =$ digital out
  - $x =$ analog in
  - $a =$ offset err
  - $b =$ gain err

- Every Ideal Code has Offset Error added
- Every ideal code is Multiplied by Gain Error
Offset/Gain Impact on Dynamic Range

- **ADC12 specifications**
  - Offset
    - $E_O \text{ typ} = \pm 2 \text{ LSB}$
    - $E_O \text{ max} = \pm 4 \text{ LSB}$
  - Gain
    - $E_G \text{ typ} = \pm 1.1 \text{ LSB}$
    - $E_G \text{ max} = \pm 2 \text{ LSB}$
      ($= \pm 0.0488\%$)
    - $1 \text{ LSB} = (V_{R+} - V_{R-})/ 2^{12}$
    - Easy to calibrate

**Gain Error**

**Offset Error**

Worse case

Dynamic Range = 4082 bits = 11.995 bits

Analog Voltage IN $\rightarrow V_{\text{REF}}$

Digital Code OUT $\rightarrow 4096$
DNL and INL Errors

- **Ideal transfer function**
- **Actual transfer function**

INL < 0

DNL < 0

Digital Output Code

Analog Voltage In

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INL/DNL/Noise Impact on Dynamic Range

- **ADC12 specifications**
  - DNL error
  - $E_D \text{ max } = \pm 1.7 \text{ LSB}$
  - INL error
  - $E_I \text{ max } = \pm 1 \text{ LSB}$
  - $1 \text{ LSB } = (V_{R+} - V_{R-})/2^{12}$

- **INL, DNL and Noise errors move across the entire range**

- **Impacts the Effective Number of Bits (ENOB)**

- **Not Easily calibrated**

- **Effects Accuracy**
ADC Input Impedance

- Input Internal Impedance is Relatively Low
- A High Impedance Source Increases Sample Cap Charging Time
- Rise Time of Voltage on CI \( \sim (RS + RI) \times CI \)

\begin{align*}
R_S &= 2k \Omega \\
C_I &= 40pF
\end{align*}
Sample Cap Charging Time

1400 ns (min) Sample Period

Conversion Complete

Desired Voltage on $C_I$

Final Voltage on $C_I$

Rise Time of $(R_S + R_I) \times C_I$

$V_C$

SAMPCON

ADC12OSC/ADC12DIV

ADC12MEMX

Start Conversion

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Alternative High Resolution Devices

• ADC12
  ▪ Resolution = 12 bits
  ▪ Minimum LSB size = VREF / 2^n = 1.5 V / 2^12 = 366 mV
  ▪ # channels = 12 to 16 (depends on part number)

• ADS8341
  ▪ Resolution = 16 bits
  ▪ Minimum LSB size = VREF / 2^n = 2.7 V / 2^16 = 41.2 mV
  ▪ # channels = 4

• ADS1100
  ▪ Resolution = 16 bits
  ▪ Minimum LSB size = VREF / 2^n = 2*2.7 V / 2^16 = 82.4 mV
  ▪ # channels = 1
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Operational Amplifiers

- Most Prevalent Building Block in Analog Circuits
- Very Flexible - Large Variety of Functions

Circuits We Will Talk About
- General Purpose Op amp
- Unity Gain Buffer
- Comparator
- PGA (Programmable Gain Amplifier)
- Differential Amplifier
Where to Find Op Amps

- Sensor Interface
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- A/D Converter Driver

- μC

- DDS Synthesis

- Forks

- Valve
Ideal Op Amp

**POWER SUPPLY**
- No min or max Voltage
- $I_{\text{SUPPLY}} = 0$ Amps
- Power Supply Rejection = $\infty$

**OUTPUT**
- $V_{\text{OUT}} = V_{\text{SS}}$ to $V_{\text{DD}}$
- $I_{\text{OUT}} = \infty$
- Slew Rate = $\infty$
- $Z_{\text{OUT}} = 0 \ \Omega$

**INPUT**
- Input Current ($I_{\text{B}}$) = 0
- Input Impedance ($Z_{\text{IN}}$) = $\infty$
- Input Voltage ($V_{\text{IN}}$) → no limits
- Zero Noise
- Zero DC error
- Common-Mode Rejection = $\infty$

**SIGNAL TRANSFER**
- Open Loop Gain = $\infty$
- Bandwidth = 0 → $\infty$
- Zero Harmonic Distortion

$0.00$

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Open Loop vs Closed Loop Design

- OAFCx = 011

- Open Loop Configuration
  - In Comparator mode

- OAFCx = 000

- Closed Loop Configuration
  - Always a Connection from Output to Inverting Input
  - Gain is Dependant on Resistors

\[ V_{OUT} = (1 + \frac{R_F}{R_IN}) \times V_{IN} \]

\[ V_{OUT} = \text{High for } V_{IN} > V_{REF} \]
\[ V_{OUT} = \text{Low for } V_{IN} < V_{REF} \]
Comparator Mode – OAFCh = 011

Temperature Sensor

\[ V_A(t) \]

\[ R_{\text{NTC}} || R_{\text{PAR}} \]

\[ R_{\text{REF}} \]

\[ V_{\text{TH}} \]

\[ t = 0 \quad t = t_1 \quad t = t_2 \]

Time

\[ \frac{R_{\text{NTC}} || R_{\text{PAR}}}{R_{\text{REF}}} = \frac{t_{\text{NTC}} || R_{\text{PAR}}}{t_{\text{REF}}} \]

Comparator Mode – OAFCh = 011

Temperature Sensor

\[ V_A(t) \]

\[ R_{\text{NTC}} || R_{\text{PAR}} \]

\[ R_{\text{REF}} \]

\[ V_{\text{TH}} = 0.25V_C \]

\[ \text{Comparator} \]

\[ \text{Timer} \]

\[ C_{\text{INT}} \]

MSP430FG43x

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General Op amp Mode – OAFCx = 000
General Op amp Mode – OAFCx = 000

Non-inverting Gain

\[
V_{OUT} = V_{IN} \left(1 + \frac{R_F}{R_{IN}}\right) - V_{REF} \cdot \frac{R_F}{R_{IN}}
\]
General Op amp Mode – OAFCx = 000

Inverting Gain

\[ V_{\text{OUT}} = V_{\text{REF}} \left(1 + \frac{R_F}{R_{\text{IN}}}\right) - V_{\text{IN}} \frac{R_F}{R_{\text{IN}}} \]

\[ V_{\text{REF}} = 0.5V_{\text{CC}} \]
Data Acquisition System

- Analog Gain and Signal Conditioning Cell
- Analog Low Pass Filter (LPF)
- Analog to Digital Conversion (ADC)
- Digital Filter

Input Signal Analog → Analog Gain and Signal Conditioning Cell → Analog Low Pass Filter (LPF) → Analog to Digital Conversion (ADC) → Digital Filter → Output Signal Digital
Noise Reduction with a Low Pass Filter

Noise Reduction or Anti-aliasing Filter

\[ V_{IN} \]
\[ R_{21} \]
\[ R_{22} \]
\[ R_{23} \]
\[ C_{21} \]
\[ C_{22} \]
\[ V_{REF} \]
\[ OA \]
\[ ADC12 \]
**Anti-alias Filter :: Nyquist Theorem**

- **Signal at the Input of the A/D Converter**
  - \( f_{ALIASED} = |f_{IN} - N f_S| \)
  - Find \( N \) by making \( f_{ALIASED} < f_s / 2 \)

- **Digital Representation at the Output of the Converter**

**Diagram**

- **Analog Input**
  - \( N = 0 \)
  - \( N = 1 \)
  - \( N = 2 \)
  - \( N = 3 \)
  - \( N = 4 \)

- **Sampled Output Representation**
  - \( N = 0 \)
  - \( N = 1 \)
  - \( N = 2 \)
  - \( N = 3 \)
  - \( N = 4 \)

- **Frequency Points**
  - \( 0 \)
  - \( f_s / 2 \)
  - \( f_s \)
  - \( 2f_s \)
  - \( 3f_s \)
  - \( 4f_s \)
  - \( 5f_s / 2 \)
  - \( 7f_s / 2 \)
Filter Pro Software

• **Filter synthesis tool for designing**
  - Multi-section filter
  - Low-pass Filter
  - High-pass active filter

• **Supports**
  - 2nd to 10th order
  - Multiple-feedback (MFB) Filter Topology
  - Sallen-Key Filter Topology

• [www.ti.com](http://www.ti.com)
Operational Amp Output Swing

- Rail-to-Rail Output Operation does not Exist
- How Close the Amplifier’s Output can Come to the Power Supplies (or “rails”) and still be Linear
- MSP430FG43x = \((VSS + 200\text{mV})\) {min} to \((VCC - 200\text{mV})\) {max}

\[
V_{OUT} = \left(1 + \frac{R_F}{R_{IN}}\right) V_{IN}
\]
Operational Amp Output Swing

Offset Voltage, $V_{os}$ (mV)

Output Voltage, $V_{OUT}$ (V)

Offset Voltage, $V_{os}$ (mV)

Output Voltage, $V_{OUT}$ (V)

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Unity Gain Buffer Mode – OAFCx = 001

- Op Amp Internally connected as a buffer
- Non-inverting input available on a Controller pin
- Op Amp Output connected directly to ADC12
Op Amp Input Voltage Range

- **RRIP ON =**
  
  \((VSS - 0.1V) \{\text{min}\} \text{ to } (VCC + 0.1) \{\text{max}\}\)

- Charge pump on input stage is turned on
- Great Feature, not all amps have this!

- **RRIP OFF =**
  
  \((VSS - 0.1V) \{\text{min}\} \text{ to } (VCC - 1.2) \{\text{max}\}\)

- (Appropriate for Gains > 2)
PGA Mode –
Non-inverting Mode OAFCx = 100

\[ V_{OUT} = G \times V_{IN} \]

MSP430FG44x

DACs or external

V_{IN}

Ax int/ext

V_{OUT}

R_{BOTTOM}

R R R R R

2R 2R 4R 4R

R_{TOP}

AV_{SS}

RRIP on

RRIP off

OAxCCTL1

111100x1 G=16
110100x1 G=8
101100x1 G=3.33
100100x1 G=4
011100x1 G=2.67
010100x1 G=2
001100x0 G=1.33
000100x0 G=1

PGA Non-inverting

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PGA Mode – Inverting Mode OAFCx = 110

\[ V_{OUT} = G \cdot V_{IN} + V_{REF}(1 - G) \]

**MSP430FG44x**

**OAxCCTL1**
- 111110x1  G=-15
- 110110x1  G=-7
- 101110x1  G=-4.33
- 100110x1  G=-3
- 011110x1  G=2.67
- 010110x1  G=-1.67
- 001110x1  G=-1
- 000110x0  G=-0.33

**RRIP on**

**RRIP off**

**PGA Inverting**

**VOUT**

**IN**

**REF**

**TOP**

**BOTTOM**

**DACs or external**
Bridge Network

INA326
\[ G = 2 \left( \frac{R_2}{R_1} \right) = 245 \]

LCL-816G

V_{REF1}

R_{L1} R_{L2} R_1

R_2

C_1

OA

V_{REF2}

R_{21} R_{22} R_{23}

C_{21} C_{22}

SAR – ADC
12 bits

MSP430FG43x

μController
Functions

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Summary

• **12-bit SAR Converter – ADC12**
  - 12-bit Resolution and Accuracy
  - Excellent Dynamic Range
  - For more Resolution – Discrete Options

• **Operational Amplifier – OA**
  - Standard Single Supply CMOS Op Amp
  - Rail-to-rail Input
  - Rail-to-rail Output
  - Six Configurations or Modes
  - For more Accuracy – Discrete Options
  - For more Complexity – Discrete Options

• **MSP430 Analog Options – Very Useful!**
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