Outline

• Transport Layer Details
• Link Layer Details
Transport Layer Overview

- Maps the data → octets → frames consisting of multiple octets
- Adds optional control bits to samples if needed
  - Control bits can be used to communicate status information, mark an inactive converter on the link or control receiver operation
- Adds tail bits if needed to create ‘full’ octets
- Distinguishes the possible combinations of device/links/lanes/etc.
  - Single converter connected to single lane link
  - Single converter connected to multiple lanes link
  - Multiple converters in a converter device connected to a single lane link
  - Multiple converters in a converter device connected to multiple lanes link

TI Information
- NDA Required
Transport Layer Data Flow

Converter device, $M \times N$ bits, $S$ samples per single converter per frame cycle

- Converter 0
- Sample 0
- Sample 1
- Sample $S-1$
- Converter $j$
- Sample 0
- Sample $S-1$
- Converter $M-1$
- Sample 0
- Sample $S-1$

Control bits appended to each sample ($CF=0$) or mapped into $CF$ separate control words ($1 \leq CF \leq L$)

- Word 0
- Word 1
- NG 0
- NG 1
- TT

Words padded with tail bits to nibble groups NG. Sample NGs contain $N'$ bits.

- Octet $N/4-1$
- Octet $F-1$
- Octet $j \times F$
- Octet $(j+1) \times F-1$
- Octet $(L-1) \times F$
- Octet $L \times F-1$

- Lane 0
- Lane $j$
- Lane $L-1$

Texas Instruments
Transport Layer (Example #1)

Mapping Converter Samples to Frames

- **N=11** Converter Resolution
- **N'=13** Number of bits in Sample plus control bits
- **CS=2** Control bits per sample
- **RBD=** User Defined
- **K=** User Defined
- **L=4** Lanes per Device
- **F=4** Octets per Frame (per lane)

<table>
<thead>
<tr>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 0 [10:3]</td>
<td>Core 0 [2:0]</td>
<td>Core 1 [10:3]</td>
<td>Core 1 [2:0]</td>
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<tr>
<td>Core 2 [10:3]</td>
<td>Core 2 [2:0]</td>
<td>Core 3 [10:3]</td>
<td>Core 3 [2:0]</td>
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<tr>
<td>Core 6 [10:3]</td>
<td>Core 6 [2:0]</td>
<td>Core 7 [10:3]</td>
<td>Core 7 [2:0]</td>
</tr>
</tbody>
</table>

Octet 0 | Octet 1 | Octet 2 | Octet 3

1 Frame

- **M=8** Converters per Device
- **S=1** Samples per Frame (per converter)

Texas Instruments
Transport Layer

• Some important parameters associated with transport layer are:
  
  – L  Number of lanes in a link
  – M  Number of converters per device
  – F  Number of octets per frame
  – S  Number of samples per converter per frame clock cycle
  – K  # of frames per multiframe
  – CF Number of control words per frame clock cycle per link
  – N  Converter Resolution
  – N’ Total number of bits per sample

• Control bits can either be appended after the LSB of every sample or all the bits for different samples can be sent together in CF number of frames.
Example #2 (16b Quad ADC)

What is the “LMFK” for this link?
L = 4, M = 4, F = 8, K = 4

What is “S”?
S = 4
LINK LAYER
Link Layer Functions

• 8b/10b Encoding
• Link Synchronization
  – Code group synchronization
  – Initial frame synchronization
  – Initial lane synchronization
  – Link re-initialization
• Link Monitoring
  – Special alignment character insertion
  – Error Reporting
• SYNC~ signal combining
• Test Modes
Link Layer: 8b/10b Encoding

- Encodes 8-bit “octets” into 10-bit symbols
- Octet to symbol mapping depends on running disparity (RD)
- Coding provides many bit-transitions to enable CDR techniques
- DC balancing enables AC coupling
**Link Layer: Link Establishment**

- Link Establishment accomplishes TX and RX synchronization
  - Code Group Synchronization (CGS)
  - Initial Frame Synchronization
  - Initial Lane Synchronization
Link Layer: Code Group Synchronization

• During CGS, the RX aligns with the 10-bit symbol boundary of the transmitted symbols

• Synchronization Procedure:
  1. Receiver generates synchronization request by asserting SYNC~ signal
  2. In response, transmitter sends K28.5 comma symbols
  3. After receiving 4x K28.5 symbols on all lanes, the RX de-asserts SYNC~
  4. RX aligns frame boundary to next non-K28.5 symbol (Initial Frame Synchronization)

• If link has multiple lanes, then SYNC~ signal for all lanes in a link must be combined and presented simultaneously to the transmitter
Link Layer: Initial Lane Synchronization

- Lanes are synchronized using initial lane alignment (ILA) sequence
- TX transmits ILA on next multi-frame boundary following CGS

ILA is 4 multi-frames minimum, containing configuration parameters and alignment symbols (A)
ILA is never scrambled, even if scrambling is enabled
ILA information may be verified by the Rx, or it can be ignored if the Rx already expects a certain format
Link Layer: Frame Alignment Monitoring

• Transmitter sends out user data after ILA sequence
• Alignment characters are inserted into data stream in special conditions to re-check alignment
  – If last octet in 2 successive frame are equal → transmitter replaces latter octet with K28.7 symbol (scrambling disabled)
  – If last octet of a multi-frame is equal to last octet in previous frame → replace latter octet with K28.3 symbol
• Receiver “undoes” the special character replacement
• Receiver will re-align it’s frame clock to alignment characters under certain conditions
• **Texas Instruments** converter devices support both the monitoring and correction of lane alignments
Error Reporting

- Standard lists the following errors to be detected by each receiver.
  - 8B/10B disparity error
  - 8B/10B not-in-table code error
  - Control character in wrong position
  - Code Group Synchronization error

- Texas Instruments JESD204B DAC core also generates RX errors
  - Multiframe alignment error
  - Frame alignment error
  - Elastic buffer overflow (indicative of bad RBD value)
  - Link configuration error (TX and RX parameters do not match)
  - Some of the errors can be made to retrigger the synchronization request as specified by setting the corresponding bit in `sync_req_ena` configuration parameter

TI Information – NDA Required
JESD204B Link Errors

• Elastic Buffer Overflow
  – Occurs when any of the RX lane buffers overflow before all the buffers have received their first non-/K28.5/ character

• Link Configuration mismatch
  – Occurs when the link configuration data sent in the 2nd multi-frame during ILA does not much the programmed RX configuration

• Frame alignment error
  – Occurs when /A/=/K28.3/ alignment char found but not at end of frame

• Multi-frame alignment error
  – Occurs when /F/=/K28.7/ alignment char found, but not at end of multi-frame

• 8b/10b disparity error
  – Occurs when received character is not consistent with running disparity

• 8b/10b not in table
  – Received 10-bit character is not found in the 8b/10b character table
Link Re-Initialization

• Under certain error conditions data receiver will request re-initialization of the link by asserting SYNC~

• Upon receiving the SYNC~ request, the transmitter device will start sending /K/ (K28.5) symbols

• A transmitter may also request re-initialization of the link by moving its state machine to the SYNC state and emitting a stream of /K/ symbols

• Minimum duration of SYNC~ request is defined by the standard to ensure a sufficiently long stream of /K/ symbols
Link Layer Test Modes

• Link layer test modes consist of predetermined sequences of 8b/10b characters that are transmitted in all frames and on all lanes of a multi-point link.

• Link layer test characters are specified as if injected directly to the 8b/10b encoder and are never scrambled.

• Link layer test modes required by JESD204B standard:
  – Continuous /D21.5/: high frequency pattern useful for random jitter (RJ) or receiver eye mask testing.
  – Continuous /K28.5/: medium frequency pattern useful for deterministic jitter (DJ) testing.
  – Repeated ILA sequence.
  – One of the following:
    • Continuous sequence of modified random pattern (modified RPAT).
    • Continuous sequence of a scrambled jitter pattern (JSPAT).
Link Layer Test Modes

- All receiver devices must be able to verify the following:
  - A continuous sequence of \(/K28.5/\) symbols for CGS
- Most devices must also support a CGS sequence followed by repeated ILA sequence
- All RX devices must also have the capability to suppress error reports due to a missing ILA
  - This feature enables BER measurements using standard test equipment which output 8b/10b encoded test patterns after initial synchronization with a K28.5 sequence
  - Most of the bit errors will lead to running disparity or not-in-table errors which will be evident by the RX asserting the SYNC~ interface
  - This allows the SYNC~ assertion to be used as a relatively accurate method for BER determination
- Additional test modes may be included in the TX physical layer
SYNC~ Signal Combining

- For a multi-lane link between an RX and TX device, the synchronization requests of all receivers are combined and presented simultaneously to the TX device.

- On multi-point links (one TX to multiple RX or multiple TX to one RX) the synchronization requests may be combined but it is not mandatory.

Figure 33 — Examples of SYNC~ signal combination
SYNC~ Signal Combining (cont’d)

Figure 34 — Examples of non-combined SYNC~ signaling
Summary

• Transport Layer defines the mapping of data → octets → frames and is summarized by the transport layer parameters (LMFS, etc.)

• Link Layout primarily consists of definitions for 8b/10b encoding, Link Synchronization and Link Monitoring

• The link synchronization sequence includes
  – Code group synchronization (CGS)
  – Initial frame synchronization
  – Initial lane synchronization (ILA)

• A variety of link errors are detected which may be reported over the SYNC~ interface or may trigger link re-synchronization
More Educational Resources

www.ti.com/lstic/ti/dataconverters/high-speed-adc-greater-10msps-jesd204b.page
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