JESD204B Overview

Texas Instruments High Speed Data Converter Training
Outline

• JESD204B Standard at a Glance
• Benefits / Cost
• Timing Signals
• Layers Overview (Transport, Link, Physical)
• Deterministic Latency
• Subclasses
JESD204B Standard at a Glance

- A standardized serial interface between data converters (ADCs and DACs) and logic devices (FPGAs or ASICs)

- Serial data rates up to 12.5 Gbps

- Mechanism to achieve deterministic latency across the serial link

- Uses 8b/10b encoding for SerDes synchronization, clock recovery and DC balance

- JESD204B is a must for high density systems!
## JESD204B Standard at a Glance

<table>
<thead>
<tr>
<th>Feature</th>
<th>JESD204</th>
<th>JESD204A</th>
<th>JESD204B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Lane Rate</td>
<td>3.125 Gbps</td>
<td>3.125 Gbps</td>
<td>12.5 Gbps</td>
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<tr>
<td>Multiple Lane Support</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Multi-Lane Synchronization</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Multi-Device Synchronization</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Deterministic Latency</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Harmonic Clocking</td>
<td>No</td>
<td>No</td>
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JESD204B Benefits

- Reduced/simplified PCB area
- Reduced package size
- Comparable power for large throughput
- Scalable to higher frequencies
- Simplified interface timing
- Standard interface


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Speed limited by setup/hold due to PVT variation

Speed scalable using SERDES/CDR techniques
JESD204B Benefits

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LVDS Timing

SERDES Timing
JESD204B Benefits

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- Standard interface
JESD204B Costs

- Increased interface latency
- Increased FPGA firmware complexity / licensing
JESD204B Link Data Flow and Protocol Layer Diagram

JESD204B Transmitter (Tx)

- Data Generation
- Transport Layer
- Scrambler (optional)
- Link Layer
- Physical Layer (Tx)

- Parallel → Serial Data Mapping
- 8b/10b Encoding
- Alignment Character Insertion
- Link Synchronization (slave)
- Data Serialization Transmission

- Frame and LMFC Clock Generator
- Local Multi-Frame Clock (Tx, LMFC)
- Frame Clock (Tx)

- Device Clock
- Device Clock

JESD204B Receiver (Rx)

- Back-end Data Processing
- Transport Layer
- De-Scrambler (optional)
- Link Layer
- Physical Layer (Rx)

- Serial → Parallel Data Mapping
- 8b/10b Decoding
- Character Replacement
- Link Synchronization (master)
- Data De-Serialization Reception

- Frame and LMFC Clock Generator
- Frame Clock (Rx)
- Local Multi-Frame Clock (Rx, LMFC)

*Subclass 1
Frame Clock
• Data frame of the transport layer is aligned to the frame clock
• Frame clock period in all the TX and RX devices must be identical

Local Multi-Frame Clock (LMFC)
• Multi-Frame is composed of ‘K’ Frames
• LMFC is aligned to the multi-frame boundary
• Acts as a low-frequency reference to resolve frame clock phase ambiguity across multiple devices
• LMFC period in all TX and RX devices must be identical
JESD204 Timing Signals/Terminology

Device Clock

• System clock from which the device’s frame, sampling, LMFC clocks are derived (externally applied)

Sample Clock

• Internal conversion clock of data converter
• Derived from Device Clock (via multipliers or dividers)
• Relationship to frame clock depends on packing of data into frame

SYSREF

• Timing phase reference from which LMFC clocks are generated in subclass 1 implementations (externally applied)
• Must be source synchronous with Device Clock
• Rising edge transition determines LMFC alignment
JESD204 Timing Signals/Terminology

SYNC

- Unidirectional, Receiver-to-Transmitter
- Active low signaling, often referred to as ‘SYNC~’ or ‘SYNCb’
- Mainly used for device synchronization requests and error reporting
- Aligns LMFC phase in Subclass 2 devices
- Options available for distributing SYNC to multiple devices
Transport Layer Overview

- Maps the data → octets → frames consisting of multiple octets
- Adds optional control bits to samples if needed
- Distinguishes the possible combinations of device/links/lanes/etc.
- Important parameters associated with transport layer include:
  - L  # of lanes per converter device
  - M  # of converters per device
  - F  # of octets per frame (per lane)
  - S  # of samples per converter per frame clock cycle
  - CS # of control bits per conversion sample
Transport Layer (Generic Example)

- **Converters per Device (M):** 8
- **Samples per Frame (S):** 1
- **Converter Resolution (N):** 11
- **Converter Resolution (N'):** 13
- **Control bits per sample (CS):** 2
- **Number of bits in Sample plus control bits:** 13
- **Number of bits per Lane (L):** 4
- **Octets per Frame (F):** 4
- **Frames per Multi-Frame (K):** User Defined
- **Release Buffer Delay (RBD):** User Defined

### Mapping Converter Samples to Frames

- **Octet 0:** Core 0 [10:3] Core 0 [2:0] C1 C0 T T T
- **Octet 1:** Core 2 [10:3] Core 2 [2:0] C1 C0 T T T
- **Octet 2:** Core 4 [10:3] Core 4 [2:0] C1 C0 T T T
- **Octet 3:** Core 6 [10:3] Core 6 [2:0] C1 C0 T T T

**1 Frame**

- **Lane 0:** Core 1 [10:3] Core 1 [2:0] C1 C0 T T T
- **Lane 1:** Core 3 [10:3] Core 3 [2:0] C1 C0 T T T
- **Lane 2:** Core 5 [10:3] Core 5 [2:0] C1 C0 T T T
- **Lane 3:** Core 7 [10:3] Core 7 [2:0] C1 C0 T T T
Transport Layer (ex. ADS42JB49)

LMFS 2221

N=14 14-bit Samples

ADC Core 0

ADC Core 1

M=2

S=1

N’=14

CS=0

Tails Bits

Lane 0

Lane 1

F=2

Octet 0

Octet 1

Core 0 [13:6] Core 0 [5:0]

Core 1 [13:6] Core 1 [5:0]

Note: Actual ADS42JB49 implementation defines N’=16 and inserts 0’s into LSBs instead of defining tail bits

LMFS 4211

N=14 14-bit Samples

ADC Core 0

ADC Core 1

M=2

S=1

N’=14

CS=0

Lane 0

Lane 1

Lane 2

Lane 3

F=1

L=4

Octet 0

Octet 1

Core 0 [13:6]

Core 0 [5:0]

Core 1 [13:6]

Core 1 [5:0]
Scrambling

• Scrambling randomizes data and spreads the spectral content to reduce spectral peaks that could cause EMI and interference problems.

• Transport layer output may be optionally scrambled with the polynomial: $1 + x^{14} + x^{15}$

• The RX descrambler self-synchronizes after receiving only two octets.

• TX supports early-synchronization option that allows descrambler to self-synchronize during ILA.
Data Link Layer

- 8b/10b Encoding
- Link Establishment, including frame and lane alignment
- Link Monitoring using control symbols
Data Link Layer: 8b/10b Encoding

- Encodes 8-bit “octets” into 10-bit symbols
- Octet to symbol mapping depends on running disparity (RD)
- Coding provides many bit-transitions to enable CDR techniques
- DC balancing enables AC coupling
Data Link Layer: Link Establishment

- Link Establishment accomplishes TX and RX synchronization
  - Code Group Synchronization (CGS)
  - Initial Frame Synchronization
  - Initial Lane Synchronization
Physical Layer: Serial Lanes

- Physical layer defines the electrical and timing characteristics of data transfer
- Point-to-point, unidirectional serial interface
- AC or DC compliance
- 3 signal speed-grade variants
- Performance limited by SERDES, CDR and driver/receiver blocks

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<tr>
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</thead>
<tbody>
<tr>
<td>Data Rates</td>
<td>312.5Mbps – 3.125Gbps</td>
<td>312.5Mbps - 6.375Gbps</td>
<td>312.5Mbps – 12.5Gbps</td>
</tr>
<tr>
<td>Differential Output Voltage</td>
<td>500 – 1000 (mV)</td>
<td>400 – 750 (mV)</td>
<td>360 – 770 (mV)</td>
</tr>
<tr>
<td>Bit Error Rate (BER)</td>
<td>≤ 1e-12</td>
<td>≤ 1e-15</td>
<td>≤ 1e-15</td>
</tr>
</tbody>
</table>
Deterministic Latency: Motivation

- Applications are often sensitive to the variation of system latency
  - Synchronous sampling
  - Multi-channel phase array alignment
  - Gain control loop stability

- JESD204 and JESD204A do not achieve known/constant latency across the link across temp/supply/reboot variation

- Providing support for devices with internal clock dividers introduces potential for even more latency uncertainty
Deterministic Latency: Achieved

• JESD204B achieves deterministic latency: known/constant latency
  – Subclass 0: DL not achieved
  – Subclass 1: DL achieved using SYSREF with strict timing
  – Subclass 2: DL achieved using SYNC~ with strict timing

• Deterministic Latency achieved with these architecture features
  – SYSREF or SYNC~ are used to provide a deterministic reference phase to all devices for synchronization
  – LMFC provides a low frequency reference to avoid frame clock phase ambiguity in the presence of link delay changes
  – RX has an “elastic buffer” that absorbs link delay variation

• Texas Instruments recommends/supports subclass 1
  – LMFC phase easier to control with source synchronous SYSREF than with system synchronous SYNC~
JESD204B Subclasses

- Subclass distinction: Whether to, and how to achieve **time reference alignment** (as a requirement for **deterministic link latency**)

<table>
<thead>
<tr>
<th></th>
<th>Subclass 0</th>
<th>Subclass 1</th>
<th>Subclass 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deterministic Latency Supported?</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>How to achieve Deterministic Latency?</td>
<td>N/A</td>
<td>Time reference (LMFC) alignment using <strong>SYSREF</strong></td>
<td>Time reference (LMFC) alignment using <strong>~SYNC</strong></td>
</tr>
</tbody>
</table>
Subclass Signaling Requirements

**SUBCLASS 0**

- Transmitter: JESD204B Subclass 0
- Receiver: JESD204B Subclass 0
- Clock Generator

**SUBCLASS 1**

- Transmitter: JESD204B Subclass 1
- Receiver: JESD204B Subclass 1
- JESD204B Clock Generator

**SUBCLASS 2**

- Transmitter: JESD204B Subclass 2
- Receiver: JESD204B Subclass 2
- Clock Generator
## Choosing a Subclass

<table>
<thead>
<tr>
<th>Feature</th>
<th>Subclass 0</th>
<th>Subclass 1</th>
<th>Subclass 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>JESD204A Backward Compatible?</strong></td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Deterministic Latency Supported?</strong></td>
<td>No</td>
<td>Yes</td>
<td>Yes, but speed limited</td>
</tr>
<tr>
<td><strong>SYSREF Required?</strong></td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Clock and Sync Signals</strong></td>
<td>Device Clock SYNC~</td>
<td>Device Clock SYSREF SYNC~</td>
<td>Device Clock SYNC~</td>
</tr>
<tr>
<td><strong>SYNC~ is Timing Critical?</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Interface Hardware Complexity</strong></td>
<td>Least</td>
<td>Most</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>Link Latency</strong></td>
<td>8-100 sample clocks (non-deterministic)</td>
<td>15-120 sample clocks (deterministic)</td>
<td></td>
</tr>
</tbody>
</table>
# Subclass by Application Examples

<table>
<thead>
<tr>
<th>Application</th>
<th>Subclass 0</th>
<th>Subclass 1</th>
<th>Subclass 2</th>
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<tbody>
<tr>
<td><strong>Wireless Comms. Repeater</strong></td>
<td><img src="image" alt="Checkmark" /></td>
<td><img src="image" alt="Checkmark" /></td>
<td><img src="image" alt="Checkmark" /></td>
</tr>
<tr>
<td>- Narrowband (&lt;125 MSPS ADC)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- No DL requirements</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Software Defined Radio</strong></td>
<td></td>
<td><img src="image" alt="Checkmark" /></td>
<td><img src="image" alt="Checkmark" /></td>
</tr>
<tr>
<td>- Wideband</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- DL required</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Radar, Imaging Sensor</strong></td>
<td><img src="image" alt="Checkmark" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Wideband (&gt;250 MSPS ADC)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- DL required + Multi-Device Sync.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Oscilloscope, Spectrum Analyzer</strong></td>
<td><img src="image" alt="Checkmark" /></td>
<td><img src="image" alt="Checkmark" /></td>
<td></td>
</tr>
<tr>
<td>- Wideband (&gt; 250 MSPS ADC)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- No DL Required</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>- DL Required</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Texas Instruments’ JESD204B device all support subclass 1 while some support all 3 subclasses
Summary

- JESD204: Standard serial data interface for data converters

- JESD204B subclasses offer 3 implementation variations

- Transport Layer defines data framing into serial lanes

- Link layer defines encoding, synchronization and data monitoring

- Physical layer defines the electrical and timing performance

- Deterministic latency achieved with subclasses 1, 2 and is required for known/constant latency through link
More Educational Resources

www.ti.com/lsds/ti/data-converters/high-speed-adc-greater-10msps-jesd204b.page
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