Overview

• What is the Physical Layer (PHY)?
• Speed Grades and Compliance Types
• SERDES Interface
• Solutions for Long/Lossy Channels
• Device Clock, SYSREF and SYNC~ Interfaces
• PCB Layout Recommendations
What is the Physical Layer (PHY)?

- The “Physical Layer” refers to the serial data transmitter and receiver of the JESD204B link
- Point-to-point, unidirectional serial interface
- Definition includes electrical and timing characteristics
- This presentation also considers the other signal interfaces
What is the Physical Layer (PHY)?

**JESD204B Tx PHY**

- Parallel-to-Serial Converter (10:1 MUX)
- Bit-Stream
- Pulse-Shaping / Emphasis (Optional)
- Differential CML Driver

**JESD204B Rx PHY**

- Serial-to-Parallel Converter (1:10 DEMUX)
- Character Alignment
- Bit-Stream
- CDR (Clock/Data Recovery)
- Equalizer (Optional)
- Differential CML Receiver
Speed Grades and Compliance

- The JESD204B standard defines 3 speed grade variants
- Based on OIF Optical standards (OIF-CEI-02.0)
- Variants differ most importantly in data rate, eye mask, and BER

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rates</td>
<td>312.5Mbps – 3.125Gbps</td>
<td>312.5Mbps - 6.375Gbps</td>
<td>312.5Mbps – 12.5Gbps</td>
</tr>
<tr>
<td>Differential Output Voltage</td>
<td>500 – 1000 (mV)</td>
<td>400 – 750 (mV)</td>
<td>360 – 770 (mV)</td>
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<tr>
<td>Output Rise or Fall Time</td>
<td>≥ 50 (ps)</td>
<td>≥ 30 (ps)</td>
<td>≥ 24 (ps)</td>
</tr>
<tr>
<td>(20% - 80% into 100Ω load)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit Error Rate (BER)</td>
<td>≤ 1e-12</td>
<td>≤ 1e-15</td>
<td>≤ 1e-15</td>
</tr>
</tbody>
</table>

- Compliance refers to AC or DC coupling and impacts the electrical characteristics of the driver/receiver
**PHY Electrical Requirements**

- PHY defines the I/O electrical structure of the driver and receiver.

### Common Mode Voltage Range

### Signal Swing Range

### Impedance and Return Losses

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>UI</td>
<td>Unit Interval</td>
<td></td>
<td>80</td>
<td>1569</td>
<td>ps</td>
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<tr>
<td>True/Tfall</td>
<td>Rise and Fall Times</td>
<td>20% - 80% into 100 Ω load</td>
<td>24</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>T_Vcm</td>
<td>Output Common Mode Voltage</td>
<td>- Applies only to AC coupling. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 3). - Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 4). - Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 5). - Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 6).</td>
<td>0</td>
<td>1.8</td>
<td>V</td>
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<tr>
<td>Vdiff</td>
<td>Transmitter Differential Voltage</td>
<td>Into floating 100 Ω load</td>
<td>360</td>
<td>770</td>
<td>mVppd</td>
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<tr>
<td>Idshort</td>
<td>Transmitter Short Circuit Current</td>
<td>Transmitter terminal(c) shorted to each other or ground, power on.</td>
<td>-100</td>
<td>+100</td>
<td>mA</td>
</tr>
<tr>
<td>Zdiff</td>
<td>Differential Impedance</td>
<td>At DC</td>
<td>80</td>
<td>120</td>
<td>Ω</td>
</tr>
<tr>
<td>RLdiff</td>
<td>Differential Output Return Loss</td>
<td>From 100MHz to 0.75*Band Rate</td>
<td>8</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RLcm</td>
<td>Common Mode</td>
<td>From 100MHz to 0.75*Band Rate</td>
<td>6</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**Figure 2 — Differential peak-to-peak Voltage = 2 * (V_{high} - V_{low})**
PHY Eye/Timing Requirements

- Total jitter is composed of both random and deterministic components
- JESD204B standard identifies requirements for different types of jitter

PHY Eye/Timing Requirements

• Jitter Units
  – ‘peak-to-peak Unit Interval’ [p-p UI]:
    • 1 UI is equivalent to 1 bit period at the given transfer rate
  – ‘peak-to-peak seconds’ [p-p s]
  – ‘peak-to-peak Root-Mean-Square seconds’ [p-p rms]
    • Used to describe unbounded random jitter values
    • Must specify a BER to indicate probability density function (PDF) bounds for conversion to [p-p UI] (i.e. 1e-15)

• Combining Jitter Components
  – Random Jitter adds as sum of squares (un-correlated)
  – Deterministic Jitter sums directly (correlated)
  – Total Jitter is a direct sum of Random and Deterministic Components
    • $TJ = RJ + DJ$
PHY Eye/Timing Requirements

- TX and RX Eye Masks with amplitude, rise-time, and jitter requirements
- RX must recover signal after channel loss and ISI

### Transmit Eye Mask

<table>
<thead>
<tr>
<th>XT1 (UI)</th>
<th>XT2 (UI)</th>
<th>YT1 (V)</th>
<th>YT2 (V)</th>
<th>T_UBHPJ (p-p UI)</th>
<th>T_DCD (p-p UI)</th>
<th>TJ (p-p UI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.15</td>
<td>0.4</td>
<td>0.385</td>
<td>0.18</td>
<td>0.15</td>
<td>0.05</td>
<td>0.3</td>
</tr>
</tbody>
</table>

### Receive Eye Mask

**Deterministic Jitter (DJ)**

**Random jitter plus Deterministic Jitter**

Bit-Error Rate

---

**Figure 9** Transmit Eye Mask for LV-OIF-11G-SR – based operation

**Figure 10** Receive Eye Mask for LV-OIF-11G-SR – based operation
Solutions for Long/Lossy Channels

- Channel dielectric loss degrades the signal integrity of the signal
- Loss reduces the vertical/horizontal Eye opening and edge rate due to attenuation and inter-symbol interference (ISI)
- Loss Profile mask is specified in the JESD204B standard
Solutions for Long/Lossy Channels

- Equalization can be used to pulse-shape at TX or pulse-correct RX
- High-pass profile of equalization counteracts low-pass loss profile of channel
- Pre-emphasis
  - AMPLIFY HIGH frequencies to achieve high-pass profile
- De-emphasis
  - ATTENUATE LOW frequencies to achieve high-pass profile
  - May require broadband amplification to meet eye requirements at large de-emphasis

High-pass emphasis profile (blue) matches the inverse of the channel loss profile (pink)
Solutions for Long/Lossy Channels

- **ADC16DX370** De-Emphasis Waveform @ 5 Gb/s at TX output

  ![De-emphasis disabled](image1)

  ![Maximum De-emphasis](image2)

- Waveform @ 7.4 Gb/s at output of 20-inch FR4 channel

  ![De-emphasis disabled](image3)

  ![De-emphasis Optimized](image4)

**Easily Meets JESD204B RX Eye Spec!!!**
Solutions for Long/Lossy Channels

- **ADC12J4000** Pre-Emphasis Waveform @ 7 Gb/s over 7 inches FR4
Device Clock and SYSREF Interfaces

- No strict definition for electrical characteristics
  - LVDS, LVPECL are common solutions
- Device clock frequency may be equal to sampling rate or multiple
- Noise on device clock typically sets jitter performance of converter
- Attention required for DC-coupled common-mode compatibility of TX/RX
- Subclass 1
  - SYSREF must meet setup/hold relative to device clock
  - Electrical characteristics recommended to be consistent between device clock and SYSREF

- Subclass 2: SYSREF not required
SYSREF Interface (Signal Types)

- **Periodic**
  - SYSREF always ON with periodic edges
  - Risk of interferer spurs near IF due to SYSREF

- **Gapped-Periodic**
  - Send periodic edges for a brief pulse of time
  - No spurs

- **One-Shot**
  - Single SYSREF pulse and then leave in logic-low state
  - No spurs

- SYSREF pulse period equal to integer multiple of multi-frame period
- Disabling and gating the SYSREF signal may be employed
TSW1400 Captured Data, SYSREF enabled

- Periodic SYSREF has sub-harmonic relationship to ADC sampling clock
TSW1400 Captured Data, SYSREF disabled
SYNC~ Interface

- No strict definition for electrical characteristics
  - LVDS, LVPECL, CMOS are common solutions

- DC coupling mandatory

- Subclass 1
  - SYNC~ does not have strict timing

- Subclass 2
  - SYNC~ must meet setup/hold relative to device clock
  - Timing requirements very difficult to meet for device clock rates > 250MHz

![SYNC~ signal timing for Subclass 0 and Subclass 2 Devices](image)
Differential Interfaces
(Example circuits)

- Serial Lane Interface
  - AC or DC Coupling
  - 100Ω differential channel
  - Routing signal integrity is MOST critical of all JESD204B interface signals

- Device Clock / SYSREF Interface
  - AC or DC Coupling
  - AC coupling SYSREF requires provision for DC balancing at receiver
  - 100Ω differential channel
  - Match device clock and SYSREF interface to meet setup/hold requirement
Differential Interfaces (Example Circuits)

- **SYNC~ Interface**
  - DC Coupling only
  - $100\Omega$ differential channel
  - Routing VERY critical for subclass 2
  - Routing is LEAST critical for subclass 1
Generating Device Clocks and SYSREF

- Example: LMK04828
  - Subclass 1 capable
  - 7 Device CLK / SYSREF pairs
  - Low Jitter clock source
  - SYSREF Disable feature
  - Delay options
  - LVPECL, LVDS, HSDS outputs
  - Supports Clock Distribution mode using external clock source
PCB Recommendations (Differential Pairs)

• Route differential signal as \textit{tightly coupled} microstrip or stripline lanes ($S \leq W$)

• 100 $\Omega$ differential impedance

• Avoid 90° turns
  – Reduces +/- trace mismatch
  – Reduces impedance discontinuity

• Recommend 0201 series components (AC coupling) to minimize impedance discontinuity of pads

• Routing on inner layers (stripline) has advantages:
  – Better impedance control
  – No speed issues with Nickel plating
  – Less interference/emissions
PCB Recommendations (Trace Matching)

- Device Clock, SYSREF, SYNC~, and serial lanes must be between matched +/- traces

- Device Clock and SYSREF pairs must be matched to each other

- Serial lanes need NOT match to each other

- Use wiggles to match the lengths of multiple differential pairs.
  - Keep radius of the wiggle > 3 times trace width
  - Use equal number of turns in each direction

- Use small jog-outs to correct +/- trace mismatch
PCB Recommendations (Vias)

- Vias in the signal path create impedance discontinuities that result in signal reflections/degradation
- Simulate signal path with vias to determine signal integrity before manufacturing
- Avoid changing layers where possible, but use adjacent grounding vias where layer change is necessary to provide return current path
- Via stitch along sensitive differential signal paths
- Use blind vias or back-drilling to eliminate via stubs

![Waveform “blip” due to via in the signal path](image1)
![Adjacent GND vias](image2)
![Via stitching](image3)
PCB Recommendations (Material/Stack-Up)

- Serial lane speeds > 3 Gb/s at length > 8”
  - Recommend low-loss, good impedance consistency dielectric material
  - Rogers-4350, Megtron-6.
  - Use premium dielectric only where needed

- Serial lane speeds < 3 Gb/s at length < 8”
  - Recommend low cost materials
  - FR4, 370HR

- Board shop reports that 370HR can be used up to 10 GHz with very short traces (1-3 inches)
PCB Recommendations (Reference Planes)

• Use a ground plane as the signal reference on adjacent layers

• Avoid splits in the reference plane underneath signals when possible
  – Return current for high-speed signals follows trace on the reference plane
  – Splits require the return current to travel around, increasing loop inductance, coupling, and interference

• When reference plane splits under differential signals are necessary:
  – Minimize split width
  – Ensure tight coupling of differential pair
  – Jump split at 90°
  – Good GND via stitching along channel
  – Avoid jumping split in vicinity of other noisy signals
PCB Recommendations (Reference Planes)

• Keep analog signals separate from digital signals
  – Single ground plane is recommended
  1. Split ground plane at DAC/ADC into analog and digital planes
  2. Route the signal traces in their respective domains
  3. Recombine the two ground planes into one after routing
PHY Debug (Test Patterns)

- Test patterns can verify the PHY layer signal integrity

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Use Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRBS7 /15 /23 /31</td>
<td>Long pattern performance</td>
</tr>
<tr>
<td></td>
<td>Deterministic Jitter (ISI)</td>
</tr>
<tr>
<td>01010101010 (D21.5)</td>
<td>Random Noise</td>
</tr>
</tbody>
</table>

- PRBS and D21.5 patterns available on all TI JESD204B devices
- Most FPGA giga-bit transceivers have built-in PRBS generators/detectors
## Handling Link Errors

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Effect on Serial Stream</th>
<th>Link Error Detection</th>
<th>Link Response</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Jitter/ISI</strong></td>
<td>Single bit error</td>
<td>8b/10b decoding fails</td>
<td>- Output previous good frame</td>
</tr>
<tr>
<td><strong>Single bit error</strong></td>
<td></td>
<td>(not-in-table error)</td>
<td>- SYNC asserted for 2 frames</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Jitter/ISI</strong></td>
<td>Multi-bit error, possibly across many frames</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Multi-bit error</strong></td>
<td></td>
<td>- Not-in-table error</td>
<td>- Depends on specific error</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Disparity error</td>
<td>- SYNC asserted &gt;= 2 frames</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Control Char error</td>
<td>- Link re-initialization likely*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Frame alignment error</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>ADC Core Sample Error</strong></td>
<td>None. Erroneous sample is encoded, transmitted, received as usual.</td>
<td>No error detected</td>
<td>No change</td>
</tr>
</tbody>
</table>

- The list of errors which require link re-initialization is implementation specific
## TI Devices SERDES Summary

<table>
<thead>
<tr>
<th>Device</th>
<th>Max Conversion Rate</th>
<th>Max Bit Rate</th>
<th>Min #Lane/Ch. (at full MSPS)</th>
<th>Emphasis / Equalization?</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC16DX370</td>
<td>370 MSPS</td>
<td>7.4 Gb/s</td>
<td>1</td>
<td>TX De-emphasis</td>
</tr>
<tr>
<td>ADS42JB69</td>
<td>250 MSPS</td>
<td>3.125 Gb/s</td>
<td>2</td>
<td>Not needed</td>
</tr>
<tr>
<td>ADS42JB46</td>
<td>160 MSPS</td>
<td>3.125 Gb/s</td>
<td>1</td>
<td>Not needed</td>
</tr>
<tr>
<td>ADC3K Family (Preview)</td>
<td>160 MSPS</td>
<td>3.125 Gb/s</td>
<td>1</td>
<td>Not needed</td>
</tr>
<tr>
<td>ADC12J4000</td>
<td>4000 MSPS</td>
<td>8 Gb/s</td>
<td>*</td>
<td>TX Pre-Emphasis</td>
</tr>
<tr>
<td>ADC12J2700</td>
<td>2700 MSPS</td>
<td>10 Gb/s</td>
<td>*</td>
<td>TX Pre-Emphasis</td>
</tr>
<tr>
<td>DAC38J84</td>
<td>2500 MSPS</td>
<td>12.5 Gb/s</td>
<td>0.25</td>
<td>RX Adaptive Equalizer</td>
</tr>
</tbody>
</table>

*Decimation Factor Dependent
Summary

- The Physical Layer refers to the electrical and timing characteristics of the TX and RX and their ability to send and recover data.

- Equalization and (pre-/de-) emphasis can be used to enhance signal integrity of the link for longer lengths and higher bit rates.

- Device Clock, SYSREF, and SYNCb interfaces and not strictly defined in the standard, but common guidelines are provided.

- Very high speed layout techniques for the serial lanes are critical to ensure impedance matching and minimization of signal reflections.

- Test patterns such as D21.5 and PRBS usually patterns are available for physical layer debug.
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