**APPENDIX C**

**FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL**

**Example 1: 12 Volt, 60 Watt Output**

\[ f_s = 80 \text{ kHz}, \ T = 12.5 \mu\text{sec} \]
\[ V_{in} = 12 \text{ to } 24 \text{ V} \]
\[ V_o = 12 \text{ V}, \ I_o = 0.5 \text{ to } 5 \text{ A} \]
\[ R_o = 24 \text{ to } 2.4 \text{ Ohms} \]
\[ I_{sc} = 6 \text{ A Short Circuit Limit} \]

Discontinuous Current Mode Boundary

Duty Cycle Limit at \( I_{sc} \text{ min } V_{in} \):

\[ D_{max} = \frac{1}{1+V_{in}/V_o} = 0.5 \]

Max. \( t_d = (1-D)T = 6.25 \mu\text{sec} \)

Max. \( I_p = 2I_{sc}/(1-D) = 2x6/0.5 = 24 \text{ A} \)

\[ L = (V_o+V_f)t_d/I_p = 13x6.25/24 = 3.4 \mu\text{H} \]

ESR Max for 0.1 \( V_{pp} \) Ripple at \( I_o = 5\text{A} \):\n
\[ R_c = 0.1/20A = 5 \text{ m\Omega max} (1 \text{ m\Omega min}) \]

\[ C = 20,000 \mu\text{F} \]

**Basic Equations — Duty Cycle Control:**

\[ D = V_c/V_s : \]

DC Relationships:

\[ V_o = V_{in}D\left(\frac{R_o}{2L_f}\right)^{\frac{1}{2}} = V_{in}V_c\left(\frac{R_o}{2L_f}\right)^{\frac{1}{2}} \quad (1a) \quad V_c = \frac{V_oV_s}{V_{in}\left(\frac{2L_f}{R_o}\right)^{\frac{1}{2}}} \]

Control to Output Gain:

\[ \frac{V_o}{V_c} = \frac{V_{in}}{V_s}\left(\frac{R_o}{2L_f}\right)^{\frac{1}{2}} \text{He}(s), \quad \text{He}(s) = \frac{1+s/\omega_z}{1+s/\omega_p} \quad , \quad \omega_p = \frac{2}{R_o C} \quad \omega_z = \frac{1}{R_c C} \]

Line to Output Gain:

\[ \frac{V_o}{V_{in}} = \frac{V_c}{V_s}\left(\frac{R_o}{2L_f}\right)^{\frac{1}{2}} \text{He}(s) = \frac{V_o}{V_{in}} \text{He}(s) \]

Corner Frequencies from Equation (2):

\[ f_p = 2/(2\pi R_o C) = 15.92/R_o \quad = 6.63 \text{ Hz at } 2.4 \Omega, \quad .663 \text{ at } 24 \Omega \]
\[ f_z = 1/(2\pi R_c C) = 7.95/R_c \quad = 1590 \text{ Hz at } 5 \text{ m\Omega}, \quad 7950 \text{ Hz at } 1 \text{ m\Omega} \]

Low Frequency Gain from Equation (2) \( (V_s = 2.5 \text{ V for UC1524A}) \)

\[ \frac{V_o}{V_c} = .542V_{in}\sqrt{R_o} = 20.2 \text{ (26.7 dB) at } 24 \text{ V, } 2.4 \Omega \]
\[ \quad = 31.9 \text{ (30.1 dB) at } 12 \text{ V, } 24 \Omega \]

\( V_c \text{ must be clamped to } 1.25 \text{ V to limit Duty Cycle to } 0.5 \text{ max.} \)
FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - DIRECT DUTY CYCLE CONTROL

Error Amplifier Compensation:

Control I.C.: UC1524A

Crossover frequency (0 dB loop gain):

\[ f_c = \frac{f_s}{4} = 20 \text{ kHz} \]

E/A gain needed at 20 kHz = 21.5 dB

ESR zero, \( f_z \), cancelled by pole \( f_p \) at \( \frac{max f_z}{10} \). This increases low frequency gain and adds 45° more phase lag, still leaving a phase margin of 45°:

\[ f_p = \frac{max f_z}{10} = 795 \text{ Hz} \]

E/A gain required below \( f_p \) is:

\[ 21.5 + 20 \log(20,000/795) = 49.5 \text{ dB} \]

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ V_c = \frac{V_o V_f}{V_i n} \left( \frac{2 L f}{R_o} \right) = \frac{12 \times 2.5 - 3.4 \times 0.8}{V_i n - R_o} = 0.188 \text{ to } 1.19 \text{ V} \]

\( \Delta V_c = 1.0 \text{ V} \)

Output voltage error with actual E/A DC gain of 298 (49.5 dB):

\[ \Delta V_o = \frac{\Delta V_c}{298} = 3.4 \text{ mV} \] (120 mV = 1% regulation)

Implementation: Circuit of Appendix A-1 (omit \( R_p \) and \( C_p \))

UC1524A has transconductance error amplifier (\( gm = .002 \))

With \( R_f = 3M\Omega \), max. gain = \( gmR_f = 6000 \) (75.6 dB, > 64 dB required, OK)

Gain required below \( f_p = 298 \) (49.5 dB) = \( R_f/R_i \).

\[ R_i = 3M/298 = 10K \]

Pole at 795 Hz:

\[ C_f = \frac{1}{(2\pi f_p R_f)} = 67 \text{ pF} \]
Example 2: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 1.

Basic Equations — Voltage Feedforward:

\[ D = \frac{V_c}{V_s}, \quad V_s = \frac{V_{in}}{K}, \quad K = \frac{V_{in}D}{\max V_c} \]

DC Relationships:

\[ (1) \quad V_o = \frac{V_{in}D}{\frac{R_o}{2L_f}} = K V_c \left( \frac{R_o}{2L_f} \right)^\frac{1}{2} \]

\[ (1a) \quad V_c = \frac{V_o}{K} \left( \frac{R_o}{2L_f} \right)^\frac{1}{2} \]

Control to Output Gain:

\[ (2) \quad \frac{V_o}{V_c} = K \left( \frac{R_o}{2L_f} \right)^\frac{1}{2} H_e(s), \quad H_e(s) = \frac{1+s/\omega_p}{1+s/\omega_z}, \quad \omega_p = \frac{2}{R_oC}, \quad \omega_z = \frac{1}{R_eC} \]

Line to Output Gain:

\[ (3) \quad \frac{V_o}{V_{in}} = 0 \quad \text{Inherent good line regulation and audio susceptibility} \]

Corner Frequencies from Equation (2):

\[ f_p = \frac{2}{(2\pi R_o C)} = 15.92/R_o = 6.63 \text{ Hz at } 2.4 \Omega, \quad .663 \text{ at } 24 \Omega \]

\[ f_Z = \frac{1}{(2\pi R_e C)} = 7.95/R_e \quad = 1590 \text{ Hz at } 5 \text{ m}\Omega, \quad 7950 \text{ Hz at } 1 \text{ m}\Omega \]

Low Frequency Gain from Equation (2) \( \max V_c = 3.5 \text{ V for UC1840} \)

\[ K = \frac{V_{in}D}{\max V_c} = 12\times0.5/3.5 = 1.71 \quad \text{(feedforward factor)} \]

\[ \frac{V_o}{V_c} = 2.52 - \sqrt{R_o} \quad = 3.91 (11.8 \text{ dB}) \text{ at } 2.4 \Omega \]

\[ = 12.35 (21.8 \text{ dB}) \text{ at } 24 \Omega \quad V_{in} = 12 \text{ to } 24 \text{ V} \]
FLYBACK — DISCONTINUOUS INDUCTOR CURRENT — VOLTAGE FEEDFORWARD CONTROL

Error Amplifier Compensation:

Control I.C.: UC1840

Crossover frequency (0 dB loop gain)

\[ f_c = \frac{f_s}{4} = 20 \text{ kHz} \]

E/A gain needed at 20 kHz = 35.8 dB

ESR zero, \( f_z \), is cancelled by pole \( f_p \) at max \( f_z/10 \). This increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

\[ f_p = \frac{\text{max} f_z}{10} = 795 \text{ Hz} \]

E/A gain required below \( f_p \) is:

\[ 35.8 + 20 \log\left(\frac{20,000}{795}\right) = 63.8 \text{ dB} \]

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ (1a) \quad V_c = \frac{V_o}{K} \left(\frac{2Lf_c}{R_o}\right) = \frac{12-\sqrt{2} \times 3.4 \times 0.08}{1.71 - \sqrt{R_o}} = 1.05 \text{ to } 3.33 \text{ V.} \quad \Delta V_c = 2.28 \text{ V} \]

Output voltage error with actual E/A DC gain of 1550 (63.8 dB):

\[ \Delta V_o = \frac{\Delta V_c}{1550} = 1.5 \text{ mV} \quad (120 \text{ mV} = 1\% \text{ regulation}) \]

Implementation: Circuit of Appendix A-1 (omit \( R_p \) and \( C_p \))

Voltage feedforward factor, \( K \), in UC1840 is set by an independent ramp generator whose slope varies directly with \( V_{in} \). A minimum ramp charging current of 36 \( \mu \text{A} \) is chosen (near the bottom end of the optimum range).

\[ R_T = \min V_{in}/\min I_T = \frac{12}{36\mu \text{A}} = 330K \]

\[ \frac{dv}{dt} = I_T/C_T = V_{in}/R_T C_T = \text{max} v_c/t_{on}. \quad R_T C_T = V_{int_{on}}/\text{max} v_c = K/f \]

\[ C_T = K/f R_T = 1.71 / (80K \times 330K) = 65 \text{ pF} \]

UC1840 has voltage mode amplifier with 65 dB gain, > 63.8 dB required, OK.

\( R_f = 3 \text{ M}, \) chosen somewhat arbitrarily because of high gain required.

Gain required below \( f_p = 1550 \) (64 dB) = \( R_f/R_i \). \quad \( R_i = 3M/1550 = 2K \).

Pole at \( f_p = 795 \text{ Hz} \):

\[ C_f = 1/(2\pi f_p R_f) = 67 \text{ pF} \]

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Example 3: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 1.

Basic Equations — Current Mode Control:

\[ I_p = K V_c, \quad K = \frac{\text{max}I_p}{\text{max}V_c} \]

DC Relationships:

1. \[ V_o = V_{in}D \left( \frac{R_o}{2L_f} \right)^{\frac{1}{2}} = K V_c \left( \frac{R_o L_f}{2} \right) \]  
   \[ V_c = \frac{\sqrt{2}}{K \sqrt{L_f R_o}} \]

Control to Output Gain:

2. \[ \frac{V_o}{V_c} = K - \sqrt{R_o L_f} \frac{H_e(s)}{2} \]
   \[ H_e(s) = \frac{1 + s/\omega_p}{1 + s/\omega_p}, \quad \omega_p = \frac{2}{R_o C}, \quad \omega_z = \frac{1}{\tau} \]

Line to Output Gain:

3. \[ \frac{V_o}{V_{in}} = 0 \quad \text{Inherent good line regulation and audio susceptibility.} \]

Corner Frequencies from Equation (2):

\[ f_p = \frac{2}{(2\pi R_o C)} = 15.92/R_o = 6.63 \text{ Hz at } 2.4 \Omega, \quad \text{663 at } 24 \Omega \]
\[ f_z = \frac{1}{(2\pi R_o C)} = 7.95/R_c = 1590 \text{ Hz at } 5 \text{ m\Omega}, \quad 7950 \text{ Hz at } 1 \text{ m\Omega} \]

Low Frequency Gain from Equation (2) \( (V_c \text{ clamped to } 2.4 \text{ V for } 24 \text{ A } I_{SC}) \)

\[ K = \frac{\text{max}I_p}{\text{max}V_c} = 24/2.4 = 10 \]
\[ \frac{V_o}{V_c} \approx 3.7\sqrt{R_o} = 5.73 (15.2 \text{ dB}) \text{ at } 2.4 \Omega \]
\[ = 18.1 (25.2 \text{ dB}) \text{ at } 24 \Omega \]
\[ V_{in} = 12 \text{ to } 24 \text{ V} \]
FLYBACK - DISCONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Error Amplifier Compensation:

Control I.C.: UC1846

Crossover frequency (0 dB loop gain)

\[ f_c = \frac{f_s}{4} = 20 \text{ kHz} \]

E/A gain needed at 20 kHz = 32 dB

ESR zero, \( f_z \), is cancelled by pole \( f_p \) at max \( f_z/10 \). This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

\[ f_p = \text{max} \frac{f_z}{10} = 795 \text{ Hz} \]

E/A gain required at and below \( f_p \) is:

\[ 32 + 20 \log(20,000/795) = 60 \text{ dB} \]

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ V_c = \frac{V_o}{K/\text{LfrO}} = \frac{12 - \sqrt{2}}{10 - 3.4x.08R_0} = 3.25 - R_0 = 0.664 \text{ to } 2.1 \text{ V.} \]

\[ \Delta V_c = 1.44 \text{ V} \]

Output voltage error with actual E/A DC gain of 1000 (60 dB):

\[ \Delta V_o = \Delta V_c/1000 = 1.44 \text{ mV} \ (120 \text{ mV} = 1\% \text{ regulation}) \]

Implementation: Circuit of Appendix A-1 (omit \( R_p \) and \( C_p \))

Current control factor \( (K = 10) \) is set with the UC1846 by the fixed gain \( (3X) \) of the current amplifier and the current sampling resistor, \( R_s \):

\[ K = \frac{I_p}{V_c} = 10 = 1/(3R_s). \]

\[ R_s = 1/(30) = 0.033 \Omega \]

UC1846 error amplifier gain limit >80 dB with \( R_f >30k \), > 60 dB required, OK.

\[ R_f = 3M, \] chosen somewhat arbitrarily because of high gain required.

Gain required below \( f_p = 1000 \) (60 dB) = \( R_f/R_i \).

\[ R_i = 3M/1000 = 3k. \]

Pole at \( f_p = 795 \text{ Hz:} \)

\[ C_f = 1/(2\pi f_p R_f) = 67 \text{ pF} \]
Example 4: 12 Volt, 240 Watt Output

\[ f_s = 40 \text{ kHz}, \ T = 25 \mu \text{sec} \]

\[ V_{in} = 30 \text{ to } 60 \text{ V} \]

\[ V_o = 12 \text{ V}, \ I_o = 2 \text{ to } 20 \text{ A} \]

\[ R_o = 6 \text{ to } 0.6 \text{ Ohms} \]

\[ I_{sc} = 24 \text{ A} \text{ Short Circuit Limit} \]

**Continuous Current Mode Boundary:**

- Min. \( I_o = 2 \text{ A} \)
- Max. \( \Delta I_L = 2(\text{min} I_o) = 4 \text{ A} \)

\[ D = V_o/V_{in} = 0.2 \text{ to } 0.4 \]

\[ t_{off} = 0.8 \times 25 = 20 \mu \text{sec} \text{ max} \]

\[ L = V_o t_{off}/\Delta I_L = 12 \times 20/4 = 60 \mu \text{H} \]

**ESR Max for 0.1 \( V_{pp} \) Ripple at \( \Delta I_L = 4 \text{ A} \):**

\[ R_c = 25 \text{ m\Omega} \text{ max} \ (5 \text{ m\Omega} \text{ min}) \]

\[ C = 4000 \mu \text{F} \]

**Basic Equations — Duty Cycle Control:**

\[ D = V_c/V_s; \]

**DC Relationships:**

\[ (1) \quad V_o = V_{in}D = V_{in} \frac{V_c}{V_s} \quad (1a) \quad V_c = \frac{V_o V_s}{V_{in}} \]

**Control to Output Gain:**

\[ (2) \quad \frac{V_o}{V_c} = \frac{V_{in}}{V_s} \quad H_e(s) = \frac{1}{1 + (s/\omega_o)/(Q + (s/\omega_o))^3}, \quad \omega_o = \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_c C} \]

**Line to Output Gain:**

\[ (3) \quad \frac{V_o}{V_{in}} = \frac{V_c}{V_s} \quad H_e(s) = \frac{V_o}{V_{in}} \quad Q = \frac{R_o}{\omega_0 L} \]

**Corner Frequencies from Equation (2):**

\[ f_o = 1/(2\pi\sqrt{LC}) = 325 \text{ Hz} \]

\[ f_z = 1/(2\pi R_c C) = 39.8/R_c \quad = 1590 \text{ Hz at } 25 \text{ m\Omega}, \ 7950 \text{ Hz at } 5 \text{ m\Omega} \]

**UC1524A ramp is 2.5 V at 80 kHz. One output is not used which limits duty cycle to 50% max. at 40kHz. \( V_s \) projects to 5 V over the full 40 kHz cycle.**

**Low Frequency Gain from Equation (2):**

\[ \frac{V_o}{V_c} = \frac{V_{in}}{5} = 12 \ (21.6 \text{ dB}) \text{ at } 60 \text{ V} \]

\[ = 6 \ (15.6 \text{ dB}) \text{ at } 30 \text{ V} \]
Error Amplifier Compensation:

Control I.C.: UC1524A
Crossover frequency (0 dB loop gain):
\( f_c = f_s/4 = 10 \text{ kHz} \)
E/A gain needed at 10 kHz = 21.5 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at \( f_o \) are compensated by two zeros at \( f_z = f_o/2 \). This provides additional phase shift at \( f_o \) for sudden second order transition.

\[ f_z = \frac{325}{2} = 162 \text{ Hz} \]

ESR zero, \( f_z \), is canceled by pole \( f_p \) at least 5 times above \( f_o \) to avoid adding more phase lag at \( f_o \). This happens to coincide with min. ESR zero, \( f_z \).

\[ f_p = \frac{1590}{Hz} \text{ with } 21.5 \text{ dB gain} \]

E/A gain required at \( f_z \) is:

\[ 21.5 - 20 \log(1590/162) = 1.7 \text{ dB} \]

Total control voltage swing, \( AV_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ V_c = \frac{V_oV_s}{Vin} = \frac{12x5}{Vin} = 1 \text{ to } 2 \text{ V. } AV_c = 1 \text{ V} \]

Output voltage error with actual E/A DC gain of 180 (45 dB at 1 Hz):

\[ AV_o = AV_c/180 = 5.5 \text{ mV } (120 \text{ mV} = 1\% \text{ regulation}) \]

Implementation: Circuit of Appendix A-2 (omit \( R_p, C_p \) and \( R_{fp} \))

UC1524A has transconductance error amplifier (gm = .002). Min. load resistance (min \( R_{fz} \) ) is 30K. \( R_{iz} \) is appx. 1x\( R_{fz} \) (gain is 1.7 dB at \( f_z \)).

Set \( R_{iz} = 50K \)

Zero 2 at 162 Hz: \( C_i = 1/(\omega_{z2}R_{iz}) = 1/2\pi 162 \times 50K = .02 \mu F \)

Pole 2 at 1590 Hz: \( R_{ip} = R_{iz}/(R_{iz}\omega p^2 C_i - 1) = 50K/(50K \times 2\pi 1590 \times .02) = 5.6K \)

1.7 dB (1.22) gain at 162 Hz: \( R_{fz} = 1.22(R_{ip} + R_{iz}) = 68K \)

Zero 1 at 162 Hz: \( C_f = 1/(\omega_{z1}R_{fz}) = 1/(2\pi 162 \times 68K) = .0144 \mu F \)

Pole 1 at 0 Hz: Omitting \( R_{fp} \) (open), \( \omega_{p1} = 0 \). Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

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Example 5: 12 Volt, 240 Watt Output

All power circuit parameters are the same as Example 4.

Basic Equations — Voltage Feedforward

\[ D = \frac{V_c}{V_s}, \quad V_s = \frac{V_{in}}{K}, \quad K = \frac{V_{in}D}{\max V_c} \]

DC Relationships:

1. \[ V_o = V_{in}D = KV_c \quad (1a) \quad V_c = \frac{V_o}{K} \]

Control to Output Gain:

2. \[ \frac{V_o}{V_c} = K H_e(s). \quad H_e(s) = \frac{1 + s/\omega_0}{1 + (s/\omega_0)/Q + (s/\omega_0)^2}, \quad \omega_0 = \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_C} \]

Line to Output Gain:

3. \[ \frac{V_o}{V_{in}} = 0 \quad \text{Inherent good line regulation} \quad Q = \frac{R_0}{\omega_0 L} \]

Corner Frequencies from Equation (2):

\[ f_o = \frac{1}{(2\pi\sqrt{LC})} = 325 \text{ Hz} \]

\[ f_z = \frac{1}{(2\pi R_C C)} = 39.8/R_C = 1590 \text{ Hz at } 25 \text{ m}\Omega, \quad 7950 \text{ Hz at } 5 \text{ m}\Omega \]

Low Frequency Gain from Equation (2) (max \( V_c = 3.5 \text{ V for UC1840}):\n
\[ K = \frac{V_{in}D}{\max V_c} = 30 \times 0.5/3.5 = 4.29 \quad \text{(feedforward factor)} \]

\[ \frac{V_o}{V_c} = \frac{V_{in}}{5} = 4.29 (12.6 \text{ dB}) \text{ at } 30 \text{ to } 60 \text{ V in.} \]
Error Amplifier Compensation:

Control I.C.: UC1840
Crossover frequency (0 dB loop gain):
\[ f_c = \frac{f_s}{4} = 10 \text{ kHz} \]

E/A gain needed at 10 kHz = 31 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at \( f_0 \) are compensated by two zeros at \( f_z = \frac{f_0}{2} \). This provides additional phase shift at \( f_0 \) for sudden second order transition.

\[ f_z = \frac{325}{2} = 162 \text{ Hz} \]

ESR zero, \( f_z \), is canceled by pole \( f_p \) at least 5 times above \( f_0 \) to avoid adding more phase lag at \( f_0 \). This happens to coincide with min. ESR zero, \( f_z \).

\[ f_p = 1590 \text{ Hz with 31 dB gain} \]

E/A gain required at \( f_z \) is:

\[ 31 - 20\log(1590/162) = 11.2 \text{ dB} \]

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ (1a) \quad V_c = \frac{V_o}{V} = \frac{12}{4.29} = 2.8 \text{ V constant DC.} \quad \Delta V_c = 0 \]

DC Output voltage error is theoretically zero. Loop gain is required only for good dynamic response.

Implementation: Circuit of Appendix A-2 (omit \( R_p, C_p \) and \( R_{fp} \))

Voltage feedforward factor, \( K \), in UC1840 is set by an independent ramp generator whose slope varies proportional to \( V_{in} \). Minimum ramp charging current of 30 \( \mu A \) is chosen, near the bottom of the optimum range.

\[ R_T = \min V_{in}/\min I_T = 30/30\mu A = 1M \]

\[ \frac{dv}{dt} = I_T/C_T = V_{in}/R_T C_T = \max v_o/t_{on}. \quad R_T C_T = V_{inton}/\max v_o = K/f \]

\[ C_T = K/fR_T = 4.29/(40Kx1M) = 107 \text{ pF} \]

Set \( R_{iz} = 50K \). With gain appx. 4 at 162 Hz (\( f_z \)), \( R_f \) of 200K is OK to drive.

Zero 2 at 162 Hz: \( C_i = 1/(\omega z_2 R_{iz}) = 1/2\pi 162 \times 50K = .02 \text{ \mu F} \)

Pole 2 at 1590 Hz: \( R_{ip} = R_{iz}(R_{iz}\omega p_2 C_i - 1) = 50K/(50K \times 2\pi 1590 \times .02) = 5.6K \)

11.2 dB (3.63) gain at 162 Hz: \( R_{fp} = 3.63(R_{ip} + R_{iz}) = 202K \)

Zero 1 at 162 Hz: \( C_f = 1/(\omega z_1 R_{fp}) = 1/(2\pi 162 \times 200K) = .0049 \text{ \mu F} \)

Pole 1 at 0 Hz: Omitting \( R_f \) (open), \( \omega p_1 = 0 \). Actual pole occurs at 80 dB gain limit of UC1840 error amplifier at a frequency below 1 Hz.
Example 6: 12 Volt, 240 Watt Output

All power circuit parameters are the same as Example 4.

Basic Equations — Current Mode Control:

\[ I_L = K V_C, \quad K = \frac{\text{max} I_L}{\text{max} V_C} \]

DC Relationships:

\[ (1) \quad V_O = I_L R_O = K V_C R_O \]

\[ (1a) \quad V_C = \frac{V_O}{K R_O} \]

Control to Output Gain:

\[ (2) \quad \frac{V_O}{V_C} = K R_O \cdot H_e(s), \quad H_e(s) = \frac{1 + s/\omega_p}{1 + s/\omega_z}, \quad \omega_p = \frac{1}{R_O C}, \quad \omega_z = \frac{1}{R_C C} \]

Line to Output Gain:

\[ (3) \quad \frac{V_O}{V_{in}} = 0 \quad \text{Inherent good line regulation and audio susceptibility} \]

Corner Frequencies from Equation (2):

\[ f_p = \frac{1}{(2\pi R_O C)} = 66.3 \text{ Hz at 0.6 } \Omega, \quad 6.63 \text{ Hz at 6 } \Omega \]

\[ f_z = \frac{1}{(2\pi R_C C)} = 39.8/R_C \quad = 1590 \text{ Hz at 25 m} \Omega, \quad 7950 \text{ Hz at 5 m} \Omega \]

Low Frequency Gain from Equation (2) (\text{max} V_C clamped to 2.5 V for 25 A Isc):

\[ K = \frac{\text{max} I_L}{\text{max} V_C} = \frac{25}{2.5} = 10 \]

\[ \frac{V_O}{V_C} = K R_O = 6 (15.6 \text{ dB}) \text{ at 0.6 } \Omega, \quad 60 (35.6 \text{ dB}) \text{ at 6 } \Omega \]
BUCK - CONTINUOUS INDUCTOR CURRENT - CURRENT MODE CONTROL

Error Amplifier Compensation:

Control I.C.: UC1846
Crossover frequency (0 dB loop gain):
f_c = f_s/4 = 10 kHz
E/A gain needed at 10 kHz = 12 dB

ESR zero, f_zC, is canceled by pole f_p at max f_z/10. This decade offset increases low frequency gain and adds 45° more phase lag, still leaving 45° phase margin.

f_p = max f_z/10 = 795 Hz
E/A gain required at and below f_p is:
12 + 20log(10000/795) = 34 dB (50)

Total control voltage swing, ΔV_c, needed to maintain constant output voltage V_o with worst case line and load variation is (from Eq. 1a):

(1a) \[ V_c = \frac{V_o}{K_R} = \frac{12}{10R_o} = 0.2 \text{ to } 2 \text{ V}, \quad \Delta V_c = 1.8 \text{ V} \]

Output voltage error with actual E/A gain of 50 (34 dB)

\[ \Delta V_o = \Delta V_c/50 = 36 \text{ mV} \ (0.3\% \text{ regulation}) \]

Implementation: Circuit of Appendix A-1 (omit R_p and C_p)

Current control factor, K = 10, in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor R_s.

K = I_L/V_c = 10 = 1/(3R_s). \quad R_s = 1/30 = .033 \Omega

UC1846 error amplifier gain limit is >80 dB with R_f >30K. 34 dB needed, OK

Gain required at and below f_p = 795 Hz is 50 (34 dB) = R_f/R_1.

Let R_f = 500K, \quad R_1 = R_f/50 = 10K

1 Pole at f_p = 795 Hz. \quad C_f = 1/(2nf_pR_f) = 400 pF

Slope compensation: Current downslope is 4A/20µs, or 5A projected over 25 µs period, equating to 5x.033 = .165 volts p-p at input of current sense amplifier. Compensation ramp should be .165/2 = .082 V positive ramp. UC1846 oscillator ramp is 2 V. A 24:1 divider provides .083 V. Put 1K between current sense R_s and current sense amplifier input, and 24K from timing capacitor C_t to current sense ampl. input.

2C-12

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Example 7: 12 Volt, 60 Watt Output

\[ f_s = 80 \text{ kHz}, \ T = 12.5 \mu \text{sec} \]

\[ V_{in} = 12 \text{ to } 24 \text{ V} \]

\[ V_o = 12 \text{ V}, \ I_o = 0.5 \text{ to } 5 \text{ A} \]

\[ R_o = 24 \text{ to } 2.4 \text{ Ohms} \]

\[ I_{SC} = 6 \text{ A Short Circuit Limit} \]

Continuous Current Mode Boundary:

- \( \text{Min. } I_o = 0.5 \text{ A} \)
- \( D = \frac{V_o}{V_o+V_i} = 0.33 \text{ to } 0.5 \)
- \( \text{Max. } AIL = 2(\text{minI}_o)/(1-D_{\text{min}}) = 1.5 \text{ A} \)
- \( t_{\text{off}} = 12.5(1-D) = 8.33 \mu \text{sec} \text{ max} \)
- \( L = \frac{V_o t_{\text{off}}}{AIL} = 12 \times 8.33/1.5 = 72 \mu \text{H} \)
- \( I_{\text{IL max}} = \max I_o/(1-D_{\text{max}}) = 10 \text{ A} \)

ESR Max for 0.1 \( V_{pp} \) Ripple at \( I_L = 10 \text{ A} \):

\[ R_C = 10 \text{ m\Omega} \text{ max (2 m\Omega min)}, \ C = 10,000 \mu \text{F} \]

Basic Equations — Duty Cycle Control:

- \( D = \frac{V_C}{V_s} \)
- \( \omega_o = \frac{1-D}{\sqrt{L C}}, \ \omega_z = \frac{1}{R_C C}, \ Q = \frac{R_o}{\omega_o L} \)

DC Relationships:

1. \( V_o = \frac{V_{in} D}{(1-D)} = \frac{V_{in}}{(V_s/V_C-1)} \)

2. \( \frac{V_o}{V_C} = \frac{V_{in}}{(1+V_o/V_i)^2} f_1(s) H_e(s) \)

3. \( \frac{V_o}{V_{in}} = \frac{V_C}{V_s} H_e(s) = \frac{V_o}{V_{in}} H_e(s) \)

Corner Frequencies:

- \( f_o = \frac{(1-D)}{(2\pi\sqrt{L C})} = 94 \text{ Hz at } 12 \text{ V}, 125 \text{ Hz at } 24 \text{ V} \)

- \( f_z (\text{ESR}) = \frac{1}{(2\pi R_C C)} = 1590 \text{ Hz at } 10 \text{ m\Omega}, \ 7950 \text{ Hz at } 2 \text{ m\Omega} \)

- \( f_z (\text{RHP}) = 2728 \text{ Hz at } 12 \text{ V and } 2.4 \Omega, = 7275 \text{ Hz at } 24 \text{ V and } 2.4 \Omega \)

UC1524A ramp \( V_s = 2.5 \text{ V} \). The two outputs of the UC1524A are paralleled.

Low Frequency Gain from Equation (2):

\[ \frac{V_o}{V_C} = 19.2 \ (25.6 \text{ dB}) \text{ at } 12 \text{ V}, \ = 21.6 \ (26.7 \text{ dB}) \text{ at } 24 \text{ V} \]
**Error Amplifier Compensation:**

Control I.C.: UC1524A

Crossover frequency (0 dB loop gain):

\[ f_c = 800 \text{ Hz} \text{ (best achievable - RHPzero)} \]

E/A gain needed at 800 Hz = 11.6 dB

A pole at low frequency (<1 Hz) provides enough gain at low frequencies to meet regulation requirements.

Two second order filter poles at \( f_o \) are compensated by two zeros at \( f_z = f_o \).

\[ f_z = 94 \text{ Hz} \]

E/A gain required at \( f_z \): -7 dB

Two additional poles cancel the ESR zero and right-half-plane zero. The location of these two poles is adjusted by trial and error. Although above the crossover frequency these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

\[ f_p = 2700 \text{ Hz at 22.2 dB gain, } f_p = 8000 \text{ Hz also at 22.2 dB} \]

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ V_c = \frac{V_o}{V_{in}+V_o} = 0.833 \text{ to } 1.25 \text{ V, } \Delta V_c = .417 \text{ V} \]

Output voltage error with actual E/A DC gain of 40 (32 dB at 1 Hz):

\[ \Delta V_o = \Delta V_c/40 = 10 \text{ mV (0.1% regulation)} \]

**Implementation:** Circuit of Appendix A-2 (omit \( R_{fp} \))

UC1524A has transconductance error amplifier (\( gm = .002 \)). Min. load resistance (\( \text{min } R_{fz} \)) is 30K. \( R_{iz} \) is appx. 2x\( R_{fz} \) (gain is -7 dB at \( f_z \)).

Set \( R_{iz} = 100K \)

Zero 2 at 94 Hz: \( C_i = 1/(\omega z_2R_{iz}) = 1/2\pi 94 \times 100K = .017 \mu F \)

Pole 2 at 2700 Hz: \( R_{ip} = R_{iz}/(R_{iz}\omega p_2C_i - 1) = 100K/(100K \times 2\pi 2700 \times .017-1) = 3.6K \)

-7 dB (.45) gain at 94 Hz: \( R_{fz} = .45(R_{ip} + R_{iz}) = 47K \)

Zero 1 at 94 Hz: \( C_f = 1/(\omega z_1R_{fz}) = 1/(2\pi 94 \times 47K) = .036 \mu F \)

Pole 1 at 0 Hz: Omitting \( R_{fp} \) (open), \( \omega p_1 = 0 \). Actual pole occurs at 80 dB gain limit of UC1524A error amplifier at a frequency well below 1 Hz.

Pole 3 at 8000 Hz. \( R_p = R_{ip}/10 = 360 \Omega \). \( C_p = 1/(2\pi f p_3R_p) = .055 \mu F \)
Example 8: 12 Volt, 60 Watt Output

All power circuit parameters are the same as Example 7.

Basic Equations — Duty Cycle Control:

$$I_o = I_L(1-D), \quad I_L = K V_C, \quad K = \max \frac{I_L}{\max V_C}, \quad \omega_Z = \frac{1}{R_C C}, \quad \omega_p = \frac{1+D}{R_C C}, \quad D = \frac{V_{in}}{V_o + V_{in}}$$

DC Relationships:

1. $$V_o = V_{in} D/(1-D) = K V_C R_C \frac{V_{in}}{V_o + V_{in}} \quad \text{(1a)}$$
   
2. Control to Output Gain:
   $$V_c = \frac{V_0(V_0 + V_{in})}{K R_C V_{in}}$$

3. Line to Output Gain:
   $$\frac{V_o}{V_{in}} = \frac{V_o^2}{2 V_o V_{in} + V_{in}^2} \cdot H_e(s)$$
   
   RHP zero: $$f_1(s) = 1 - \frac{\pi}{R} \frac{V_0(V_0 + V_{in})}{V_{in}^2}$$

Corner Frequencies:

- $$f_p = \frac{(1+D)/(2 \pi R C)}{0.884 \text{ Hz at 24 V}, \ 9.95 \text{ Hz at 12 V}, \ 2.4 \Omega}$$
- $$f_z (\text{ESR}) = \frac{1}{(2 \pi R_C C)} = \frac{1590 \text{ Hz at 10 m\Omega}, \ 7950 \text{ Hz at 2 m\Omega}}{2728 \text{ Hz at 12 V and 2.4 \Omega}, \ 7275 \text{ Hz at 24 V and 2.4 \Omega}}$$

Low Frequency Gain from Equation (2):

$$K = \frac{\max I_L}{\max V_C} = \frac{\max I_o}{(1-D)\max V_C} = \frac{6}{(1-0.5)2.5} = 4.8$$

$$\frac{V_o}{V_C} = 57.6 (35.2 \text{ dB}) \text{ at 24 V, 24 \Omega, } \ 3.84 (11.7 \text{ dB}) \text{ at 12 V, 2.4 \Omega}$$

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Error Amplifier Compensation:

Control I.C.: UC1846
Crossover frequency (0 dB loop gain):
\[ f_c = 800 \text{ Hz} \] (best achievable - RHP zero)

E/A gain needed at 800 Hz = 26.4 dB

Two poles cancel the ESR zero and right-half-plane zero. The location of these two poles is set by trial and error. Although above the crossover frequency, these poles are necessary or the gain would stay flat or even rise, causing instability at higher frequency.

\[ f_p = 2700 \text{ Hz at 26.4 dB gain} \]
\[ f_p = 8000 \text{ Hz at 17.1 dB} \]

The E/A gain is flat (26.4 dB) below the first pole at 2700 Hz.

Total control voltage swing, \( \Delta V_c \), needed to maintain constant output voltage \( V_o \) with worst case line and load variation is (from Eq. 1a):

\[ (1a) \quad V_c = \frac{V_o(V_o+V_{in})}{K_{Ro}V_{in}} = 0.156 \text{ to } 2.08 \text{ V}. \quad \Delta V_c = 1.92 \text{ V} \]

Output voltage error with actual E/A DC gain of 20.1 (26.4 dB below 2700 Hz):

\[ \Delta V_o = \Delta V_c/20.1 = 1.92/20.1 = 95 \text{ mV} \] (1% regulation)

Implementation: Circuit of Appendix A-1

Current control factor, \( K = 4.8 \), in the UC1846 is set by the fixed gain (3X) of the current sense amplifier together with current sampling resistor \( R_s \).

\[ K = I_L/V_c = 4.8 = 1/(3R_s). \quad R_s = 0.069 \Omega \]

UC1846 error amplifier gain limit is \( >80 \) dB with \( R_f >30K \). 26.4 dB needed, OK

Gain required (26.4 dB) = 20.9 = \( R_f/R_i \). Let \( R_f = 500K, \ R_i = 500K/20.9 = 24K \).

Pole 1 at \( f_p = 2700 \text{ Hz} \) \quad \( C_f = 1/(2\pi f_p R_f) = 120 \text{ pF} \)

Pole 2 at \( f_p = 8000 \text{ Hz} \) \quad \( R_p = R_i/10 = 2.4K. \quad C_p = 1/(2\pi f_p R_p) = 8200 \text{ pF} \)

Slope compensation: Current downslope is \( 1.5A/8.33 \mu s \), or 2.25A projected over the 12.5 \( \mu s \) period. This equates to 2.25\times0.069 = .155 \text{ volts p-p} at the current sense amplifier input. Compensation ramp should be \( .155/2 = .078 \text{ V} \) positive ramp. UC1846 oscillator ramp is 2 V. A 25:1 divider provides .077 V. Put 1K between current sense resistor \( R_s \) and current sense amplifier input, and 24K from timing capacitor \( C_t \) to current sense amplifier input.

2C-16
Boost regulator topologies have the same general characteristics as their flyback circuit counterparts. The Bode plots have the same shape, and the same type of compensation is employed. The specific values of gain and pole/zero frequencies are slightly different because of modifying factors in the various basic equations: Accordingly, only the basic equations are given for the boost circuits.

**BOOST — Discontinuous Inductor Current — Duty Cycle Control:**

**DC Relationships:**
(1) \( V_o = \text{Vin}(1/2 + \sqrt{1/4 + D^2/J})^{3/2}, \quad D = V_c/V_s, \quad J = 2Ls/R_o \)

**Control to Output Gain:**
(2) \( \frac{V_o}{V_c} = \frac{V_in}{V_s \sqrt{J}} \left( \frac{4-V_in/V_o}{4-V_in/V_o-V_in^2/V_o^2} \right)^{3/2} H_e(s). \quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p} \)

**Line to Output Gain:**
(3) \( \frac{V_o}{V_in} = \frac{V_o}{V_in} H_e(s), \quad \omega_z = \frac{1}{R_o C'}, \quad \omega_p = \frac{2+1/-\sqrt{1+4D^2/J}}{R_o C} \)

**BOOST — Discontinuous Inductor Current — Voltage Feedforward:**

**DC Relationships:**
\( V_s = V_in/K, \quad K = V_inD/\text{max}V_c \)
\( V_o = V_in(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_in^2})^{3/2}, \quad D = V_c/V_s = \frac{K V_c}{V_in}, \quad J = 2Ls/R_o \)

**Control to Output Gain:**
(2) \( \frac{V_o}{V_c} = \frac{K}{\sqrt{J}} \left( \frac{4-V_in/V_o}{4-V_in/V_o-V_in^2/V_o^2} \right)^{3/2} H_e(s). \quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p} \)

**Line to Output Gain:**
(3) \( \frac{V_o}{V_in} = \frac{V_o}{2V_o-V_in} H_e(s), \quad \omega_z = \frac{1}{R_o C'}, \quad \omega_p = \frac{2+1/-\sqrt{1+4D^2/J}}{R_o C} \)

**BOOST — Discontinuous Inductor Current — Current Mode Control:**

**DC Relationships:**
\( I_p = K V_c, \quad K = \text{max}I_p/\text{max}V_c \)
(1) \( V_o = V_in(1/2 + \sqrt{1/4 + (K^2/J)V_c^2/V_in^2})^{3/2}, \quad D = V_c/V_s = \frac{K V_c}{V_in}, \quad J = 2Ls/R_o \)

**Control to Output Gain:**
(2) \( \frac{V_o}{V_c} = \frac{K}{\sqrt{J}} \left( \frac{4-V_in/V_o}{4-V_in/V_o-V_in^2/V_o^2} \right)^{3/2} H_e(s). \quad H_e(s) = \frac{1+s/\omega_z}{1+s/\omega_p} \)

**Line to Output Gain:**
(3) \( \frac{V_o}{V_in} = \frac{V_o}{2V_o-V_in} H_e(s), \quad \omega_z = \frac{1}{R_o C'}, \quad \omega_p = \frac{2+1/-\sqrt{1+4D^2/J}}{R_o C} \)
Boost Configurations — Basic Equations

Boost — Continuous Inductor Current — Direct Duty Cycle Control:

\[ D = \frac{V_c}{V_s}, \quad (1-D) = \frac{V_i}{V_o}, \quad \omega_0 = \frac{1-D}{\omega_0 L}, \quad \omega_z = \frac{1}{R_c C}, \quad Q = \frac{R_o}{\omega_0 L} \]

DC Relationships:

1. \[ V_o = \frac{V_{in}}{(1-D)} = \frac{V_{in}}{(1-V_c/V_s)} \]  \hfill (1a) \[ V_c = \frac{V_o-V_{in}}{V_i} \]

Control to Output Gain:

\[ \frac{v_o}{v_c} = \frac{V_{in}}{V_s} \frac{V_o}{V_i} f_1(s) H_e(s) \]
\[ H_e(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_0)/Q + (s/\omega_0)^2} \]

Line to Output Gain:

\[ \frac{v_o}{v_{in}} = \frac{V_o}{V_{in}} H_e(s) \]  \hfill RHP zero: \[ f_1(s) = 1 - \frac{sL}{R V_i^2} \]

Boost — Continuous Inductor Current — Current Mode Control:

\[ I_o = IL(1-D), \quad IL = KVC, \quad \omega_p = \frac{2}{R_o C}, \quad \omega_z = \frac{1}{R_c C}, \quad D = \frac{V_o-V_{in}}{V_o} \]

DC Relationships:

1. \[ V_o = -\frac{KVC R_0 V_i}{2} \]  \hfill (1a) \[ V_c = \frac{V_o^2}{(KR_0 V_i)} \]

Control to Output Gain:

\[ \frac{v_o}{v_c} = \frac{K R_0}{2} \frac{V_{in}}{V_o} f_1(s) H_e(s) \]
\[ H_e(s) = \frac{1 + s/\omega_z}{1 + (s/\omega_0)/Q + (s/\omega_0)^2} \]

Line to Output Gain:

\[ \frac{v_o}{v_{in}} = \frac{V_o}{2V_{in}} H_e(s) \]  \hfill RHP zero: \[ f_1(s) = 1 - \frac{sL}{R V_i^2} \]

Voltage feedforward control does not perform effectively with continuous mode boost and flyback circuits, and this use is not recommended.