

Design Review: A Step-By-Step Approach to AC Line-Powered Converters

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ABSTRACT

An offline, three-output, 150-W forward converter is used as an example to illustrate the design process for typical isolated converters. This example emphasizes the basics with a double-ended forward topology using coupled inductors for output accuracy. Design issues and trade-off decisions to optimize power efficiency while keeping costs to a minimum are highlighted. Finally, the presentation of measured performance results confirms the design process.

I. INTRODUCTION

One of the most common power supplies today plugs into the AC wall outlet and provides an isolated single or multiple DC voltage output. While designing this power supply may seem elementary, there are many criteria to consider in order to achieve a well-designed system. And if the power supply is not designed properly, it may well attract too much attention by not working.

An offline design can be made easier if some initial conditions are first established. Since the power supply is the heart of the system, the designer must work with the project engineers to determine the power supply requirements, operating environment, cost, and development schedule.

The designer can then proceed with a “plan of record” and begin establishing the details. This plan of record should include a power supply specification agreed upon by the project team.

II. OVERVIEW

A. Defining Requirements

The first step is to define the load. This is an important step, enabling the proper choice of topology, components, and many other details. Output ripple and tolerance are critical to system performance. The output current for each load determines the power requirements, and how that current may vary influences regulation and noise on all outputs.

Load Concerns

- Output voltage(s), tolerance(s) and allowed ripple
- Output current(s), maximum and minimum.
- Transient loading on outputs, di/dt, repetition rate.
- Load capacitance, wiring inductance
- Sequencing of supplied voltages
- Protection features

Input for an offline converter power supply depends upon the countries in which the power supply operates. Input voltage ranges help define the topology, component ratings, and safety certifications. AC line harmonic requirements may require power-factor correction.

Power Train Concerns

- Input voltages for required countries. (Is a 110 V/220 V switch an option?)
- Possible need for power factor correction
- Topology selection
- Control method

And finally, safety and EMI requirements determine the mechanical design, which in turn determines airflow and component temperature. Once all is understood, then the designer can estimate a cost and create a development schedule.

TABLE 1. POWER SUPPLY TOPOLOGY SUMMARY

Topology	Power Level	Benefits	Drawbacks	Cost
Flyback	<100 W	Low parts count Single magnetic Wide input-voltage range Low output power	Poor efficiency at high power levels High peak currents Cross regulation problems High-voltage power switch	Lowest
1 Switch Forward	100 W to 500 W	Medium output power Good cross regulation with coupled inductor Potential for >50% duty-cycle	Limited input range Power Switch = $2 V_{IN}$ Transformer reset	Moderate
2 Switch Forward	100 W to 500 W	Medium output power Power switch = V_{IN} Coupled inductor Clamped transformer reset	Limited input range Top FET drive circuit required 50% duty-cycle limit Larger inductor value	Moderate
Half-Bridge	100 W to 500 W	Medium output power Power switch = V_{IN} Coupled inductor Max duty-cycle < 100%	Limited input range Top FET drive Volt-second balance of transformer Center-tapped secondary	Moderate
Full Bridge	>500 W	Resonant switching can improve efficiency Power switch = V_{IN} Coupled inductor Very high output power Max duty-cycle < 100% Efficient transformer design	4 power switches Top FET drive Volt-second balance	High
Push-Pull	25 W to 200 W	Good core utilization Coupled inductor Both switches ground referenced Small output inductor Max duty-cycle < 100%	Power switch = $2 V_{IN}$ Limited input range Center-tapped primary Volt-second balance	Moderate

B. Defining the Topology

There are many possible topologies to consider, including flyback, forward, half bridge, full bridge and push-pull. All have general areas of optimization. Table I summarizes the choices.

C. Defining the Input Configuration

The power supply input, commonly called the “front end” of an offline supply, has several components:

- line cord/receptacle
- power switch
- fuse
- inrush limiting NTC thermistor (SEM-100)
- EMI filter (SEM-1500),
- input bridge (full wave or voltage doubler)
- bulk capacitance (SEM-100)

There is a wide range of input voltages to consider for worldwide operation and tolerances (usually $\pm 10\%$) must be included! The peak working voltage maximum at the input to the converter is $V_{RMS} \times \sqrt{2}$.

TABLE 2. WORKING VOLTAGES

Area	V_{RMS} (typ)	$\pm 10\%$	Working Voltage (V_{DC})
Japan	100	90 to 110	126 to 154
US	120	108 to 132	151 to 184
Europe	220	198 to 242	277 to 339
Australia/India	230	207 to 264	289 to 370

The range for a universal input power supply is then $90 V_{RMS}$ to $264 V_{RMS}$. Wide ranging operation without a line-select switch is possible at power levels less than 100 W. While it may be technically possible to operate above 100 W over the wide input-voltage range, circuit losses and

limitations that increase cost usually dictate a 110 V/220 V switch (Fig. 1) to select a full-wave bridge or voltage-doubler configuration. When closed, the switch enables the circuit to double the 110 V/120 V input, thus making the DC working voltage approximately the same as it would be for 220 V/230 V input with the switch open.

TABLE 3. BULK RECTIFIED DC VOLTAGE

With Only Full Wave Bridge (V_{DC})	With Doubler for Low Range (V_{DC})
126 to 154	252 to 308
151 to 184	302 to 368
277 to 339	277 to 339
289 to 370	289 to 370

Thus the DC input range is usually considered to be 252 V_{DC} to 370 V_{DC} .

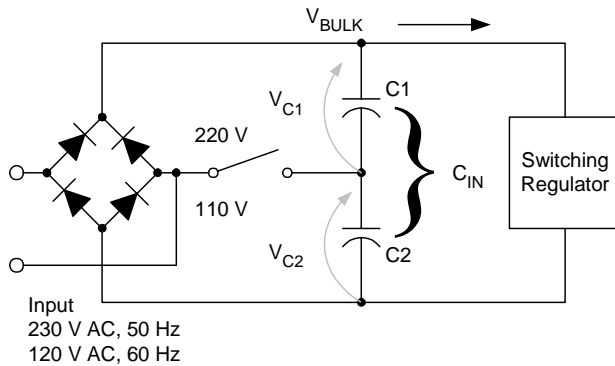


Fig. 1. A voltage doubling input range switch configuration.

D. Transformer Design

After the topology and input configuration are chosen, the transformer is considered. Each topology has different areas of concern that affect the design. Flyback designs may operate in continuous or discontinuous conduction mode, which has an impact on duty cycle and turns ratios. Forward-converter design turns ratios are determined by the input and output voltage ratios. Each has similar core and winding loss considerations

E. Voltage-Mode or Current- Mode Control

There are advantages to both peak current-mode and voltage-mode control in converter design. Average current-mode is seldom used in isolated converters, since it requires a continuous

signal usually associated with the current in the output inductor.

The advantages of peak current-mode control include fast response to input variations, inherent current limiting and easier loop compensation. However, voltage-mode control does not have the limitations of minimum load and leading-edge spike that current mode has. That advantage allows stable operation at light loads and is one reason some offline converters requiring large load variances may use voltage-mode control. Also, voltage-mode does not require a current-sense element that may increase the cost. However it is always desirable to have primary-current protection in an offline converter. Since the working DC bulk voltage is on the order of 340 V_{DC} , there is a large amount of primary power available. For this reason, voltage mode PWM's may have added protective features such as voltage feed-forward, current sense, duty-cycle clamp, and volt-second clamps to limit the input power. [2]

F. Output Filter Design

A flyback output filter in its simplest form is simply a storage capacitor which must handle the high charge currents during the flyback period, and also support the entire output during the primary on-time. Designers often add an L-C filter after the first capacitor in order to reduce the high-frequency ripple voltage caused by the high peak current.

A forward converter output filter consists of an inductor (that acts as a current source and averages the secondary winding voltage) followed by a capacitor for storage. The capacitor only sees the ripple current of the inductor and does not need to support the output during the primary on-time.

Both flyback and forward converter specifications must detail the output ripple voltage and the allowable regulation window. A load-step variation on an output causes its output to drop by the resistive effects, output inductance, and loop response time. The load step should be defined in the specification together with the limits of allowable output voltage variation.

III. THE DESIGN PROCESS

A simple three-output, 150-W, universal input powered supply is selected to illustrate the design process. This type of power supply is found in many home personal computers, but the description that follows should be helpful for a wide range of similar applications and at different power levels.

A. Defining the Requirements (Plan of Record)

The official power-supply specification document contains the details of what the supply is intended to do. The minimum requirements for this example are:

- 3 outputs required
 - +5 V ($\pm 5\%$) at 18 A (90 W), 5 A typical, 2 A minimum, 3-A load step.
 - +3.3 V ($\pm 5\%$) at 5 A (16.5 W), 2.5 A typical, 1 A minimum, 1-A load step.
 - +12 V ($\pm 10\%$) at 3 A (36 W), 2 A typical, 1 A minimum, 2 A load transient.
- Total maximum power output = 144 W
- Typical power output = 60 W (Typical values reflect a standard configuration.)
- Minimum output power = 25 W
- Efficiency $\geq 80\%$
- Ripple voltage = 1% p-to-p V_{OUT} , for 5 V and 3.3 V
- Ripple voltage = 2% p-to-p V_{OUT} for 12 V
- Input voltage: Worldwide AC operation, 50/60Hz, voltage select switch acceptable, no power factor required
- Safety approvals: EN 60950, UL, CSA
- EMI: FCC CLASS B, CISPR22
- Frequency <140 kHz for EMI considerations: use 100 kHz

B. Defining the Topology and Control Method

Because the cost benefits of a flyback design begin to diminish at power levels above 100 W, a forward topology appeared an optimal choice particularly in consideration of the savings that a coupled inductor might offer when multiple outputs are required. A single switch or two-switch forward converter are good candidates and either can be implemented at this power level

with lower costs that either the half-bridge or the full-bridge.

A single-switch forward converter is usually limited to a 50% duty cycle to allow time for the transformer to reset its volt-second product. In a single-switch design, a reset winding is commonly used to clamp the reset voltage to acceptable levels. The power FET then sees approximately $2 \times V_{IN}$. At high input this voltage can exceed 740 V (1000 V likely), leading to an 800-V FET minimum. Push-pull designs also have the problem of at least $2 \times V_{IN}$ voltage rating. Since this requirement can be expensive, an alternative “double-ended” approach is preferable.

A two-transistor forward design (as shown in Fig. 2) uses a FET at each end of the transformer primary to connect to the positive rail and ground. When they turn off during the reset period, each end of the primary winding *automatically* traverses to the opposite rail, thus placing the opposite polarity on the winding to satisfy the volt-second equalization. No clamp winding is needed, and instead, only clamping diodes are required. This means that each power-FET can now be rated at the positive rail voltage of 370 V, allowing use of a pair of much less expensive 500-V FETs.

The potential cost saving (per Digi-key 1-k pricing) is shown in Table IV:

TABLE 4. POWER FET PRICE COMPARISON

Part	Current (A)	Voltage (V)	Resistance (Ω)	Price (\$)
IRF840	8	500	0.85	0.91
IRFPG50	6	1000	2.00	3.98

A two-switch forward design is a reasonable approach for this power level, considering efficiency and cost goals. Its clamped transformer voltage operation, with a maximum duty cycle of 50%, allows easy reset of the transformer core and allow lower-voltage FETs to be used in the power stage.

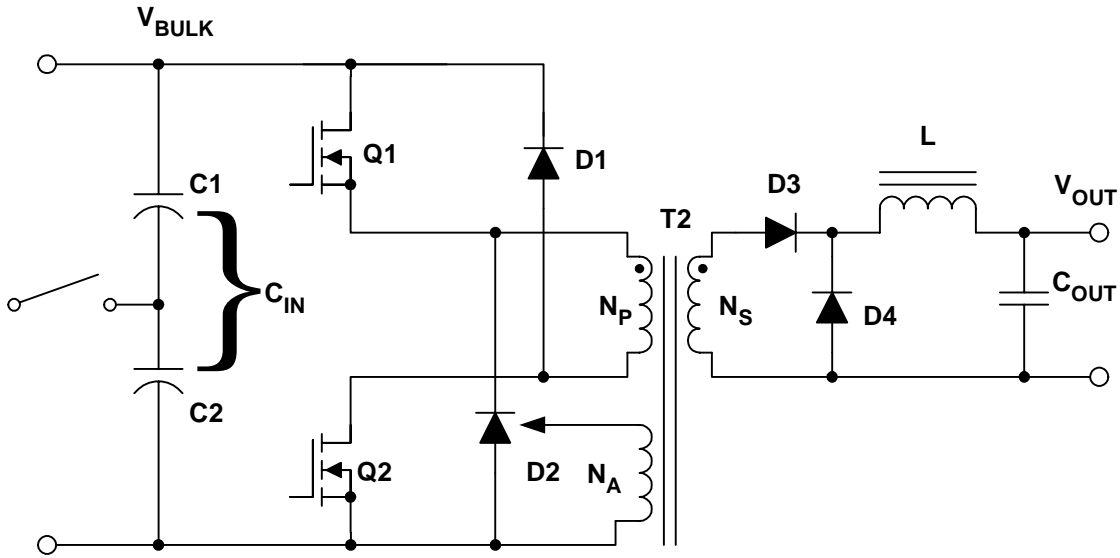


Fig. 2. Two-Switch Forward Converter

The load ratio of 144 W/25 W is 6:1, so at the minimum load there is still enough current ramp for a quality signal into the PWM comparator. This signal allows current-mode control, which includes three advantages: (1) compensation of the output L-C double-pole; (2) input feed-forward; and (3) primary pulse-by-pulse current limit.

C. Defining the Input Section

Voltage Doubler vs. Full-Wave Bridge Input

The justification for the voltage doubler is substantiated by examining the impact of a wide input voltage range on the voltage ratings required for the semiconductors, most notably at the outputs. This analysis starts at the main 5-V output and works backwards to the input, because the control loop is closed on the 5-V output since it is also the highest current output. Allowing for a schottky diode drop in the output stage (0.6 V), this design requires 5.6 V at the transformer output. The duty cycle is 50% maximum (use 45% for margin) at low-line input from which a minimum secondary voltage is derived.

$$V_{SEC(min)} = \frac{V_{OUT}}{Duty(max)} = \frac{5.6 V}{0.45} = 12.44 V$$

The estimate of maximum secondary voltage is determined by the ratio of input voltage to V_{SEC} . Without the doubler, a standard AC input bridge produces:

$$V_{DC(min)} = 90 V_{RMS} \times 1.4 = 126 V(peak)$$

$$V_{DC(max)} = 264 V_{RMS} \times 1.4 = 370 V(peak)$$

$$V_{SEC(max)} = \frac{V_{DC(max)}}{V_{DC(min)}} \times V_{SEC(min)} = \frac{370}{126} \times 12.44$$

$$= 36.5 V \text{ (with } 2 \times \text{derating, } 80 V \text{ diode required)}$$

The following equations estimate the maximum secondary voltage using the input voltage doubler with the doubler switch closed for 110-V operation and open for 220-V operation:

$$V_{DC(min)} = 90 V_{RMS} \times 2 \times 1.4 = 255 V(peak)$$

$$V_{DC(max)} = 132 V_{RMS} \times 2 \times 1.4 = 370 V(peak)$$

Calculate the lower value for 220-V operation with doubler OFF using $(220-10\%) = 198$ for $V_{DC(min)}$:

$$V_{DC(min)} = 198 \times 1.4 = 277 V(peak)$$

Calculate the upper value for 220-V operation with doubler OFF using $(200+10\%) = 264$ for $V_{DC(max)}$.

$$V_{DC(max)} = 264 V_{RMS} \times 1.4 = 370 V(peak)$$

$$V_{SEC(max)} = \frac{V_{DC(max)}}{V_{DC(min)}} \times V_{SEC(min)} = \frac{370}{255} \times 12.44 \text{ V} = 18.0 \text{ V}$$

(with 2x derating only a 40 V diode is required)

An 80-V, 30-A dual schottky diode typically costs substantially more than a 40-V device. The same premium can generally be applied to the rectifiers for the other two outputs.

TABLE 5. DIGIKEY 1-K PIECE PRICING

Part	Current (A)	Voltage (V)	Price (\$)
IR 30CPQ040	30	40	1.83
IR 30CPQ080	30	80	2.93

Other concerns that may increase cost when not using the doubler are

- increased flux density in the transformer due to lower number of primary turns required to meet the $V_{secondary}$ minimum at low AC input, resulting in a more expensive and possibly larger core
- larger output inductor value due to the longer off time caused by low duty cycle at high AC input
- higher snubber losses due to higher voltages in the secondary at high AC input
- higher current ratings due to higher primary current at low AC input

When all is considered, it is desirable to design with the doubler switch for 110-V AC operation.

Input Capacitors

SEM-100 Topic 1. [3] provides the guidelines for sizing the input capacitors,

The key concern is the DC voltage decay during the time the input rectifier is not conducting (see Fig. 3). The value of the input capacitor helps reduce the voltage drop, but at the cost of a physically larger capacitor. The final lowest decayed voltage, V_{MIN} must be used as the minimum voltage to calculate the transformer turns ratios. A common standard is a ripple voltage ($V_{PK} - V_{MIN}$) 20% to 30% of the V_{PK} . The design process is the following:

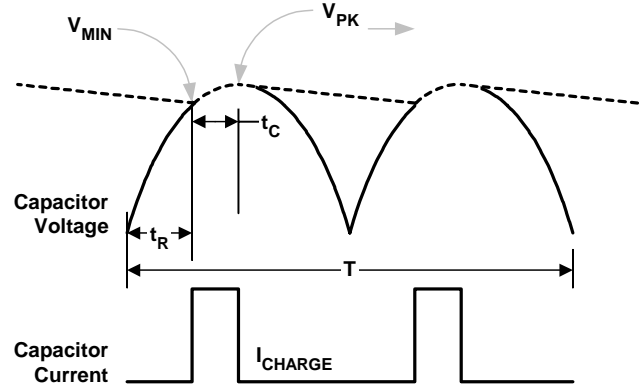


Fig. 3. Input Capacitor Waveforms

Calculate the input power required.

$$P_{IN} = P_{OUT} \times \eta = \frac{144 \text{ W}}{0.80} = 180 \text{ W}$$

Calculate the input energy required for a full-wave bridge with the doubler switch open.

$$W_{IN} = \frac{P_{IN}}{f_{LINE}} = \frac{\left(\frac{P_{OUT}}{\eta} \right)}{f_{LINE}} = \frac{\left(\frac{144 \text{ W}_{OUT}}{0.80} \right)}{50 \text{ Hz}} = 3.60 \text{ Joules}$$

$$C_{IN} = \left[\frac{W_{IN}}{(V_{PK})^2 - (V_{MIN})^2} \right]$$

where V_{PK} is the lowest peak voltage on two bulk capacitors in series in 220-V mode:

$$\begin{aligned} V_{PK(220V)} &= V_{RMS(min)} \times 1.414 \\ &= (220 \text{ V} - 10\%) \times 1.414 \\ &= 280 \text{ V} \text{ (use 275 to be conservative)} \end{aligned}$$

$$\begin{aligned} V_{MIN(220V)} &= V_{PK(220V)} - V_{RIPPLE} = (275 \text{ V} \times 0.75) \\ &\text{(use 25\% ripple to be conservative)} \\ &= 206 \text{ V} \end{aligned}$$

Now, solve for capacitance:

$$\begin{aligned} C_{IN} &= \left[\frac{W_{IN}}{(V_{PK})^2 - (V_{MIN})^2} \right] = \frac{3.60}{(275)^2 - (206)^2} \\ &= 108 \mu\text{F} \end{aligned}$$

Since this design uses a doubler, two 220- μF capacitors would be used in series.

However, in the doubler mode, one capacitor is being charged while the other is discharged at 60 Hz. To determine the value of C1 and C2 needed in this case, use the following equations:

$$W_{IN} = \frac{P_{IN}}{f_{LINE}} = \frac{\left(\frac{144 \text{ W}}{0.80}\right)}{60\text{Hz}} = 3.00 \text{ Joules}$$

$$C1 = C2 = \left(\frac{W}{\left[(V_{CPK})^2 - (V_{C(\min)})^2 \right]} \right)$$

where

- V_{CPK} is the lowest peak voltage on the individual bulk capacitors in 110-V mode
- $V_{C(\min)}$ is approximated using the same $V_{(\min)}$ as the non-doubler and a new V_{CPK}' calculated as

$$\begin{aligned} V'_{CPK(110V)} &= V_{RMS(\min)} \times 1.414 \\ &= (100V - 10\%) \times 1.414 \\ &= 127V \text{ (use 125 to be conservative)} \end{aligned}$$

$$V_{C(\min)} = \frac{(2V_{MIN} - V'_{CPK})}{3} = \frac{(2 \times 206 - 125)}{3} = 96V$$

$$\begin{aligned} C1 = C2 &= \left(\frac{W}{\left[(V'_{CPK})^2 - (V_{C(\min)})^2 \right]} \right) \\ &= \left(\frac{3.00 \text{ J}}{\left[(125)^2 - (96)^2 \right]} \right) = 470 \mu F \end{aligned}$$

Therefore, the low-line, doubler-mode storage requirement defines the capacitor selection and, again being conservative, choose the next standard value of 560 μF . More capacitance can be used if missing cycle holdup is required.

Finally, since the capacitors are in series, balancing resistors are needed to keep the voltages divided between them. The balancing resistors override the potential internal capacitor leakage current as specified by the capacitor data sheets. This design uses a 44-k Ω , 1-W balancing resistor for the top capacitor and a 39-k Ω , 1-W balancing resistor in series with the PWM controller on the bottom, to provide a 2-mA balancing current. The 39-k Ω resistor also provides the PWM startup current, as demonstrated later in the paper. The lower resistor is smaller, because it is connected to a 12-V PWM V_{CC} zener clamp, so the voltage across it is less, but it still must sink the same amount of current as the top resistor.

D. Transformer Turns Ratio

Since the currents are highest in the secondary, the goal is to use minimal number of turns to keep resistive I^2R losses to a minimum. Once the minimum number of secondary turns are determined, then proceed to primary turns calculations.

Secondary Turns

Non-fractional turns ratios enable easy construction. Minimum turns on the high-current winding minimize winding resistive loss. Finding integer multiples involves comparing the ratios of the voltages with the number of turns that gets closest to those ratios. The following relation must be followed:

$$\frac{V1}{V2} = \frac{N1}{N2}$$

A common iteration process starts with one turn on the main output, and then (on the basis of volts per turn) calculates the number of turns required for the other outputs. The number of turns is incremented until integer multiples that satisfy the output regulation are found.

This design requires minimum turns on the high current 5-V winding, and good cross regulation to the 3.3-V winding, since these windings have the tightest tolerances. Assuming that 0.6-V V_F schottky rectifiers are used for both, a 5.6/3.9 or 1.46:1 ratio, or inversely a 1:0.70 turns ratio can be used. The following chart shows a winding evaluation:

TABLE 6. TRANSFORMER WINDINGS

5.6 V Turns	V/Turn	Turns To Yield 3.9 V	Effect
1	5.6	3.9/5.6=0.70	fractional
2	2.8	3.9/2.8=1.4	uneven
3	1.867	3.9/1.867=2.09	workable

The last option provides a good ratio, with 3 turns producing 5 V and 2 turns producing 3.3 V. This selection allows low turns on 5 V to get low winding losses, and good regulation for a 3.3 V output.

For a 12-V winding at 1.867 V/T, and using 0.9 V for the diode V_F , the ratio of 12.9/1.867 = 6.9 turns, is calculated, therefore use 7 turns.

Since 1.867 x 7 = 13.07 V, the resultant 12-V output is 13.07 - .9 = 12.17 V, or a +1.4% set point.

Primary Turns

Primary turns are determined by the input voltage range, duty cycle, and peak voltage allowed to the output rectifiers.

The maximum V/T of the secondary is derived from the maximum allowable voltage to the secondary rectifier divided by the number of secondary turns. Minimum V/T is derived from the maximum allowable duty cycle that can regulate the output voltage at the lowest input voltage. This calculation yields two limits where both requirements must be satisfied. Primary turns are then determined by the input voltage range and the peak voltage to be allowed on the output rectifiers.

Based on the earlier discussion of the diode voltage ratings, the maximum voltage on the 5-V diode is 19.8 V. A 40-V diode provides more headroom than necessary, and for purposes of these calculations was derated to 25 V for a 25 V/3 T = 8.3 V/T maximum.

The minimum number of primary turns ($N_{P(\min)}$) is determined by dividing the high-line input voltage by the maximum number of volts per turn of the secondary winding.

$$N_{P(\min)} = \frac{V_{IN}}{[V/T]} = \frac{370}{8.3} = 44 \text{ turns at high line}$$

Fewer primary turns are not acceptable, because the 25-V limit established for the 5-V diode would be exceeded.

The low-line diode input must be 5.6 V/45% duty cycle = 12.4 V.

The maximum V/T is 12.4 V/3T = 4.13 V/T and the low line input is $V_{\text{MIN}} = 216 \text{ V}$.

$$N_{P(\max)} = \frac{V_{IN}}{[V/T]} = \frac{216}{4.13} = 52 \text{ turns at low line}$$

More primary turns are NOT acceptable because the PWM maximum duty cycle limit could no longer regulate the output voltage.

Therefore, a 52-turn primary winding satisfies the low-line maximum duty cycle limit and remains within the voltage limits of the 5-V output diode. The secondary winding uses three turns for 5 V, 2 turns for 3.3 V, and seven turns for 12 V. However, in the actual transformer, the primary turns were reduced to 51 to fit in the core window area. Adding a 12-V PWM bias winding powers the selected PWM control circuitry with the same number of turns as the secondary 12-V output.

The transformer design should continue per guidelines set forth in the *Unitrode Magnetics Design Handbook*, (MAG100A)[1] and other application material, but that is beyond the scope of this paper. Cooper Coiltronics completed the transformer construction, with the turns ratios, output currents and operating frequency that were derived in the generation of this design.

The following are the final transformer parameters:

- Primary inductance = 2.3 mH
- Primary turns = 51, 2 windings paralleled with secondaries in between.
- 5 V = 3 T, 8.8 mΩ, copper strap
- 3.3 V = 2 T tapped off the 5-V winding, 2.2 mΩ
- 12 V = 2- 7 T windings in parallel. 22 mΩ, bifilar wound
- 12-V bias winding = 7 T
- ERL28 ferrite core
- Coiltronics # CTX16-16690

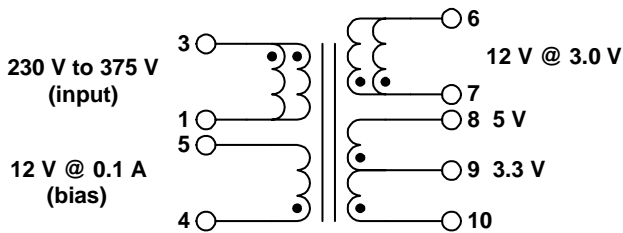


Fig. 4. Transformer schematic.

E. Output Inductor

Forward converters allow a useful technique for improved cross regulation, called the *coupled inductor*, in the output stage. Each output requires an inductor, and building on a common core greatly aids cross regulation and saves space. Regulation and ripple current can be *steered* or *adjusted* by the order of the windings on the core and by leakage inductance. The turns ratio of the coupled inductor must be the same as the transformer turns ratio, or the secondary winding has a shorted turn. Output inductor design methods in (MAG100A), Topic R5[1], base the minimum output inductor value on the minimum load specification of the output toward which the ripple current is steered, in order to maintain continuous current in the inductor. This approach is helpful in maintaining a closed-voltage loop gain for good transient response.

TABLE 7. CURRENT MINIMUM

Output Option	I _{MIN} (A)
3.3 V	1.0
5 V	2.0
12 V	1.0

It is desirable to keep the inductor current continuous for loop response concerns. The inductor operates in discontinuous mode if the minimum average current is less than half the peak-to-peak ripple current. Therefore, the peak-to-peak ripple current must be twice the minimum average current. For this example, the ripple current will be steered to the 12-V output. Here, I_{MIN} is 2 A and the ripple current can be:

$$I_{P-P} = 2 \times I_{MIN} = 2.0 \text{ A}$$

The current required during the maximum PWM OFF time determines the inductance value:

$$L = V \times \frac{dt}{di}$$

where

- di is the peak to peak ripple current (2 A)
- V is the applied voltage on the inductor during the OFF time (V_{OUT} of 2 V plus the rectifier drop of 13.07 V as determined earlier)
- dt is determined from the worse case minimum duty cycle (maximum OFF time) on the output where the loop closed, in this case, the 5-V output

$$Duty \text{ Cycle}(\min) = \frac{V_{OUT}}{V_{IN(\max)}} \times \frac{N_P}{N_S}$$

$$t_{OFF} = (1 - D_{MIN}) \times \left(\frac{1}{f_{SW}} \right)$$

To calculate the duty cycle at 100 kHz,

$$Duty \text{ Cycle}(\min) = \left(\frac{5.6}{370} \right) \times \left(\frac{51}{3} \right) = 27\%$$

- t = 2.7 μs
- t_{OFF} = 7.3 μs

As seen on the 5-V winding,

$$L = V \times \frac{dt}{di} = \frac{13.07 \times 7.3 \mu s}{2.0 \text{ A}} = 47.7 \mu H \text{ (use } 50 \mu H)$$

Although the minimum inductor value is 50 μH , a larger one can be used to lower the peak-to-peak ripple current and also allow a lower minimum load. Lowering the ripple current benefits the output voltage ripple, since the inductor ripple current times the ESR of the output capacitors largely determines the output ripple voltage. It should be noted that a higher inductor value, while potentially reducing the cost of the output capacitors, comes with the penalty of slower response to sudden load changes.

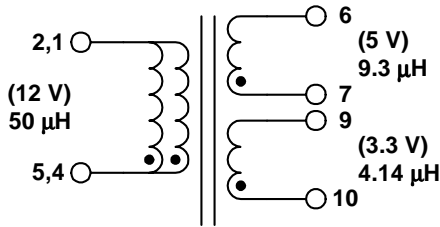


Fig. 5. Inductor schematic.

The order of the windings is determined in order to steer the ripple current to 12 V and to keep the leakage inductance between the 3.3-V and 5-V windings low, ensuring good cross regulation. The inductance for both the 5-V and 3.3-V outputs result from the relationship of the turns ratio squared. The 12-V winding was wound first, a 5-V copper strap was second, and 3.3 V was wound on the outside. The designer can experiment with different winding arrangements to affect ripple current steering and cross regulation.

The final inductor values and winding order are shown in Table VIII. This inductor was made for us by Coiltronics as CTX16-16691.

F. Output Capacitors

Output capacitors are selected on the basis of ESR, required value, physical volume, and the RMS ripple current each can accommodate.

Capacitor Equivalent Series Resistance (ESR)

The major component of the output ripple is the inductor ripple current impressed upon the ESR of the capacitor as:

$$\%V_{RIPPLE} = \frac{I_{RIPPLE} \times R_{ESR}}{V_{OUT}}$$

Since the choice was made to steer the ripple current to the 12-V output, its ripple current will be higher, while that on the other two outputs will be lower than predicted. However, since quantifying this steering function is difficult, the maximum ESR values will be calculated for each output independently as follows. For the 12-V winding, with a minimum load of 1-A_{DC}, (p/p) and a 2% ripple specification:

$$R_{ESR(max)} = \frac{2\% V_{OUT}}{I_{MIN(p-p)}} = \frac{240 \text{ mV}}{2 \text{ A}} = 120 \text{ m}\Omega \text{ (12V output)}$$

$$R_{ESR} = \frac{50 \text{ mV}}{4 \text{ A}} = 12.5 \text{ m}\Omega \text{ (5V output)}$$

$$R_{ESR} = \frac{33 \text{ mV}}{2 \text{ A}} = 16.5 \text{ m}\Omega \text{ (3.3 V output)}$$

These are the maximum ESR values that each output capacitance is allowed. ESRs of capacitors in parallel add ESR in parallel, such that a lower ESR value is achieved by placing multiple capacitors in parallel, which may also lower the cost.

TABLE 8. COUPLED INDUCTOR WINDINGS
ER28L FERRITE CORE, 1.45 MM GAP

Winding Order	V _{OUT}	Turns	L Value (μH)	Reistance ($\text{m}\Omega$)	Material
1	12 V	21	50	53	4 strands bifilar
2	5 V	9	9.3	6	Copper strap
3	3.3 V	6	4.14	2.5	Copper strap

Capacitor Value

This is a large-signal hold-up time requirement for step-load response.

The 5-V capacitor is determined first because the loop is closed on 5-V winding.

A load variation (ΔI) on an output causes a voltage variance (dV) on the basis of the time it takes the loop to respond (dt) and the output capacitance (C). For simplicity, disregard the ESR and ESL effects.

$$dV = \frac{\Delta I}{C} \times dt$$

The minimum allowable capacitance is determined by the loop response time and allowable output voltage variation as shown below:

$$C = \Delta I \times \frac{dt}{dV}$$

The allowable voltage variation is the total output tolerance minus the error amplifier set-point tolerance. A 1% reference and 1% resistors in the divider, provide a 2% $V_{SETPOINT}$.

The allowable variation ($\%V_{OUT}$) of the 5-V output is 5%.

$$\begin{aligned} dV &= V_{OUT} (\%V_{OUT} - \%V_{SETPOINT}) \\ &= 5V(0.05 - 0.02) = 5V(0.3) = 150mV \end{aligned}$$

The value dt is the loop response time, during which the capacitor holds up the output voltage until the loop can respond. The reasonable practical maximum that the loop can be crossed over is $f_{SW}/10$. At 100 kHz this is 10 kHz or 100 μs response time. 5 kHz or 200 μs is used for margin.

The load step ΔI is defined in the specification as 3 A.

$$C = \Delta I \times \frac{dt}{dV} = 3A \times \frac{200\mu s}{150} = 4000\mu F$$

This same parameter is harder to calculate on the 3.3-V and 12-V windings, since their regulation is aided by the coupled inductor. The same response time is assumed for initial calculations with a conservative margin.

To calculate the dV for the 3.3-V winding,

$$\begin{aligned} dV &= V_{OUT} (\%V_{OUT} - \%V_{SETPOINT}) \\ &= 3.3V(0.05 - 0.02) = 3.3V(0.3) = 100mV \end{aligned}$$

To calculate the capacitor value for the 3.3-V winding,

$$C = \frac{1A \times 200\mu s}{0.1V} = 2000\mu F$$

To calculate the dV for the 12-V winding,

$$\begin{aligned} dV &= V_{OUT} (\%V_{OUT} - \%V_{SETPOINT}) \\ &= 12V(0.10 - 0.02) = 12V(0.8) = 960mV \end{aligned}$$

To calculate the capacitor value for the 12-V winding,

$$C = \frac{2A \times 200\mu s}{0.96V} = 416\mu F$$

The correct choice is the closest standard value capacitor, which is 560 μF .

RMS Ripple Current

The root-mean-squared (RMS) current in each output (I_{RMS}) is approximated as a purely triangular waveform:

$$I_{RMS} = \frac{I_{PEAK}}{\sqrt{3}}$$

The derived I_{PEAK} value of 2 A is used to calculate the I_{RMS} for the 5-V winding, use:

$$I_{RMS} = \frac{2A}{1.73} = 1.156A$$

The calculation of the I_{RMS} for the 3.3-V winding, uses the derived I_{PEAK} value of 1 A:

$$I_{RMS} = \frac{1A}{1.73} = 0.58A$$

The calculation of the I_{RMS} for the 12-V winding uses the derived I_{PEAK} value of 1.0 A:

$$I_{RMS} = \frac{1.0A}{1.73} = 578mA$$

Final Selection

For the 5-V requirement, finding a 4000- μF , 12.5-m Ω , 1.156 A_{RMS} capacitor was difficult and proved too expensive.

The EEU-FC0J392, 3900 μF , 6.3 V, .030 Ω , 1.95 A_{RMS} , is available for \$0.41 (for quantities of 1,000 or more) from Digikey.

The EEU-FC0J222, 2200 μF , 6.3 V, .045 Ω , 1.44 A_{RMS} , is available for \$0.28 (for quantities of 1,000 or more) from Digikey

The compromise uses two 2200- μF capacitors in parallel. The choice was determined primarily by the ESR value limitations, and even though the combined maximum ESR is 22.5 Ω , the actual ESR is considerably less.

Table IX gives calculated values and recommended components for the three windings.

Customarily, a ceramic capacitor with a value between 0.1 μF and 1 μF is placed in parallel with the bulk capacitors to reduce high-frequency noise.

G. Output Rectifier Snubbers

Because of the inherent parasitic inductance of the board layout, and the reverse recovery time of the output rectifiers, ringing exists at the input to the inductor on each output. To compensate for this, calculate the parasitic elements and then use the formula for a critically damped L-R-C waveform to control the ringing.[4]

First measure the frequency of the ring at the inductor input. Then place a capacitor across the free wheeling diode such that the frequency of the ring is reduced by a factor of approximately two. Since it is now known that the added capacitor is equal to the parasitic capacitance, calculate the parasitic inductance by using the following equation to solve for L.

$$f = \frac{1}{2\pi\sqrt{LC}}, \text{ where } f = \text{ring frequency}$$

Now that L and C are known, calculate the R to use in series with the C to dampen the ring.

$$Q = \frac{1}{R\sqrt{LC}}$$

For a critically damped circuit set Q equal to 1 so that:

$$R = \frac{1}{Q\sqrt{LC}} = \frac{1}{\sqrt{LC}}$$

Losses in the snubber can be minimized by reducing the capacitance needed to dampen the ringing by experimentation. The following equation calculates the snubber resistor losses:

$$P = CV^2 f_{sw}$$

where V is the peak-to-peak (p-p) voltage across the diode

This design requires snubbing the highest power 5-V output. A 33-MHz ring occurred at the inductor input. Adding a 2200-pF capacitor in parallel with the free-wheeling diode reduced that to 15 MHz. The inductance of the resonant tank was calculated to be 51 nH, and a 5- Ω , 1-W resistor was used for critical dampening. This configuration provided excellent snubbing of the 5-V winding. It is also was enough to control the ringing on the other two windings due to the interaction of the coupled inductor.

H. Output Rectifiers

The reverse voltage rating for the 3.3-V and 12-V rectifiers is determined using the maximum peak input voltage and transformer turns ratio. The 5-V diode was selected to be a 35-V rated component.

TABLE 9. OUTPUT CAPACITORS: CALCULATED VALUE AND COMPONENTS

Winding Voltage (V)	Calculated Values				Component				
	Capacitance (μF)	Voltage (V)	Resistance (m Ω)	Current (A_{RMS})	Part Quantity and Name	Capacitance (μF)	Voltage (V)	Current (A_{RMS})	Resistance (m Ω)
5	4000	6.3	12.5	1.156	2 Panasonic EEU-FC0J222	(2) 2200	6.3	1.44	45
3.3	2000	6.3	16.5	0.58	2 Panasonic EEU-FC0J102	(2) 1000	6.3	0.755	90
12	560	25	120	0.578	EEU-FC1E561	(1) 560	25	1.2	65

To calculate the reverse voltage for the 12-V rectifier,

$$V_R = \frac{V_{PK(max)} N_S}{N_P} = \frac{370 \times 7}{51} \cong 51$$

To calculate the reverse voltage for the 3.3-V rectifier,

$$V_R = \frac{V_{PK(max)} N_S}{N_P} = \frac{370 \times 2}{51} \cong 14.5$$

Rectifier current is the peak inductor ripple current (minimum load current) added to the maximum output current.

To calculate the rectifier current for the 3.3-V rectifier,

$$I_{DIODE} = I_{OUT(max)} + I_{RIPPLE(peak)} = 5 A + 1 A = 6 A$$

To calculate the rectifier current for the 5-V rectifier,

$$I_{DIODE} = I_{OUT(max)} + I_{RIPPLE(peak)} = 18 A + 2 A = 20 A$$

To calculate the rectifier current for the 12-V rectifier,

$$I_{DIODE} = I_{OUT(max)} + I_{RIPPLE(peak)} = 3 A + 1 A = 4 A$$

This design requires a diode that has a low forward voltage. Diode losses are largely determined by the forward voltage and current.

$$P_{AVG} = I_{PEAK} + V_F \times Duty Cycle$$

However, rectifiers are sold in packages of two with a common anode, so eliminating the duty-cycle term allows calculation of the dual diode package loss. The general formula for calculating diode losses is

$$P_{DIODE} = V_F \times I_{PEAK}$$

Using the previously calculated criteria, the following output diodes are chosen.

TABLE 10. DIODE RECOMMENDATIONS

	Output (V)		
	3.3	5	12
Voltage Rating (V)	30	35	200
Current Rating (A)	30	30	6
Package	TO-220	TO-247	TO-263
Manufacturer	IR	IR	On-Semi
Part Number	32CTQ030	30CPQ035	MURD620

I. Power Switching FETs

The primary-side switching FETs are chosen as IRF840 devices. While there are many device types that can satisfy the requirements for this design, the IRF840, featuring specifications of 500-V, 8-A capability and an $R_{DS(on)}$ of 0.85Ω , offers good performance at a low cost.

With many IC controllers having an output drive current capability of $\pm 1 A$, interfacing the low-side FET is very straight-forward. Driving the high-side switch in parallel, however, requires a level-shifting circuit which can be implemented in several ways, but the technique selected for this design is to use an off-the-shelf isolated gate drive transformer as shown in Fig. 6. The circuit is described in considerable detail in SEM-1400, Topic 2, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits* [7], and was chosen for this application because it restores the DC levels of the PWM drive to the isolated FET gate while providing a constant drive voltage independent of duty cycle.

The Coiltronix CTX08-14225 transformer, together with a $0.1\text{-}\mu\text{F}$ coupling capacitor on each winding of the gate drive transformer satisfied the minimum requirements set forth by the governing equations in [7].

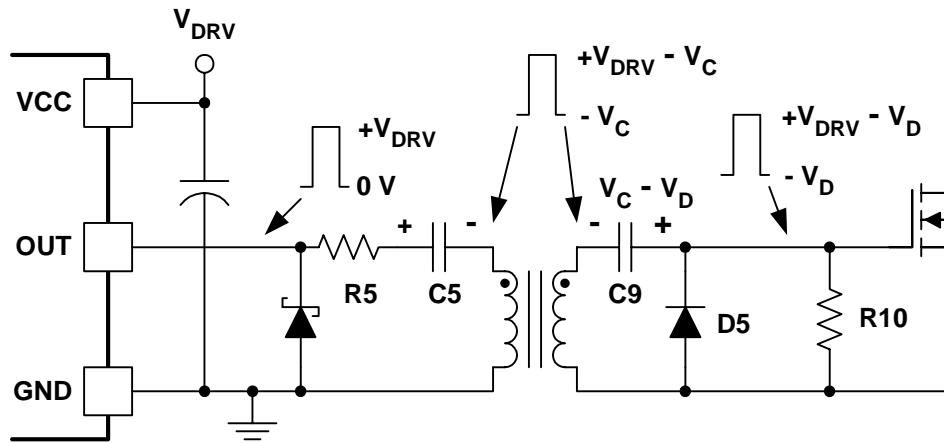


Fig. 6. Isolated gate drive transformer.

J. IC PWM Controller

The UCC3813-1 is chosen for its ease of use, current-mode control capability, and low cost. The UCC3813 is a lower cost version of the UCC3800, with some parameter tolerances widened for better yield in manufacturing. The UCC3813 family is an enhancement of the original Unitrode design, UC3842.

The application note SLUA084 [5], further details the UCC3800/UCC3813 advantages which include

- a wider range of UVLO for the UCC3813 (from 4 V to 12 V)
- internal soft start for controlled turn-on
- leading-edge blanking
- better accuracy for both V_{REF} and frequency
- faster current limit
- lower operating current
- maximum duty-cycle of 50%

PWM Bias Supply and V_{CC} Capacitance

There are two areas of concern when powering the UCC3813-1 PWM. The first is at start-up, when the PWM is attempting to bring all the outputs up to regulation. The second is under steady-state operation. During these periods, the V_{CC} must stay above the UVLO undervoltage lockout turnoff point.

- UVLO start threshold is 8.6 V to 10.2 V, $V_{CC} > UVLO$, and start PWM current is 1.2-mA maximum.
- UVLO stop threshold is 6.8 V to 8.4 V, $V_{CC} < UVLO$, and stop PWM current is 230- μ A maximum
- Start-to-stop hysteresis is 1.6 V to 2.4 V.

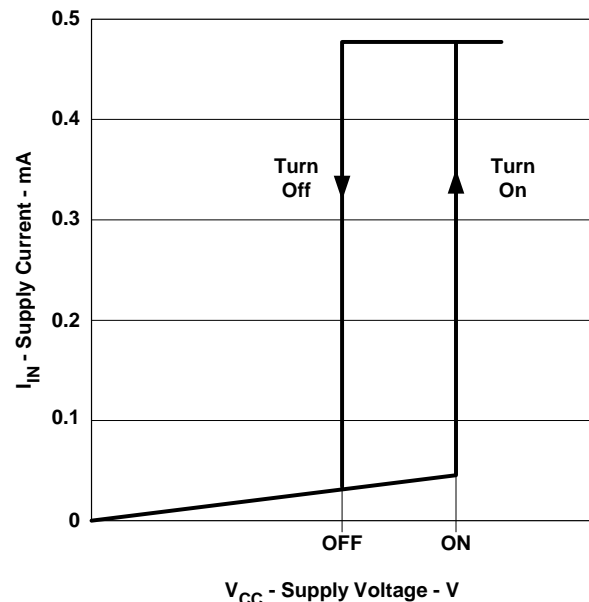


Fig. 7. Input voltage (V_{CC}) hysteresis window

Start-up is a function of the storage capacitance on V_{CC} . Value selection is by the following process:

- Determination of the lowest input voltage at which the supply is expected to turn on. (232 V_{DC})
- Use of the maximum of 230-μA startup current to determine the maximum value of R. (the bleeder resistor across the lower bulk capacitor supplies the *start-up current* listed in the data sheet) This resistor current charges the V_{CC} storage capacitor until the UVLO start threshold is reached.

$$I = \frac{\left[\left(\frac{V_{DC}}{2} \right) - V_{CLAMP} \right]}{39 k\Omega} = 2.6 mA$$

which is more than enough needed for startup.

- The capacitor must power the UCC3813 between the UVLO start and UVLO stop window, or until the bias winding takes over. The assumption is that this time is 10-ms (more than the 4-ms soft-start period of the device).
- Once the device reaches the UVLO start, current in the controller increases to *operating supply current* of 1.2-mA maximum. However, this is only the device current and does not include the current required to drive the power switching FETs which must also come from V_{CC}. Since the gate current is $I = Qgf/2$ and there are two FETs, then $I = Qgf$. The IRF840 FETs are characterized by the published data of 63-nC gate charge.

$$I = QgF = 63 nC \times 100 kHz = 6.3 mA$$

$$I_{TOTAL} = I_{MAX} + I_{FETdrive} = 1.2 mA + 6.3 mA = 7.5 mA$$

- For $I = 7.5 mA$, $dt = 10 ms$, dV as the minimum UVLO turn-on, and UVLO turn-off hysteresis = 1.6 V, the following equation solves for the capacitor value.

$$C = \Delta I \times \frac{dt}{dV} = 0.075 \times \frac{0.01}{1.6} = 46.8 \mu F \cong 47 \mu F$$

Adding a ceramic capacitor with a value between 0.1 μF to 1 μF, in parallel is standard practice to provide high frequency decoupling for the V_{CC} and to provide a reservoir for the peak currents required to turn on the power FETs.

During the second time period the bias winding must provide the PWM power. The bias winding is selected to provide a voltage that stays above the UVLO stop threshold. A 12-V bias winding voltage stays above the UVLO stop threshold and uses the same turns ratio as the 12-V main output. A lower voltage could have been used.

The bias winding is forward derived, like the isolated outputs, so an inductor, two diodes and capacitor are required. The inductor chosen is a low-cost averaging element. The calculated inductance would be very large if continuous conduction was required, approximately 18 mH, however, a smaller 100-μH inductor can be used to average the applied winding pulse and accept some loss in regulation. The 47-μF V_{CC} capacitor provides the holdup during the time the inductor is discontinuous.

Finally, a 12-V zener clamp at the V_{CC} of the PWM prevents the UCC3813 internal 13-V V_{CC} zener clamp from failing because of overcurrent conditions caused by output overloads and short circuits. A 200-Ω resistor limits the current into the 12-V clamping zener. Fig. 8 shows the resultant circuit.

Primary Current Sense Resistor

The primary current is the sum the of 1) the output current with the peak inductor ripple added in normalized to the 5-V winding and reflected to the primary by the turns ratio N_S/N_P and 2) the transformer magnetizing current I_{MAG} , which is derived from the primary magnetizing inductance. Magnetizing inductance is established by placing a small gap in the core so that this value is fixed rather than variable over volume production. A notable consequence of the 2-mH magnetizing inductance is that it adds a slope to the PWM current-sense ramp similar to slope compensation. This slope is beneficial to loop stability, even with duty cycles less than 50%.

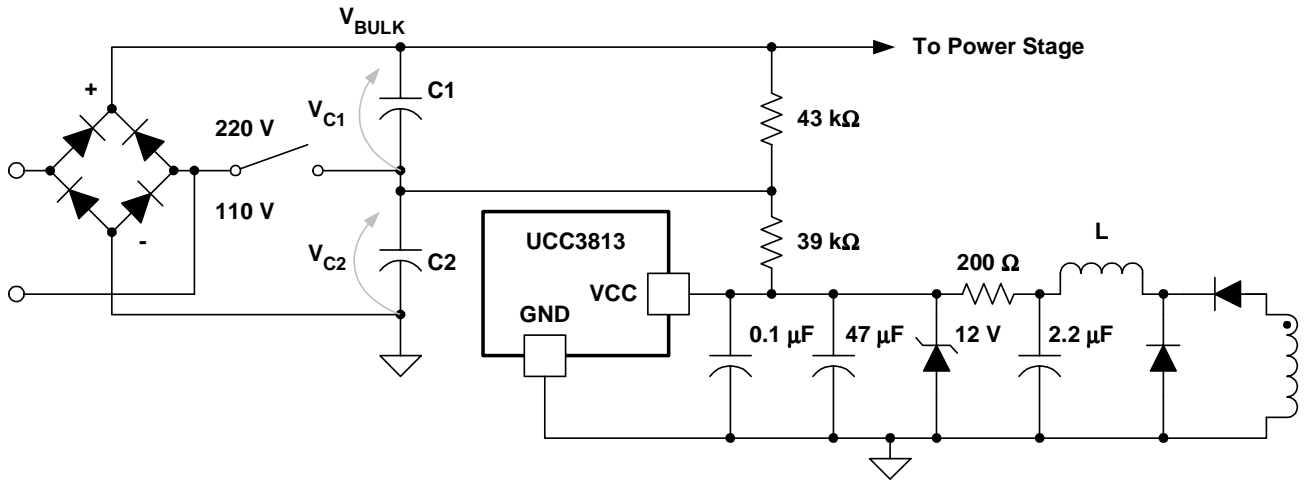


Fig. 8. PWM start-up and bias current.

$$I_P = I_{MAG} + I_S' \left(\frac{N_S}{N_P} \right) \text{ where,}$$

$$I_S' = I_{PEAK} \left(\frac{N_S}{N_P} \right) \text{ for each output}$$

$$= 20 \left(\frac{3}{51} \right) + 6 \left(\frac{2}{51} \right) + 4 \left(\frac{7}{51} \right) = 1.96 \text{ A}$$

$$I_{MAG} = \left(\frac{V_{IN(max)}}{L} \right) (t_{ON(min)}) = \left(\frac{370}{2.3mH} \right) (2.5\mu s)$$

$$= 0.40 \text{ A}$$

$$I_P = I_{MAG} + I_S' = 1.96 \text{ A} + 0.40 \text{ A} = 2.36 \text{ A}$$

The UCC3813 has a 0.9-V pulse-by-pulse current limit minimum, and the following equation solves for the primary current sense resistor:

$$R_s = \frac{V_s}{I_s} = \frac{0.9V}{2.36A} = 0.381\Omega$$

therefore, the appropriate resistor is the one with the closest available standard resistor value, 0.4 Ω .

Note that the current sense resistor also sees the FET gate current and the output rectifier recovery current at the beginning of each power pulse. This leading-edge current spike is blanked within the UCC3813.

K. Setting Up the Loop

Fig. 9 shows an isolated power supply loop being closed in the secondary with the TL431A. As the error signal is generated by the TL431A, there is no need to use the PWM error amplifier. A common practice is to make the PWM error amplifier *current source only*, commanding maximum pulse widths, and use the optocoupler circuit to reduce the duty-cycle by pulling down on the error amplifier output COMP pin. This configuration is accomplished by connecting the PWM feedback input to ground. This connection forces the output of the error amplifier COMP to be high, commanding full duty-cycle.

The COMP source current of the PWM error amplifier is specified in the data sheet as 800 μA maximum. Therefore, the optocoupler circuit must be able to sink that much current and also place COMP to a low-enough voltage to ensure zero duty-cycle. This COMP low voltage is determined by the COMP to CS offset of 0.45 V minimum listed in the UCC3813 data sheet. In other words, when COMP is at 0.45 V, then the duty cycle is zero.

The optocoupler must sink the COMP source current of 800 μA and pull COMP down to .45 V to achieve zero duty-cycle. The optocoupler has a $V_{\text{CE(sat)}}$ of 0.3 V, so it could be directly connected to the COMP pin; however, a small resistor is added in series to lessen noise effects. The resistance needed is calculated as $R=V/I=0.15\text{ V}/800\ \mu\text{A}=187\ \Omega$ maximum, so the choice is to use 150 Ω .

Another way to help reduce noise is to increase the optocoupler output current by adding a pull-up resistor between VREF and the optocoupler collector (R6 in Fig 8). However, this technique causes $V_{\text{CE(sat)}}$ of the optocoupler to increase and is not needed in this design.

It is necessary to sink 800 μA in the optocoupler, and this sink current is determined by the optocoupler diode drive and the current transfer ratio (CTR). This device has a typical 100% CTR, but reduces to 40% at the temperature extremes. Using the 40% value, at least $800\ \mu\text{A}/0.4=2\text{ mA}$ is needed to sink through the optocoupler diode. The TL431A can sink a maximum current of 30 mA, so there is enough

current to drive the optocoupler and force the PWM to zero duty cycle.

Component D12 in Figure 9 is a 10-V zener diode, the voltage source for the optocoupler drive circuit. Its current is provided from the 12-V output through a current-limiting resistor R18. R16 is calculated by subtracting the $V_{\text{F}}=1.5\text{ V}$ of the optocoupler diode, and the TL431A anode voltage of 2.5 V, from the 10-V source. Using a 30-mA maximum and solving for R16,

$$R16 = \frac{(10\text{V} - 1.5\text{V} - 2.5\text{V})}{0.03\text{A}} = 200\ \Omega$$

The TL431A has a specification for minimum cathode current for regulation of 1 mA. This is used to determine R17 in parallel with the optocoupler diode. To maintain some margin, a 2-mA value is used.

$$R17 = \frac{1.5\text{V}}{2\text{mA}} = 750\ \Omega$$

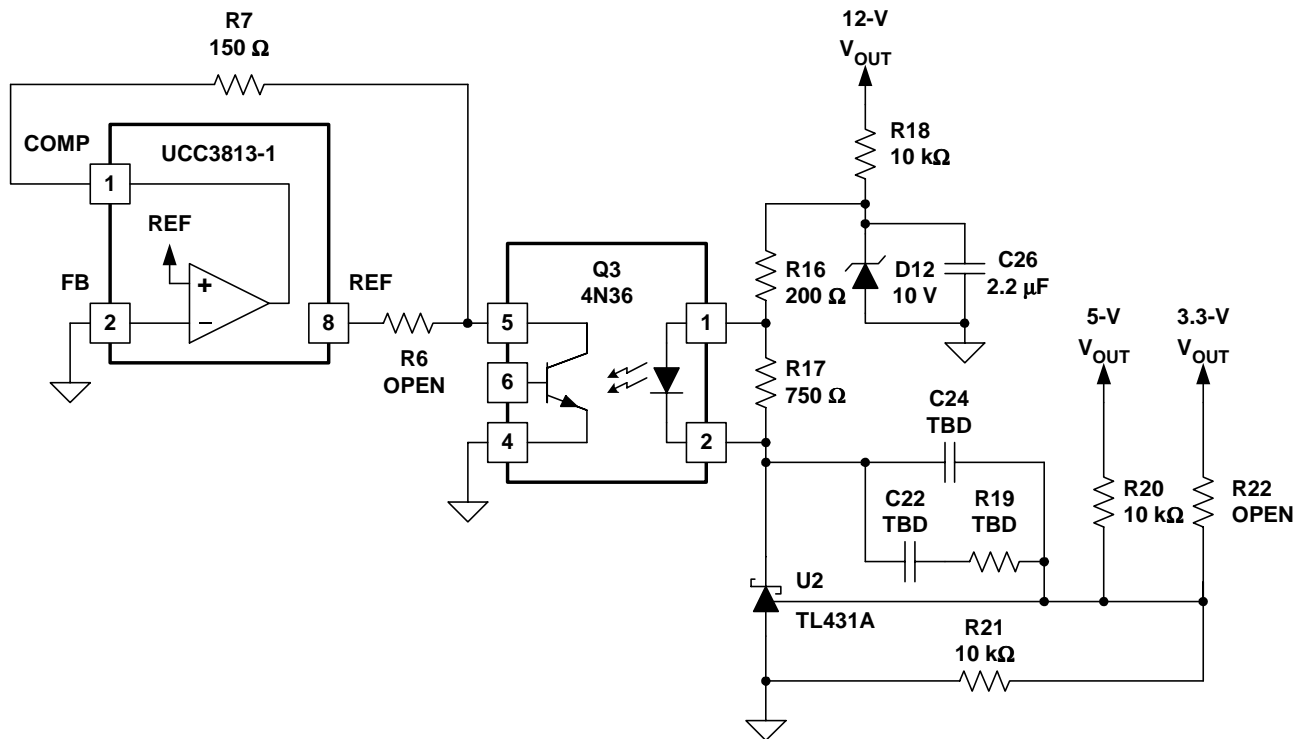


Fig. 9. Isolated power supply loop closed.

Closing the Loop

There are many interactions that a coupled inductor can add when closing the feedback loop which are beyond the scope of this paper. For testing purposes the loop is closed with a low bandwidth by using a 1 μ F capacitor for C24. Further optimization is required to determine the values needed for the 5-kHz bandwidth required. For a thorough description of closing an isolated feedback loop using the TL431, see SEM-1500, Topic 3.[6]

L. A Few Optional Ideas

There are some additional ideas that are worth mentioning:

- With the 110 V/220 V selector switch, it is possible to place the switch in the doubler mode and connect to 220 V. This setup would overvoltage the bulk capacitors, probably causing venting and a safety hazard. A common practice is to place metal oxide varistors (MOVs) (or high power zeners), in parallel with each input capacitor, so that in the event of overvoltage, the MOV impedance collapses, causing high-input currents and blowing the input fuse.
 - The addition of a schottky diode from the PWM output to V_{CC} clamps the output to V_{CC} and the external zener clamp. In the event of a MOSFET gate to drain short, the gate is pulled high and clamped to the 1-W V_{CC} zener. If a fuseable gate drive resistor is used, it then opens up during this event and prevent the PWM from venting smoke and making loud noises.
 - The loop in this design is closed on the 5-V output with a 2.0% tolerance (1% TL431A and 1% resistors). To tighten the 3.3-V regulation, with some accuracy loss to the 5 V it is possible to sum both the 3.3 V and 5 V into the TL431A feedback using R22.
 - If this power supply requires powergood or reset signal, there are several methods for meeting this requirement:
 - UC3904, AC line input fail, monitors positive and negative voltages, over and undervoltage, over current functions, power good delay.
 - TPS3514, senses three positive voltages, OV, UV, remote turn-on and turn-off control, and overcurrent.
 - Several methods are in the *supervisory circuits* home page on the TI website.
- Primary R-C snubber components are included in this design. Experience shows that the high dV/dt of the high-voltage primary waveform can be a key source of broadband emissions in the 10 MHz to 100 MHz range. In this design, the dV/dt at high line maximum load is 6.6 V/ns. An R-C filter using a 100-pF capacitor and a 1-k Ω resistor reduced that to 5 V/ns. Even slight reductions such as this can have dramatic improvements on EMI. Placeholders for snubbers and slew rate control should be included on the chance they may be needed.

IV. TEST RESULTS

Fig. 10 represents the final schematic of this forward converter design example.

A. Efficiency

A target efficiency of 80% is obtained when measured with a precision input harmonic/power analyzer that measures true input power. The data coincide very well with expected results. (As a caution, it should be noted that initial measurements, made using a DVM digital voltage meter for input current and voltage, yielded only 60% and very high RMS input currents, caused by the DVM's inability to accurately measure true RMS input current because of the high harmonic content associated with a peak detecting bridge rectifier.)

Fig. 10 shows that at full load, the efficiency was poorest at low input and increased at higher input voltages. This pattern indicates resistive losses in the design, since as the input voltage increases, the power train currents decrease. At full load output (144 W), the efficiency ranged from 79% at 90 V_{AC} input to 81% at 264 V_{AC} input.

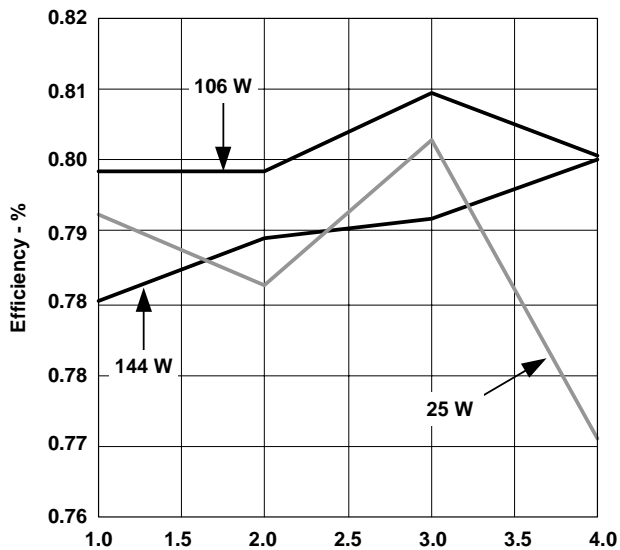


Fig. 11. Efficiency.

Note that at the light load of 25 W, efficiency drops off at the high-input voltage. This dropoff demonstrates capacitive switching losses in the circuit based on $P=CV^2f$.

B. Cross Regulation

The outputs were evaluated for cross regulation by means of the following tests:

- putting the full load on the 5-V output with minimum loads on the other two
- putting minimum load on 5-V output and full load on the others. Since the voltage loop is closed on 5-V output, it remained solid as expected. Fig. 12 shows the results.

The following variations occurred:

- 12 V varied by +8% and -5%.
- 3.3 V varied by $\pm 6\%$.
- 5V was within 1%.

Both unregulated outputs, at maximum load, were low when the 5-V output was lightly loaded. This result is expected because of resistive losses in the 12-V output and 3.3-V output paths that were not compensated for directly by the voltage loop. Both unregulated outputs were high when they were lightly loaded and 5-V output was at its maximum. Again, the resistive losses in the 5-V output were compensated for by the loop, forcing the other two outputs higher. This is, however, much better regulation than would have been typically obtained using separate inductors.

The 3.3-V output was beyond the $\pm 5\%$ specification, so summing both 3.3-V and 5-V outputs to close the loop brings the 3.3-V within the requirements while allowing the 5-V to have an increased tolerance. This summing can be an iterative exercise since the inductor coupling of the outputs and the resistive losses all contribute to the voltage variance. Treating the TL431A 2.5-V reference as a summing junction allows the adjustment of the contribution that each output has to the 2.5-V set-point and can modify each outputs regulation for a good compromise.

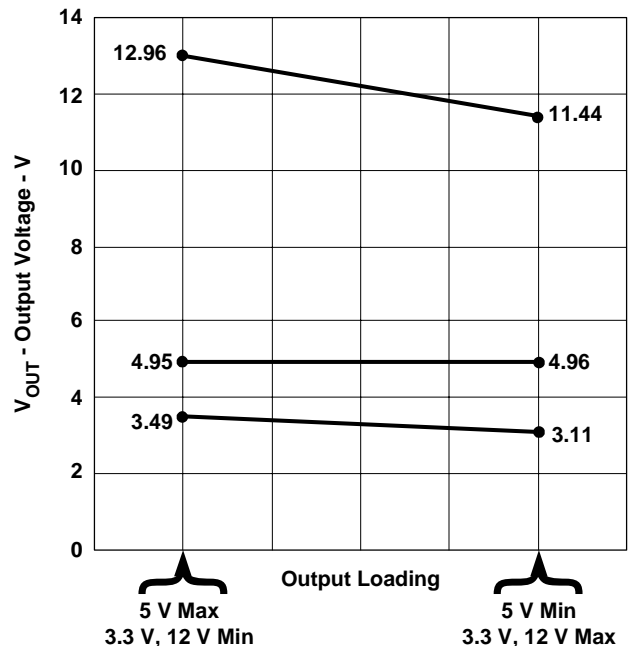


Fig. 12. Cross regulation extremes.

C. Input Capacitor Ripple

Fig. 13 shows the input capacitor ripple at maximum load and low line 90-V_{AC} input.

Two 560- μ F capacitors are used for the closest available standard to the 474- μ F calculated values.

The peak voltage on the capacitors is 231 V, with 14.2 V of ripple, resulting in a $V_{IN(min)}$ of 216.8 V, higher than the 206-V calculated but explained by the fact that the input capacitors were oversized for the low input range.

The calculations indicated that the peak voltage would be 254 V, but the measured value is less by about 20 V. Understanding the difference between calculated and measured

peak voltage is important because it affects the ability to regulate the output at maximum duty and minimum input voltage. The difference can be attributed to resistive losses in the input, the inrush thermistor, and the bridge rectifier. The peak currents are normally high when using a rectifier/capacitor input from an AC line.

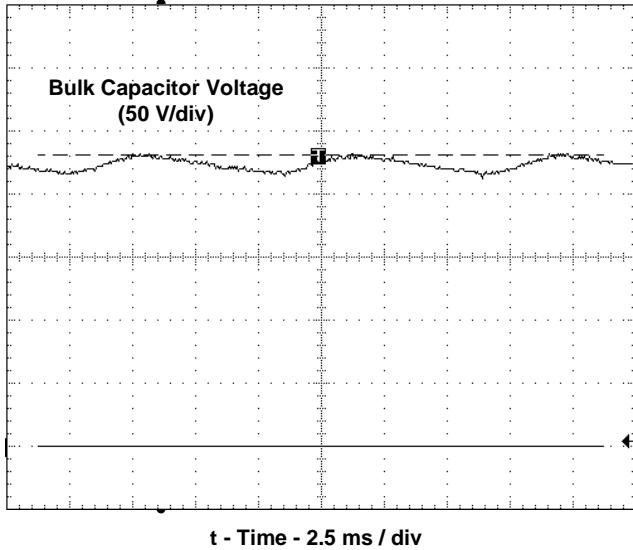


Fig. 13. Bulk capacitor input ripple at 90- V_{AC} , maximum load.

Overall, the input ripple met expectations and allowed duty cycle control over all input voltages.

D. Primary Waveforms

Fig. 14 shows the primary Q1 drain-to-source voltage at maximum load and 90 V_{AC} input, and associated drain current. The current is 2 A per division and reaches approximately 1.9 A. This value agrees with the prediction of 2.36 A primary current.

The switching frequency is 9 μs or 111 kHz. The UCC3813 data sheet graphs were used to determine the R-C values for 100 kHz and were slightly rounded up.

The duty cycle is 4- μs ON and 5- μs OFF for a 44% value. The maximum duty-cycle is required at the lowest input voltage; and with a measured value of 44% it shows some margin available.

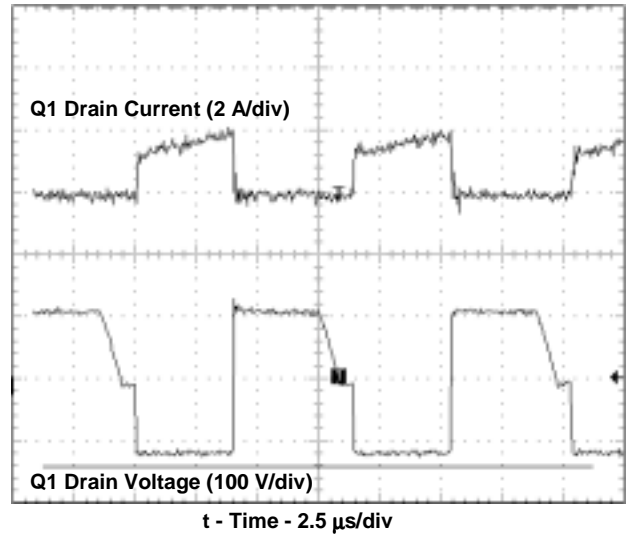


Fig. 14. Q1 drain-to-source voltage and drain current at maximum load and 90- V_{AC} input.

Fig. 15. shows the same waveforms with a 264- V_{AC} input maximum.

The duty-cycle time is 2.5- μs ON and 6.5- μs OFF for a 27% value, exactly agreeing with the calculated number. The maximum FET voltage, 350 V measured, indicates some margin on the 500-V FET rating.

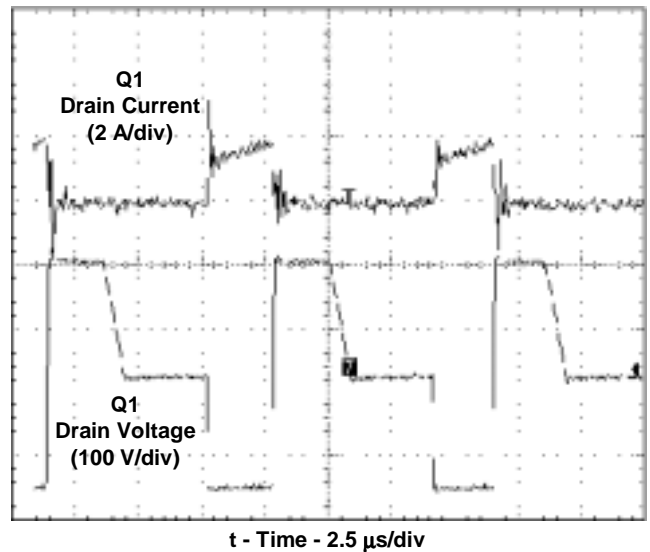


Fig. 15. Q1 drain-to-source voltage at maximum load and 264 V_{AC} input.

E. Output Ripple Voltage

The figures below show the ripple voltage in the outputs. From this information, and a knowledge of the capacitors' ESR values, you can extrapolate the inductor ripple current. The specifications for ripple voltage were 1% on the 5-V and 3.3-V outputs, and 2% for the 12-V output. The ripple and noise voltages measured on the three outputs of this power supply are given in Table X, and the waveforms are shown in Figures 16, 17, and 18.

TABLE 11. OUTPUT RIPPLE VOLTAGE

Winding (V)	Specified $V_{RPL(p-p)}$ (mV)	Measured $V_{RPL(p-p)}$ (mV)	Peak Noise Spikes (mV)
12	240	130	172
5	50	15	58
3.3	33	100	181

As shown in Table X, better filtering is needed on the 3.3-V output, The major cause of this is the coupled inductor steering mechanism which is affected by the small mismatch in the voltage drops of the 5-V and 3.3-V rectifiers whose effect is difficult to quantify. This is shown in the shape of the waveforms where the triangle wave on the 12-V output demonstrates the success in steering most of the ripple current to that output while the non-perfect ratios to the 5-V and 3.3-V outputs show distorted wave shapes. Without a coupled inductor, each output would have a triangular ripple voltage.

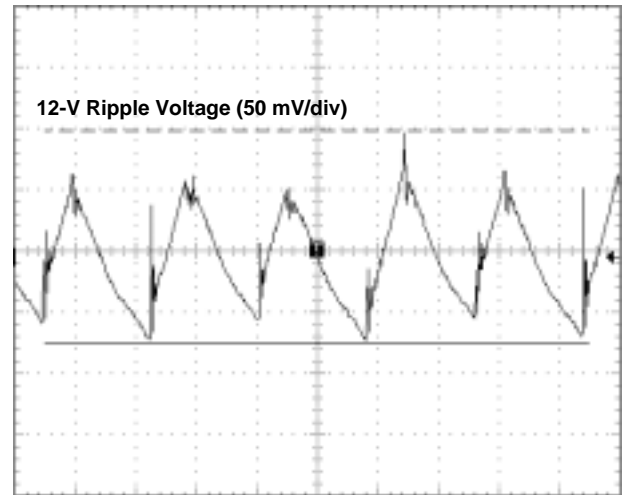


Fig. 16. 12-V Ripple voltage.

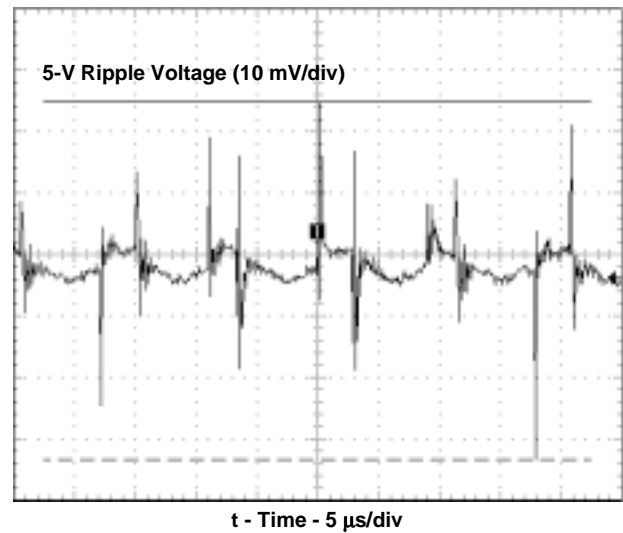


Fig. 17. 5-V Ripple Voltage.

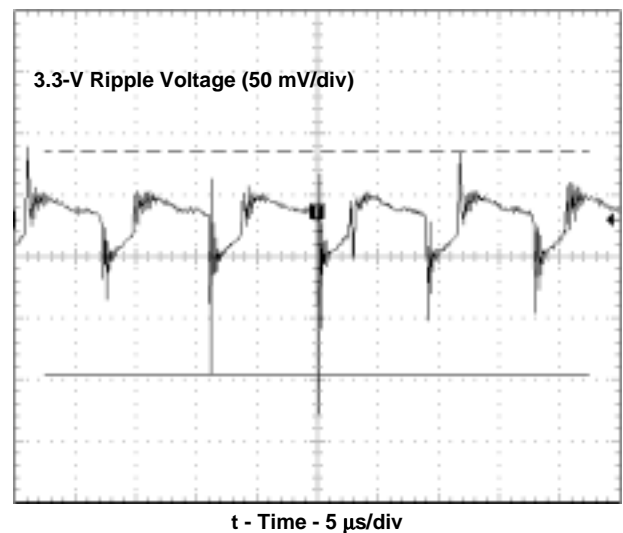


Fig. 18. 3.3-V Ripple voltage.

F. Diode Voltage

A major design factor is the voltage rating of the large 5-V schottky diode. Fig. 19 shows the measured voltage waveform on this diode at the 264 VAC high line input. The diode is conducting during the upper plateau, and the peak inverse voltage is shown at the lower plateau with a measured value of approximately -22 V. The chosen diode, IR30CPQ035 has a 35 V rating, well within the required limits. The ring on the negative portion shows that there may be a need to snub the top diode as well as the free-wheeling diode.

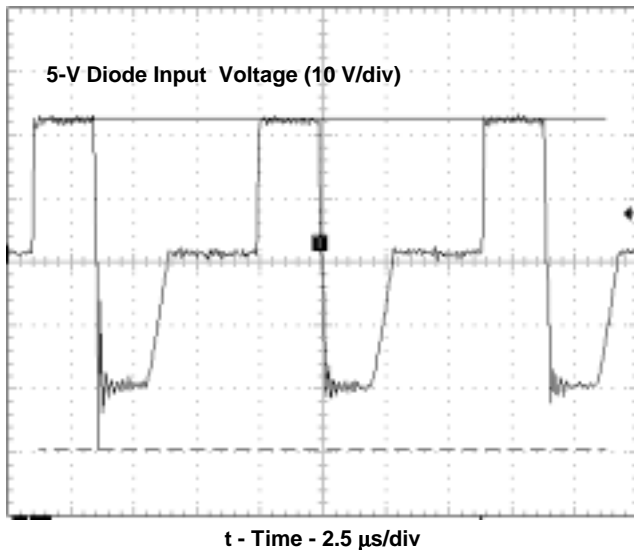


Fig. 19. Diode blocking voltage.

The free-wheeling half of the diode pair blocks the positive voltage, which is about 21 V, also well within the rating, and there is no ringing.

V. CONCLUSION

This paper discussed topics related to the design of an off-line, isolated power supply. A step-by-step process for designing the power supply was presented and followed. As with any design, there are some iterations, trial and error, and experimentation before the design is final and goes to production.

The measured results are extremely close to calculated on a first prototype. That clearly demonstrates the effectiveness of this design procedure.

The hardware demonstration would not have been possible without the help of two

individuals. Mike Pantanella of TI-Manchester who created the schematic files, material lists and board layout in PCAD; and Norman Campbell at Coiltronics who crafted the transformer and coupled inductor based on my initial inputs.

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Note: References to past Power Supply Design Seminar topics can best be found on the internet at <http://power.ti.com/seminars>

APPENDIX I

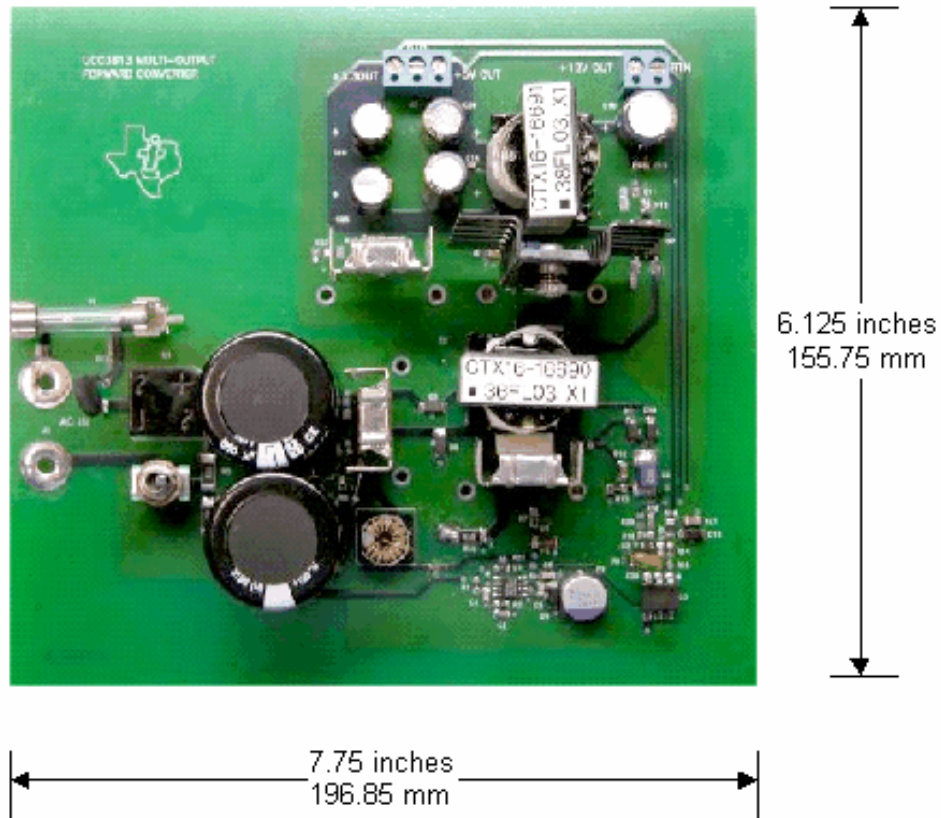


Fig. 20. Design PCB

TABLE 12. LIST OF MATERIALS

Reference Designator	Qty	Description	Size	Mfr	Part Number
C1	1	Capacitor, ceramic, 100 pF, 50 V, COG	805	Std	standard
C10	1	Capacitor, ceramic, 100 pF, 500 V, COG, ±10%	1206	Vishay	VJ1206A101KXEMT
C12	1	Capacitor, ceramic, 2200 pF, 50 V	1206	muRata	GRM42-6yyyxxxKvv
C14, C26	2	Capacitor, ceramic, 2.2 μF, 25 V, X7R	1206	TDK	C3216X7R1E225K
C19	1	Capacitor, aluminum, 560 μF, 25 V, 20%	12.5 × 20mm	Panasonic	EEU-FC1E561s
C2	1	Capacitor, ceramic, 330 pF, 50 V, NPO	805	Std	Std
C20, C25	2	Capacitor, aluminum, 2200 μF, 6.3 V, 20%	0.2	Panasonic	EEU-FC0J222
C21, C23	2	Capacitor, aluminum, 1000 μF, 6.3 V, 20%	0.2	Panasonic	EEU-FC0J102
C22	1	Capacitor, ceramic, TBD- μF, TBD-V	805	muRata	GRM40yyyxxxKvv
C24	1	Capacitor, ceramic, 1 μF, 25 V, X7R	805	Std	Std
C3, C4	2	Capacitor, aluminum electrolytic, 560 μF, 250 V	0.990 dia × 1.400"	Panasonic	EETED2E561DA
C5, C6, C7, C9, C16, C17, C18	7	Capacitor, ceramic, 0.1 μF, 50 V, X7R	805	Yageo America	08052R104K9BB0D
C8	1	Capacitor, OS-CON, 47 μF, 20 V, 45 mΩ, 20%	8.3 mm (E7)	Sanyo	20SVP47M

Reference Designator	QTY	Description	Size	Mfr	Part Number
D1	1	Diode, 6 A, 600 V, bridge rectifier	GBJ series		PB66
D10	1	Diode, dual schottky, 30 A, 35 V	TO-247AC	Int'l Rectifier	30CPQ035
D12	1	Diode, zener, 10 V, 1 W	SMA	Diodes Inc.	SMAZ10-13
D2	1	Diode, schottky, 1 A, 40 V	MELF	Diodes Inc.	1N5819M
D3, D6	2	Diode, fast, 1 A, 600 V	SMA		RS1J-13
D4, D5	2	Diode, zener, 12 V, 1 W	SMA	Diodes Inc.	SMAZ12-13
D7	1	Diode, dual ultrafast, 200 V, 6 A	D-PAK	Int'l Rectifier	MURD620CT
D8	1	Diode, dual schottky, 30 V, 30 A	TO-220AB	Int'l Rectifier	47CTQ020
D9, D11	2	Diode, schottky, 1.0 A, 100 V	SMA		BYS1100-13
F1	1	Fuse clip	0.205 × 0.220 ×2	Wickmann	520
J1	1	Connector, binding post, insulated, for standard banana plug, red, 15 A	0.425 dia	Johnson	111-0702-001
J2	1	Connector, binding post, insulated, for standard banana plug, black, 15 A	0.425 dia	Johnson	111-0703-001
J3	1	Terminal block, 2 pin, 15 A, 5.1 mm	0.40 × 0.35	OST	ED1609
J4	1	Terminal block, 3 pin, 15 A, 5.1 mm	0.60 v 0.35	OST	ED1610
L1	1	Inductor, SMT, 100 µH, 0.53 A, 1.1 Ω	0.35 × 0.24	Coiltronics	UP1B-101
L2	1	Transformer, 1 primary, 2 secondary, xx mH, yyA	0.945 × 1,260	Cooper	CTX16-16691
Q1, Q2	2	MOSFET, N-channel, 500 V, 8 A	TO-220AB	Int'l Rectifier	IRF840
Q3	1	Optocoupler, 5300 V, 100% CTR	DIP6	Fairchild	4N36
R1	1	Resistor, chip, 1 kΩ, 1/10 W, 1%	805	Std	Std
R2	1	Resistor, chip, 39.2 kΩ, 1/10 W, 1%	805	Std	Std
R3	1	Resistor, chip, 43 kΩ, 1 W, 1%	2512	Std	Std
R4	1	Resistor, chip, 39 kΩ, 1 W, 1%	2512	Std	Std
R5	1	Resistor, chip, 4.7 Ω, 1/10 W, 1%	805	Std	Std
R6, R19, R22	3	Resistor, chip, TBD- Ω, 1/10 W, TBD%	805	Std	Std
R7	1	Resistor, chip, 150 Ω, 1/10 W, 1%	805	Std	Std
R8	1	Resistor, chip, 1 kΩ, 2 W, 5%	2512	Std	Std
R9	1	Resistor, chip, 4.7 Ω, 1/8 W, 5%	1206	Std	Std
R10	1	Resistor, chip, 1 kΩ, 1/10 W, 1%	805	Std	Std
R11	1	Resistor, chip, 0.39 Ω, 1 W, 1%	2512	Std	Std
R12	1	Resistor, chip, xxx- Ω, ½ W, y%	2010	Std	Std
R15	1	Resistor, chip, 200 Ω, 1/8 W, 1%	1206	Std	Std
R16	1	Resistor, chip, 200 Ω, 1/10 W, 1%	805	Std	Std
R17	1	Resistor, chip, 750 Ω, 1/10 W, 1%	805	Std	Std
R18	1	Resistor, chip, 100 Ω, 1/8 W, 1%	1206	Std	Std
R19	3	Resistor, chip, TBD- Ω, 1/10 W, TBD%	805	Std	Std
R20	1	Resistor, chip, 10 kΩ, 1/10 W, 1%	805	Std	Std
R21	1	Resistor, chip, 10 kΩ, 1/10 W, 1%	805	Std	Std
RT1	1	Thermistor, 10.0 to 0.258 Ω, 3 A	0.41 × 0.12	Ametherm	SL10-10003
S1	1	Switch, SPDT, vertical PC-mount	0.500 × 0.270	C & K	7101SYCxE
SH1	1	Short jumper			
T1	1	XFMR, gate drive 1 primary, 1 secondary	0.512 × 0.480	Coiltronics	CTX08-14225
T2	1	Transformer, 2 primary, 2 secondary, xx mH, yyA	0.945 × 1,260	Cooper	CTX16-16690
U1	1	Low-power BiCMOS current-mode PWM	SO-8	TI	UCC3813-1D
U2	1	Precision adjustable shunt regulator	SOT23-5	TI	TL431ADBVR

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