Compensating DC/DC Converters with Ceramic Output Capacitors

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ABSTRACT

The latest technology uses ceramic capacitors as the main part of filtering in DC/DC converters. This low-ripple solution is small and inexpensive. However, ceramic capacitors in the output filter require an advanced feedback and compensation circuit design than that used for traditional electrolytic capacitor. Transient performance of a DC/DC converter with a low-output capacitance filter depends significantly on the gain and bandwidth of the feedback loop. Ceramic capacitors cause higher resonant frequency of the output filter and a sharp phase lag, affecting stable operation of a DC/DC converter. Worst-case analysis for different conditions takes into account components and parameters tolerances. The suggested compensation-circuit design procedure ensures highest gain and bandwidth of frequency response, with comfortable phase and gain margin for stability.

I. INTRODUCTION

Size, cost, and accuracy remain important for any DC/DC converter design. However, these, often contradictory, criteria require proper output-filter components and optimized loop-compensation circuit design. Recently, the cost and stability have improved for ceramic capacitors with tens of microfarads of capacity. Therefore, these capacitors are now attractive as output filters of DC/DC converters, since their low equivalent series resistance (ESR) and equivalent series inductance (ESL) offer substantial benefits of lower output ripple voltage and reduced size. However, compared to traditional electrolytic types with larger ESR and ESL, ceramic capacitors also give an output filter a higher resonant frequency, lower damping, and a more nearly ideal second-order characteristic, with a sharp and almost full 180° phase lag at resonance.

Best load-current transient response requires optimizing both the output filter and the feedback loop. Traditional filter designs with electrolytic capacitors successfully use larger capacitance values to provide low output ripple. These higher values have also relaxed the need to maximize the control bandwidth for fast transient response. However, ceramic output capacitors with less total capacitance require increased gain and bandwidth of the control loop for equivalent transient response. These requirements, while insuring unconditional stability with an ideal second-order filter, significantly challenge the circuit engineer.

This paper addresses that challenge, discussing worst-case conditions for voltage-mode control loop design, the effect of component tolerances and variations, and the effect of limited bandwidth of the error amplifier. It provides practical recommendations implemented in Mathcad™-based design software.

II. CERAMICS OUTPUT CAPACITORS VS ELECTROLYTIC

A. Main Parameters

The dramatic increase in capacitance-to-size ratio of ceramic capacitors with X5R, X7R dielectric within the last few years makes the switching DC/DC converters with ceramic output capacitors a very popular solution. This popularity is due to low cost, better filtering capability, high-frequency operation, and thermal stability of X5R, X7R ceramic capacitors. Table 1 compares typical characteristics of ceramic capacitors to those of other popular types, including electrolytic, OS-CON, and specialty polymer.

TABLE 1. TYPICAL CHARACTERISTICS OF VARIOUS OUTPUT FILTERING CAPACITORS

Type	Vendor	Part Number	V_{DC} (V)	C (μF)	ESR (mΩ)	ESL (nH)	Size (mm)	Relative Cost
Aluminum Electrolytic	Rubycon	6.3ZA1000	6.3	1000	24	4.8	10 (diam) x 16	1
OS-CON	Sanyo	4SP820M	4	820	8	4.8	10 (diam) x 10.5	6
POSCAP	Sanyo	4TPC150M	4	150	40	3.2	7.3 x 4.3 x 1.9	3
Ceramic	TDK	C3225X5R1A156M	6.3	15	2	0.5	3.2 x 2.5 x 1.35	0.7

Ceramic capacitors with X5R or X7R dielectric have much lower parameter variations and tolerances in comparison to the electrolytic capacitors. The latest ceramic capacitors have capacitance in the 10-μF to 100-μF range, with extremely low ESR, near 2 mΩ to 5 mΩ. Their capacitance has ± 20% tolerance or lower.

B. Output Voltage Ripple

Low ESR and ESL of ceramic capacitors significantly decrease the output voltage ripple of DC/DC converters. The ripple in this case depends primarily on capacitance value. The ripple of other types of capacitors with relatively large ESR is defined mainly by the ESR value. Thus the output voltage ripple reflects the current ripple waveforms of the output inductor. The waveforms in Fig. 1 show the switching waveforms and output voltage ripple of a DC/DC converter using 2 x 150-μF specialty-polymer capacitors. The waveforms in Fig. 2 relate to the regulator with 3 x 22-μF ceramic capacitors. Both regulators have the same 0.65-μH output inductor and run at the same switching frequency of 700 kHz. The input voltage is 3.3 V and the output voltage is 1.8 V for these measurements. The peak-to-peak ripple using totally 66-μF ceramic capacitors is only 6.4 mV, while the totally 300-μF SP capacitors have peak-to-peak ripple of 23.2 mV.

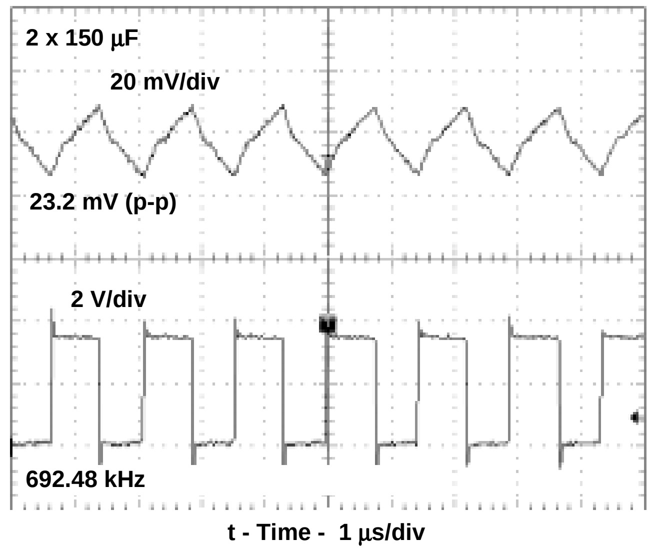

Fig. 1. Output ripple and switching waveforms of converters with specialty-polymer capacitors.

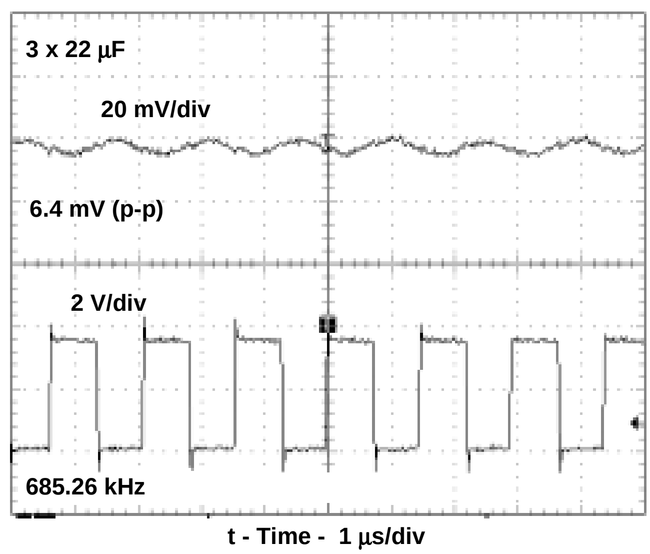

Fig. 2. Output ripple and switching waveforms of converters with ceramic capacitors.

C. Output Filter Frequency Response

Output capacitor parameters and their tolerances significantly affect the frequency response of the regulator. The differences of typical output-filter frequency responses for electrolytic and ceramic capacitors are illustrated in Figs. 3 and 4. When using electrolytic capacitors, selecting a larger inductance value generates approximately equal output ripple at the same switching frequency as the ceramics.

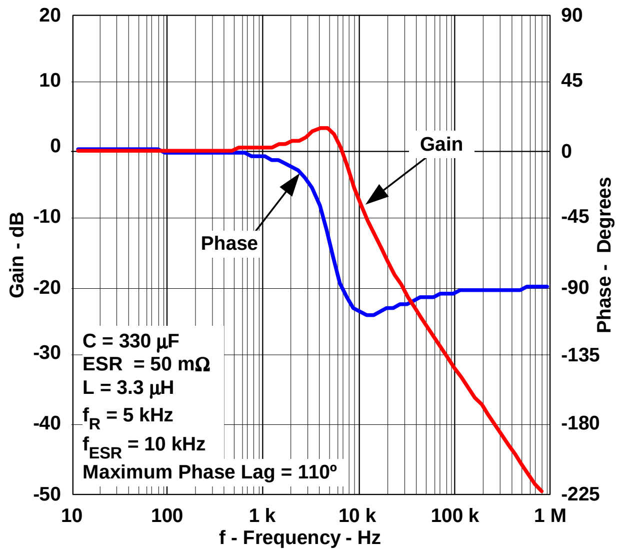

Fig 3. Frequency response of output filter with electrolytic capacitors.

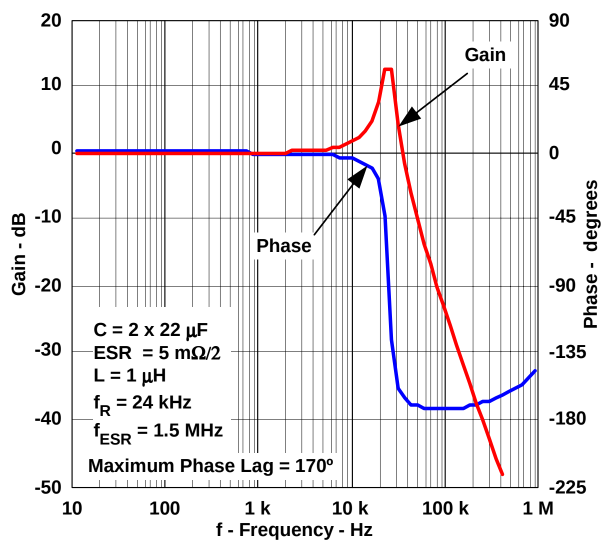

Fig 4. Frequency response of output filter with ceramic capacitors.

Most electrolytic capacitors have relatively large capacitance and ESR values that vary by 2 to 3 times or more, depending on the type and lot of capacitor, temperature and frequency. ESR of the output capacitor and its variation affect the feedback-loop design, because one of the poles of the compensation circuit is usually selected equal to the frequency of the ESR-zero. Variation of output capacitance leads to the variation of corner frequency of the output L-C filter. This fact also influences compensation circuit design. Because of wide tolerances and variations, electrolytic capacitors require at least 60° phase margin at nominal operating condition when the compensation circuit of the feedback loop is selected.

The frequency of the ESR-zero for ceramic capacitors is located in the MHz range. It is far above the typical crossover frequency, which is usually less than 1/5 of the switching frequency. That means that the ESR-zero has negligible effect on compensation-circuit design. For example, the crossover frequency of a 700-kHz switching frequency regulator does not exceed 140 kHz, which is much lower than the frequency of the ESR-zero.

Fig. 4 shows that the output filter of a DC/DC converter using ceramic capacitors has about 5-times higher resonant frequency (F_R), 15-times higher ESR-related zero frequency (F_{ESR}), and a phase lag of 170° versus 110° for the electrolytic output capacitor. For example, an ideal second-order filter provides 180° phase lag, and thus the output filter with ceramic capacitors is close to ideal.

D. Transient and Frequency Response of Converter Using Electrolytic Capacitors

Ceramic and electrolytic capacitors behave differently during the load-current transients of the DC/DC converter.

A typical example of the load current transient response using electrolytic output capacitors is shown in Fig. 5. Two transient peaks, V_{m1} and V_{m2}, must be considered closely. Peak V_{m1} occurs at the beginning-of-load current step. It is defined by ESR and ESL of the output capacitor. This spike is too fast for the feedback loop of the converter. The ESL-related part of V_{m1} can be decreased by adding high-frequency decoupling capacitors. The ESR-related portion requires more capacitors in parallel or more expensive, lower ESR electrolytic capacitors.

The second peak V_{m2} is caused by the removal of charge from the output capacitor during the load current step-up. A similar but positive peak occurs during the load current step-down. In that case it is caused by the excessive charge delivered from the output inductor. The amplitude of second peak V_{m2} depends on optimal output filter selection and on how quickly the feedback loop of the converter responds on transient [1],[2]. However, relatively large capacitance helps maintain the output voltage dynamic deviation within the required window, even with the relatively slow feedback loop. The loop frequency response for this converter is shown in Fig. 6. The crossover frequency is 33 kHz, and the phase margin is 88°. Because of low bandwidth and gain feedback loop, the output voltage returns to the nominal value slowly, after more than 100 µs in this case. However, for this particular output filter, increase of loop bandwidth does not affect peak-to-peak output voltage deviation, because V_{m2} is already less than V_{m1}. It is important to remember that the output ripple of converters with electrolytic capacitors can occupy a significant part of the voltage window allowed for the transient response. Standard evaluation module with electrolytic capacitors TPS54310EVM-201 from TI [8] has been used for the measurements.

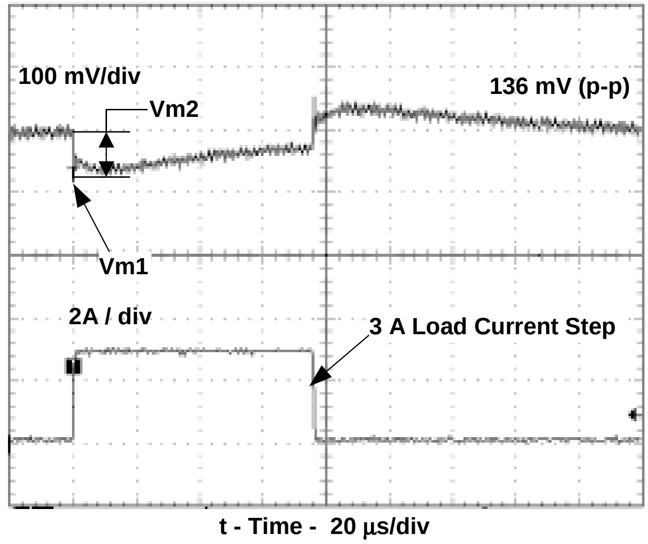

Fig. 5. Load current transient response of converter using electrolytic capacitors.

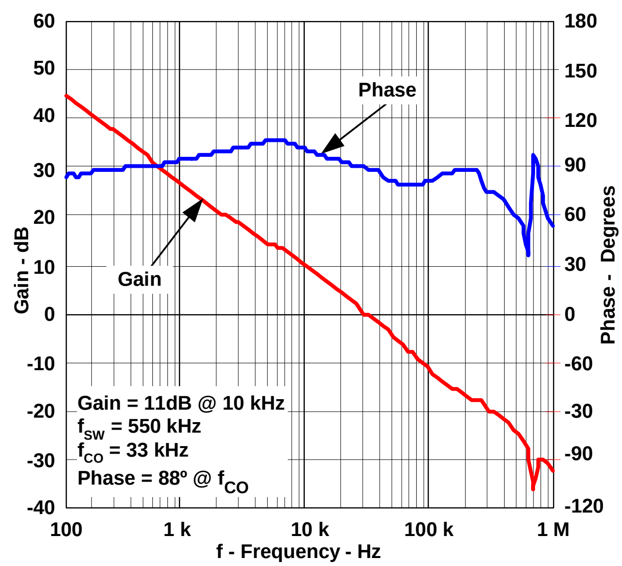

Fig. 6. Frequency response of converter using electrolytic capacitors.

E. Transient and Frequency Response of Converter Using Ceramic Capacitors

The load current transient response of a converter using ceramic output capacitors is shown in Fig. 7. TI's Evaluation module TPS54610EVM-213 using ceramic capacitors is selected for the comparison [5].

In case of ceramic capacitors, the first peak V_{m1} is negligible because of low ESR and ESL. The output ripple is also very low and practically does not affect peak-to-peak voltage deviation during the transient. However, the second peak V_{m2} is larger in comparison to the electrolytic capacitors. This difference occurs because ceramic capacitors experience the same excessive charge and discharge during the transients as electrolytic capacitors in previous section, but their capacitance is much lower. Selection of lower output inductance helps to reduce the charge applied to the capacitor during the transients because of the shorter time needed to change the inductor current to the new load level. However, it does not solve the problem if the feedback loop does not respond quickly on transient. The loop frequency response for this converter is shown in Fig. 8. The compensation circuit for this version is referred to as Circuit A for the comparison. It has a crossover frequency of 60 kHz and a gain of 12 dB at 10 kHz while for the converter with electrolytic capacitor the crossover frequency 33 kHz and the gain 10 dB at 10 kHz were sufficient (Fig. 6). Thus, an output filter with ceramic capacitors requires higher feedback loop bandwidth to provide similar transient performance as the electrolytic capacitors.

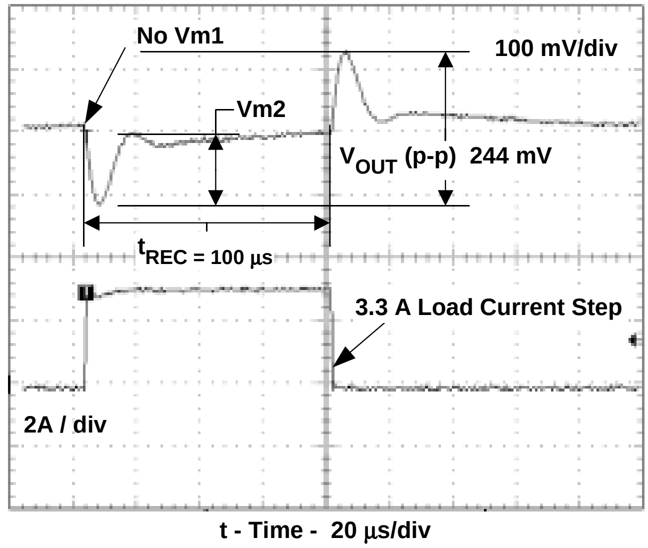

Fig. 7. Load currrent transient response of converter using ceramic capacitors.

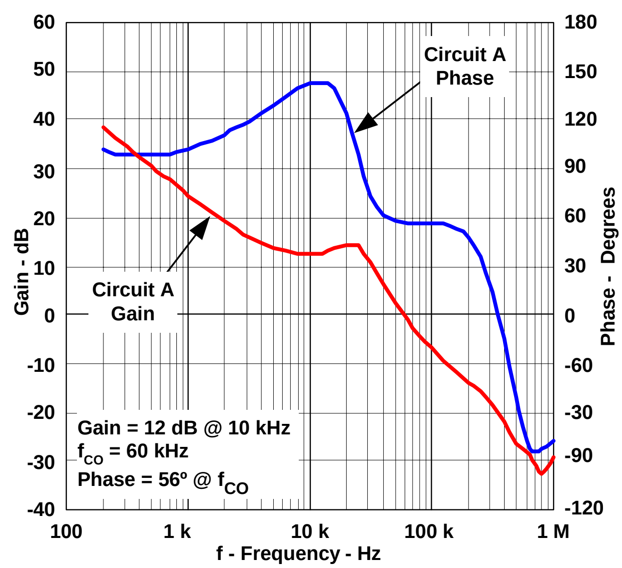

Fig. 8. Frequency response of converter using Compensation Circuit A.

Figs. 9 and 10 illustrate the effect of the increased bandwidth and gain feedback loop using Compensation circuit B. The feedback loop of the example shown in Fig. 8 has been modified to increase the crossover frequency up to 80 kHz and the gain up to 22 dB at 10 kHz. At the same transient conditions, 3.3-V input voltage, 1.8-V output and 3.3-A current step, the converter with higher gain and bandwidth has peak-to-peak transient response of 184 mV and recovery time of 20 µs (Fig. 9), while the converter with the original loop has 244 mV and 100 µs (Fig. 7). This is a 33% improvement of the peak-to-peak output voltage transient. To provide the same peak-to-peak transient response, the converter with low bandwidth requires more output ceramic capacitors, thus increasing the cost of converter.

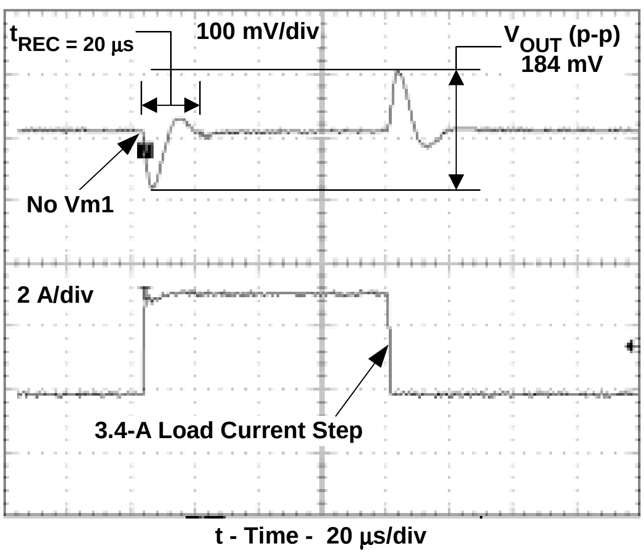

Fig. 9. Transient response improvement for the converter.

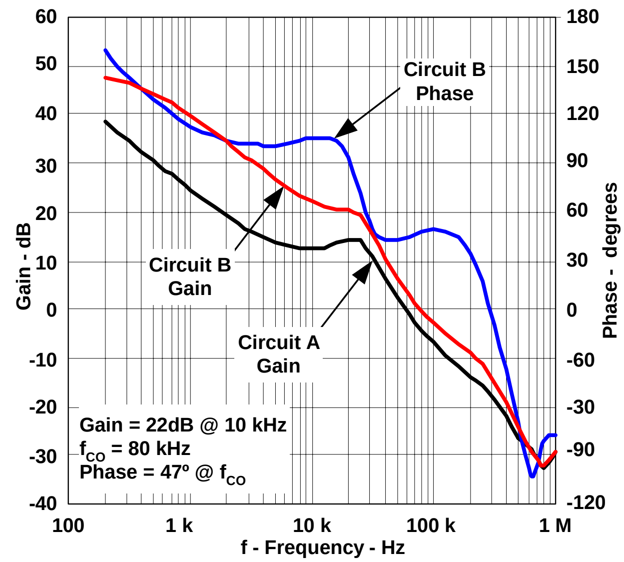

Fig. 10. Frequency response using Compensation Circuit B.

III. Accuracy of Small Signal Analytical Model for DC/DC Converter with Voltage Mode Control

Stable operation of switching DC/DC converters requires an adequate frequency response phase and gain margin. The previous section of this paper discussed the importance of high gain and bandwidth in the feedback loop for better transient response of DC/DC converters with ceramic output capacitors. Increased loop bandwidth requires careful consideration of converter switching delays, sampling, and error amplifier limitations that may affect accuracy of existing small-signal frequency response models. A simplified schematic of a synchronous buck converter with voltage-mode control is shown in Fig. 11. The overall frequency response loop has two main parts. The first part includes the power-stage, driver, and PWM comparator. The second part is the compensation circuit, which includes an error amplifier and additional impedances Z1 and Z2, which shape the required feedback-loop frequency response.

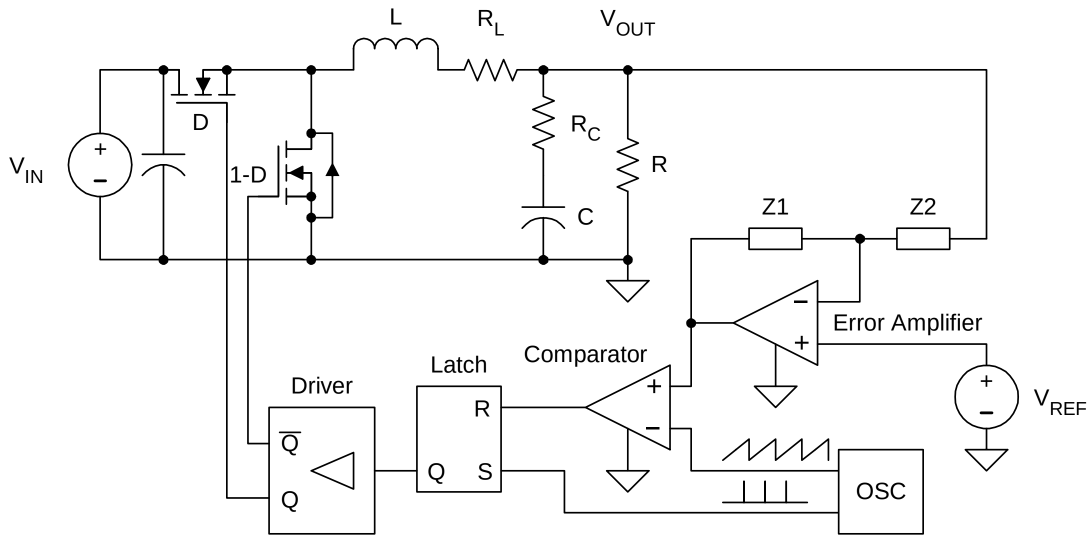

Fig. 11. Simplified schematic of voltage-mode control synchronous buck converter.

F. Power Stage and Modulator Transfer Function

The widely-used small-signal transfer function of the power stage and modulator for synchronous buck converter is defined by equation (1), where:

- V_S is the input voltage
- R is the load resistance
- L is the output inductance
- C is the output capacitance
- R_L is the sum of output inductor DC resistance and $R_{DS(ON)}$ of FETs
- R_C is the equivalent series resistance (ESR) of the output capacitor
- K_{PWM} ($=1/V_{PWM}$) PWM gain where V_{PWM} is an amplitude of the ramp modulation signal

It does not take into account any potential phase lag caused by modulator and driver delays and by sampling. To verify the validity of the equation, the frequency response is measured on a standard evaluation module with ceramic capacitors TPS54610EVM-213 from TI [5], at the following conditions:

- $Vs = 3.3$ V
- $V_{OUT} = 1.8$ V
- $R = 1800\ \Omega$
- $C = 3 \times 22\ \mu F$
- $R_C = 1\ m\Omega$
- $R_L = 58\ m\Omega$
- $L = 0.65\ \mu H$
- $V_{PWM} = 1$ V
- $F_{SW} = 700$ kHz

All further analysis and measurements are based on the same module TPS54610EVM-213. The schematic, list of materials, and other technical details related to this module are in [5].

Comparison of measured frequency response and plots calculated from equation (1) (Figs. 12 and 13) does not reveal any phase lag associated with the delay and sampling effect. The measured Bode plots closely replicate behavior of a second-order filter at frequencies up to 350 kHz (half the switching frequency, 700 kHz). Half of the switching frequency is the theoretical limit that determines whether small-signal analysis applies to the switching system.

$$Wpt(s) = Vs\left(\frac{R}{R+R_L}\right)K_{PWM}\frac{1+s\times R_C\,C}{1+s\left(R_C\,C+\dfrac{R\,R_L}{R+R_L}\times C+\dfrac{L_O}{R+R_L}\right)+s^2\times L_O\,C\times\left(\dfrac{R+R_C}{R+R_L}\right)} \qquad (1)$$

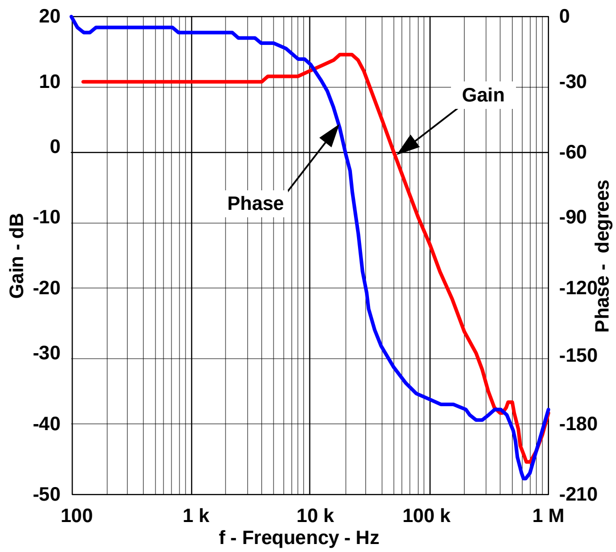

Fig. 12. Experimental results based on measurements.

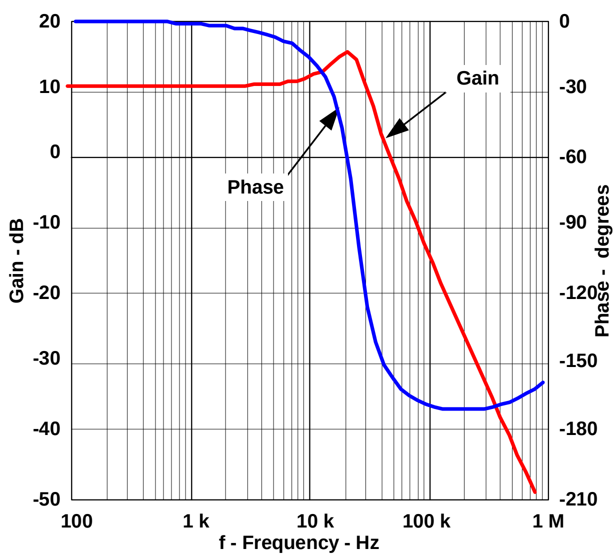

Fig. 13. Model in accordance with equation (1).

G. Transfer Function of Type 3 Compensation Circuit and its Limitation

The type 3 compensation circuit in Fig.14 is widely used for voltage-mode control because of design flexibility.

The generic transfer function of an ideal error amplifier with type 3 compensation is defined by equation (2):

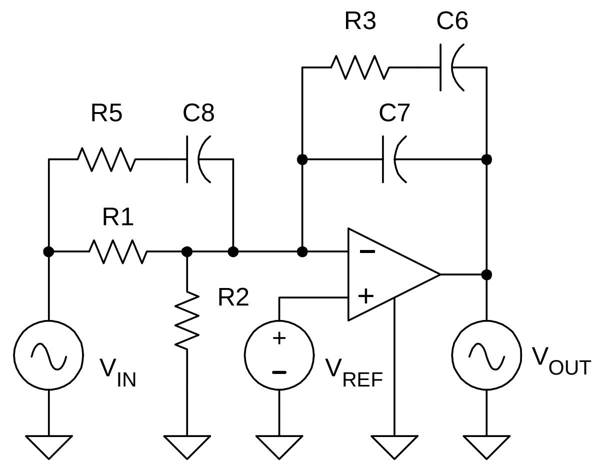

Fig. 14. Type 3 compensation circuit.

The type 3 compensation has a pole at the origin (integrator) that ensures high dc gain and resulting low output-voltage error of the converter. Additionally, a pair of available zeros provides required phase boost near resonant frequency thus allowing increased bandwidth of feedback loop. Another pair of additional poles sets required gain margin in high-frequency region. However, the actual frequency response measurements of converters with ceramic capacitors, designed for the high-bandwidth feedback loop, revealed an unexpected and sharp phase-lag at frequencies above 200 kHz.

$$W1(s) = \frac{[1+s\ C8\ (R1+R5)]\ (1+s\ C6\ R3)}{s\ (C6+C7)\ R1\ (1+s\ C8\ R5)\times\left[1+s\ R3\times\left(\frac{C6\ C7}{C6+C7}\right)\right]} \qquad (2)$$

The theoretical frequency response and experimental measurements are shown in Figs. 15, 16, and 17 for the comparison. The measured gain (Fig. 15) and gain based on equation (2) (Fig. 16, solid line) coincide well up to 200 kHz. At frequencies above 200 kHz, the measured gain declines at 20 dB/decade, while the theoretical gain still increases until it reaches a frequency of about 1 MHz. The internal gain of error amplifier, built into the same plot (Fig. 16, straight line), explains this effect. If the frequency response of the compensation circuit goes beyond the boundary of the error-amplifier internal bandwidth then the 20-dB/decade slope of the error-amplifier internal gain defines the phase of the compensation circuit

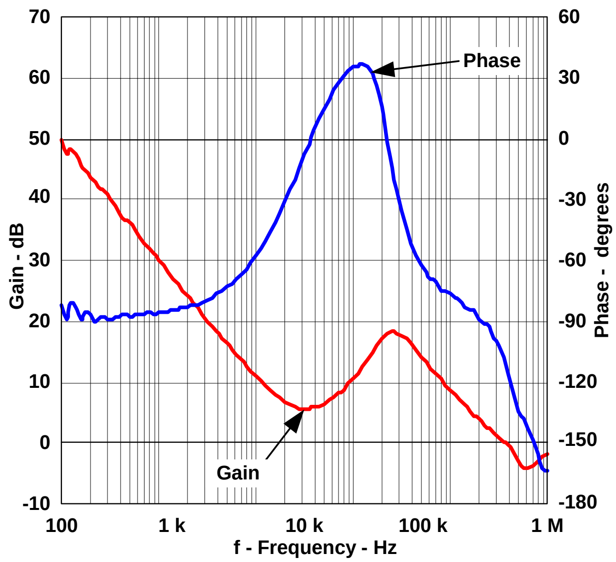

Fig. 15. Measured gain and phase.

The only way to avoid this issue with compensation circuit is to stay below the bandwidth limit of the error amplifier[9]. (The gain and phase based on this assumption are shown in Figs. 16 and 17 by dashed lines.) That means that higher bandwidth of the error amplifier is required to take full advantage of ceramic as opposed to electrolytic capacitors.

The transient of existing design may need to be improved even if the compensation circuit has reached the error-amplifier limit. Room remains for the transient response improvement but equation (2) is not valid above the error-amplifier limit.

However, an accurate equation can be derived that predicts gain and phase of frequency response when the compensation circuit exceeds the boundary of the error amplifier. The new equation helps to improve transient performance of a DC/DC converter using the existing error amplifier.

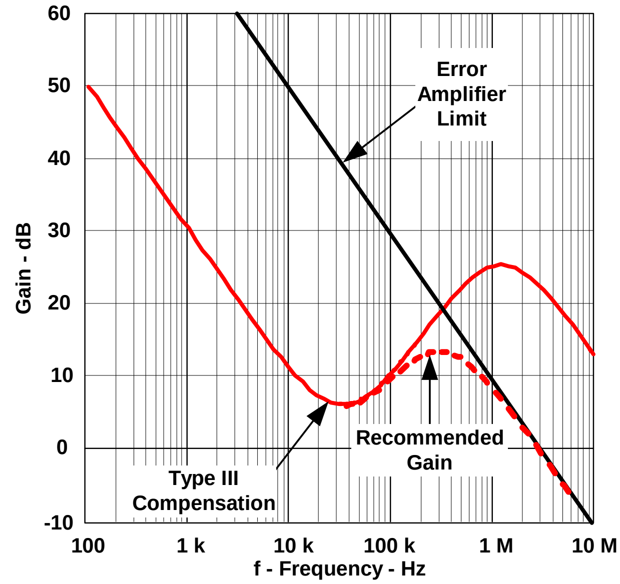

Fig. 16. Gain based on equation (2).

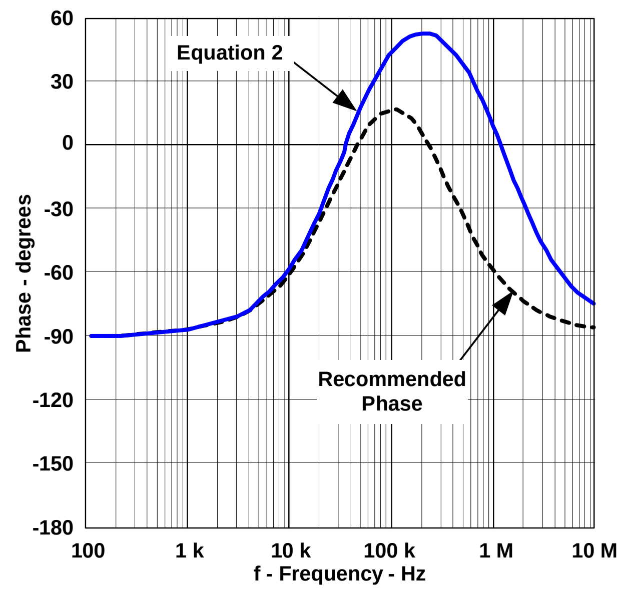

Fig. 17. Phase based on equation (2).

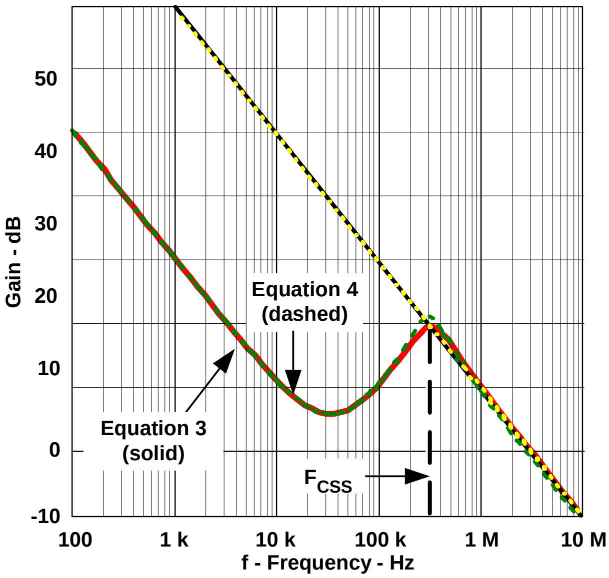

Fig. 18. Gain based on equations (3) and (4).

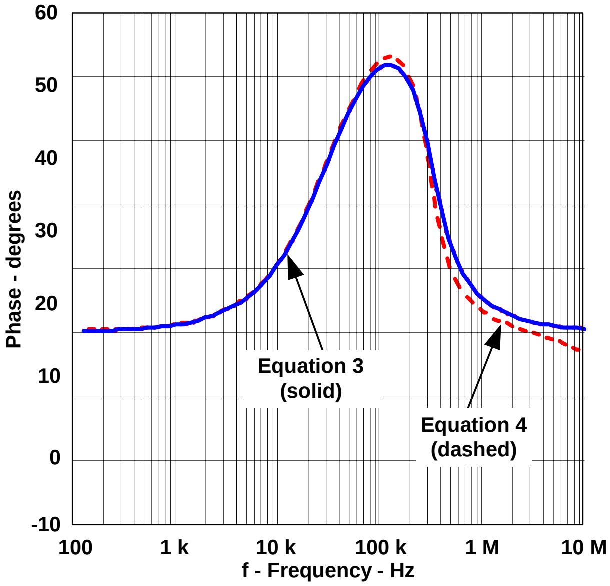

Fig. 19. Phase based on equations (3) and (4).

Assume that the compensation circuit frequency response curve, originally selected using equation (2), crosses the error amplifier boundary at the frequency F_{CSS} (Fig. 18).

The curve has positive 20-dB/decade slope below F_{css} and then changes its slope to negative 20 dB/decade above F_{css}. So, the total slope change is 40 dB/decade. This behavior is similar to the straight line approximation of a second-order filter with the resonant frequency equal to F_{css} and the quality factor Q = 1. The effect of the two poles in equation (2) is negligible, because they are located well above F_{css} (Fig. 16). With these assumptions, equation (3) below applies. A more general equation (4) describes a non-ideal inverting operational amplifier and is provided in equation (4) in [7].

$$W1(s) = \frac{(-a(s)\times Z1)}{(Z1 + Z2 + a(s)\times Z2)} \qquad (4)$$

The variable a(s) in this equation is the frequency response of non-ideal amplifier itself and Z1 and Z2 are the compensation circuit impedances shown in Fig. 11. This general equation becomes complicated after the substitution of all variables. However, it is preferable for the final design validation with the help of computer software tools.

The gain and phase of the compensation circuit in accordance with equations (3) and (4) are shown in Figs. 18 and 19 respectively. Fig. 18 also includes the boundary of the error amplifier, shown as the straight line to the right. The gain and phase based on the new equations (3) and (4) closely match the measured frequency response shown in Fig. 15. Note that equation (3) is most accurate if the high frequency poles in accordance with equation (2) are at least 4 times higher than F_{CSS}.

The frequency above 3 MHz must be excluded from the comparison, because the test setup is not highly accurate in the MHz region. That range is outside the practical design scope for this application.

$$W1(s) = \frac{[1 + s\ C8\ (R1+R5)]\times(1+s\ C6\ R3)}{s\ (C6+C7)\ R1}\times\left[\frac{1}{1+\left(\frac{s}{2\pi\times F_{CSS}}\right)+\left(\frac{s}{2\pi\times F_{CSS}}\right)^2}\right] \qquad (3)$$

IV. Worst-Case Stability Analysis at Two Critical Conditions

The following parameters affect the worst-case analysis based on equations (1) and (3):

- Operating conditions, including input voltage and load-resistance range.
- Power stage parameters, including output inductor and capacitor tolerances, resistance of power FETs, and DCR of the output inductor. Variations of these parameters are important, because the corner frequency and damping factor of the L-C output filter depend on these parameters.
- Internal error-amplifier and PWM-modulator tolerances, including gain and bandwidth of the error amplifier, ramp-signal variation, and additional phase lag when the compensation circuit frequency response exceeds the boundary of the error amplifier gain.
- External components, including three resistors and three capacitors and their tolerances when using type 3 compensation.

Two worst-case situations become obvious from the Bode plots in Fig. 8. The first one, based on the abrupt phase lag at frequencies above 200 kHz, is due to the limited bandwidth of the error amplifier. The extreme condition in this case occurs when the error amplifier has minimum bandwidth while the rest of the feedback loop has maximum gain and bandwidth. This condition occurs when the input voltage is high and the output inductor and capacitor are at their lowest values. In this situation, the compensation circuit may not provide the required phase-boost at frequencies above 200 kHz, because it is limited by the error amplifier bandwidth.

Another worst-case condition is at the minimum gain and bandwidth, where the resonant frequency of the output filter stays close to the crossover frequency. In Fig. 8 this is the area near 50-kHz frequency. Additional phase lag in this area because of feedback-loop tolerances may cause conditional instability at transients, or even unconditional oscillation if the gain is low enough at steady-state condition.

Table 2 shows the worst-case tolerances of all variables for these two conditions. The possibility of 14 different variables having worst-case condition is relatively low, but the statistical analysis of tolerances is outside the scope of this paper. Maximum load resistance is selected as the worst case for both conditions because lower damping means larger phase-lag for the second-order output filter.

Table 2. Worst Case Tolerances for the Two Extreme Conditions

Component/Parameter	Condition 1: Maximum Gain	Condition 2: Minimum Gain
Input voltage	$V_{S(max)}$	$V_{S(min)}$
Load resistance	Maximum	Maximum
Error amplifier bandwidth	3 MHz (minimum)	3 MHz (minimum)
Ramp signal	- 10%	+ 10%
Output inductor L	- 20%	+ 20%
Output capacitor C	- 20%	+ 20%
Compensation C6, C7, C8 (Fig. 14)	± 20%	± 20%
Compensation R1, R3, R5 (Fig. 14)	± 1% (± 3% over temperature)	± 1% (± 3% over temperature)

Worst-case Bode plots, calculated for Conditions 1 and 2 in accordance to Table II, are shown in Figs. 20 through 23. All data for the analysis are taken from [5], except that C1 is 270 pF instead of 470 pF, and C4 is 3300 pF instead of the original 470 pF (p. 4-2, Fig. 4-1 in [5]). The solid line shows frequency response when all feedback loop parameters have nominal values. The dashed and dotted lines show Bode plots at Conditions 1 and 2 at worst-case tolerances of components R1, R3, R5, C6, C7, and C8 (Fig.14). For Condition 1, minimum phase margin is about 43°, and for Condition 2 it is about 38°. The input voltage for Condition 1 is 6 V and for Condition 2 is 3 V. The phase margin varies from 38° to 55° and gain margin from -10 dB to -26 dB after taking into account all worst-case conditions and tolerances. The crossover frequency varies in the range from 45 kHz to 130 kHz. At minimum load resistance, the damping is higher, phase shift is lower and the phase margin is even higher. This analysis shows that 45° phase margin, -10 dB gain margin, and 100 kHz crossover frequency can be taken as the design goal at nominal conditions for the voltage-mode control, synchronous buck-converters using ceramic capacitors in the output filter. This combination allows stable operation at worst-case conditions and good dynamic response of DC/DC converter at large load-current transients

V. Feedback Loop Design Recommendations

Most recommendations and design rules for selecting feedback-loop bandwidth and stability margins are based on industry's long-time experience with electrolytic capacitors [3], [4]. Usually, a phase margin ranging between 45° and 60° is recommended to avoid instability caused by feedback-loop variation because of components and parameters tolerances. The crossover frequency or feedback-loop band-width does not exceed 30 kHz in most designs using electrolytic capacitors. However, as mentioned in the previous section, the much lower tolerances of ceramic capacitors with X5R and X7R dielectrics as compared to tolerances of electrolytic capacitors allows selection of a comfortable 45° margin in most cases.

The outline below summarizes the lessons learned during an analysis, design, and performance measurements of DC/DC converters with ceramic-output capacitors using voltage-mode control. It specifies the design goals, outlines potential limits, and provides recommendations helpful for optimizing feedback-loop design for the best transient response while maintaining a comfortable margin for stability.

A. Design Goals

- Design for highest gain and bandwidth feedback loop, while allowing for worst-case conditions at any practically reasonable combination of feedback-loop tolerances.
- Provide phase margin of 45° for ceramic capacitors and 65° for electrolytic
- Allow at least 10 dB gain margin for less jitter and noise sensitivity.

B. Feedback Loop Limitations

- The error amplifier may limit compensation-circuit bandwidth.
- Crossing the frequency-response boundary of the error amplifier by the compensation circuit initiates a sharp phase lag at frequency about half a decade below crossing.
- Switching frequency may also limit crossover frequency: $F_{CO} < F_S/2$ (theory), $F_{CO} < F_S/5$ (practice).
- Abrupt phase lag at frequency above resonant might cause the conditional instability.
- Two conditions at worst-case tolerance combinations require verification for stability.

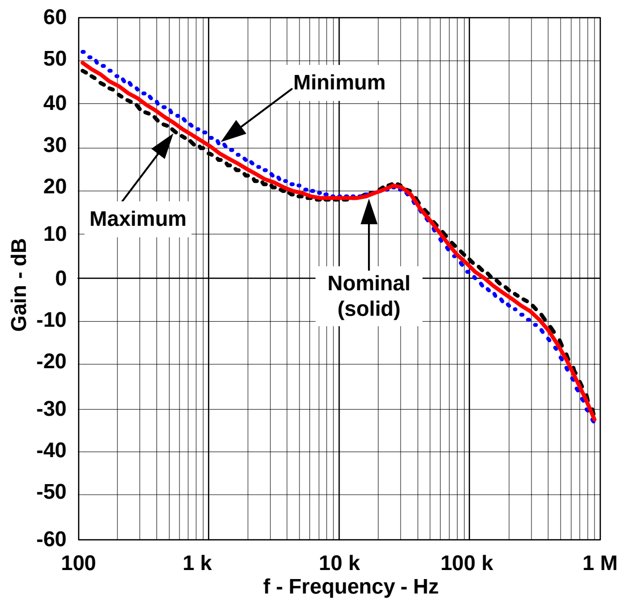

Fig. 20. Gain at worst case Condition 1.

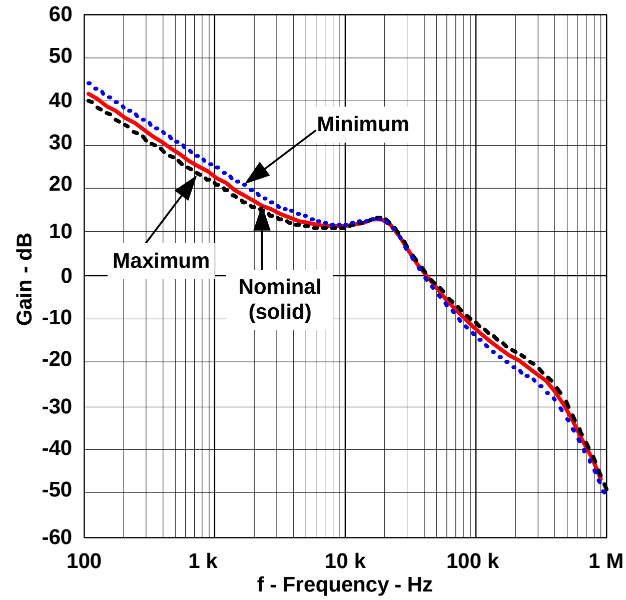

Fig. 22. Gain at worst case Condition 2.

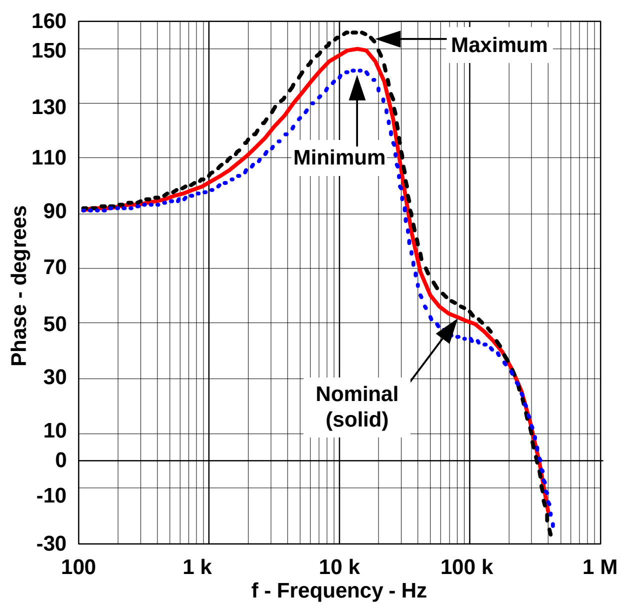

Fig. 21. Phase at worst case Condition 1.

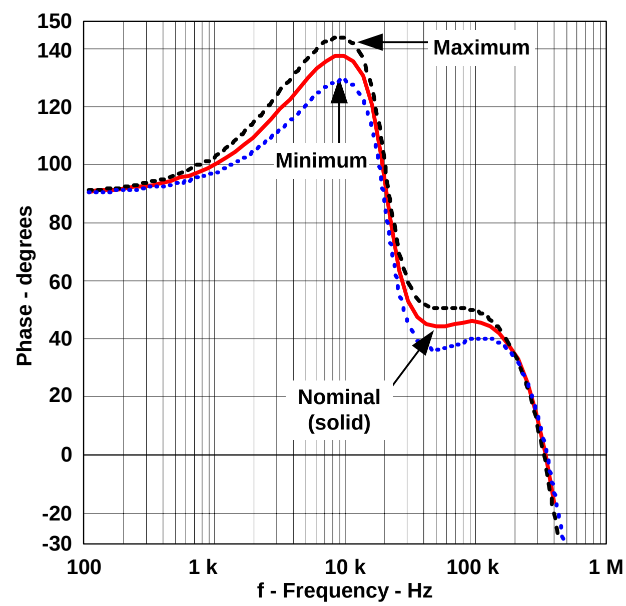

Fig. 23. Phase at worst case Condition 2.

C. Recommendations

- Keep gain and bandwidth as high as possible for good transient response.
- Use type-3 compensation circuit to provide proper phase boost.
- Accept compensation-circuit gain to between 10 dB and 20 dB at switching frequency. The low output-ripple of ceramic capacitors does not cause significant jitter of switching waveforms with this gain.
- Recognize that the frequency of ESR-zero does not affect compensation circuit design, because it is in MHz range. This is well above of the considered frequency range.
- Increase the bandwidth by putting two equal poles as high as possible, but not above the error-amplifier limits. Use of equation (3) for the compensation circuit allows design for higher bandwidth and improved transient response.
- Ensure that the crossover frequency does not exceed one-fifth (1/5) of switching frequency.
- After frequency of equal poles is located on the basis of maximum achievable crossover frequency, locate the fist zero in accordance with the equation

$$Fz1 = \frac{\left(Fr^2 \times 10^{\frac{1}{Q}}\right)}{Fp1} \tag{5}$$

where:

  - F_r is resonant frequency
  - Q is the quality factor

- Locate the second zero to ensure 45° phase margin at crossover frequency. If necessary, move this zero into lower frequency region to guarantee 30° phase margin at the frequency

$$Fr \times 10^{\frac{1}{2Q}} \tag{6}$$

These design goals and recommendations have been implemented in the Mathcad™ file. The file includes not only worst-case feedback loop design for voltage mode control, but also steady state design including RMS currents, ripple, power losses, efficiency, etc. The file also generates main waveforms of power stage. This file is available for free distribution upon request [6].

VI. Conclusion

The main characteristics of ceramic capacitors versus electrolytic, OS-CON, and specialty polymer capacitors are compared. The pros and cons of use of ceramic capacitors in the output filter of DC/DC converters are analyzed and illustrated by measurements. Currently available ceramic capacitors, with thermally stable X5R and X7R dielectrics, provide a low cost, small size, low ripple solution but require optimal feedback loop design. The effect of feedback loop bandwidth and gain on the load-current transient-response is confirmed by experiments. Based on experiments, modification of the small-signal transfer function of synchronous buck converter for voltage mode control is described that takes into account error amplifier limitations. This analytical model is used for the worst-case stability analysis of DC/DC converters with ceramic output capacitors. Two worst-case conditions are investigated covering 14 different variations of feedback loop parameters and components. General recommendations for the optimal feedback loop design of synchronous buck converter with ceramic output capacitors are provided. This algorithm is implemented in a Mathcad-based program that includes complete steady-state and small-signal design of a buck converter.

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