

# TMS320F2802x Power Reference Design

*PMP - DC/DC Low-Power Converters*

## ABSTRACT

This design was created to help those desiring to design-in the TMS320F2802x into a system using a 5-V input voltage bus and is interested in using a power device with integrated FETs for high-efficiency, ease of use and low part count.

## 1 Features

- 5-V  $\pm 10\%$  input voltage
- Integrated upper FET for minimal external passive device count
- TPS62203 is capable of up to 300-mA continuous operation
- Efficiency is greater than 94% at 150 mA
- Power Save mode available for maintaining high efficiency at light loads

## 2 Introduction

This reference design is for the TMS320F2802x devices and accounts for voltage, current, and sequencing requirements given below. The operating input voltage is 4.5 V to 5.5 V. This design is optimized for ease-of-use and quick design time.

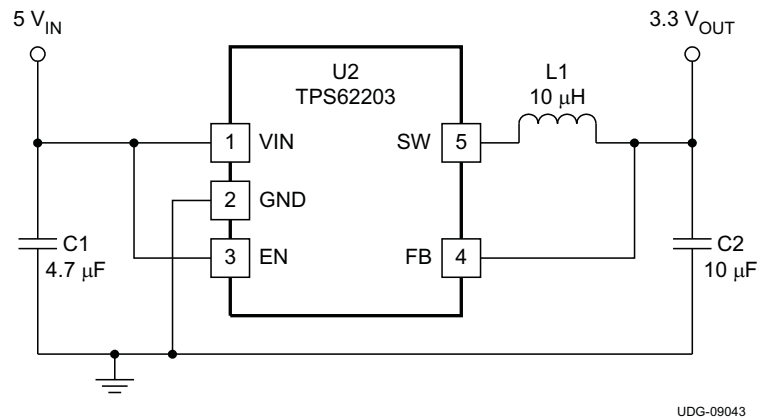
## 3 Requirements

The TMS320F2802x requires a single 3.3-V rail. An internal regulator inside the F2802x provides power to the device core.

**Table 1. TMS320F2802x Power Requirements**

	PIN NAME	VOLTAGE (V)	I <sub>MAX</sub> (mA)	TOLERANCE	SEQUENCING ORDER	TIMING DELAY	OTHER
I/O	VDDIO	3.3	80 <sup>(1)</sup>	$\pm 5\%$	--	--	Internal regulator supplies power to device core
I/O	VDDA	3.3	20	$\pm 10\%$	--	--	

<sup>(1)</sup> I<sub>MAX</sub> in table is for 40 MHz operation. At 60 MHz, I<sub>MAX</sub> = 125 mA


**Figure 1. PMP4250 Reference Design Schematic**

#### 4 List of Materials

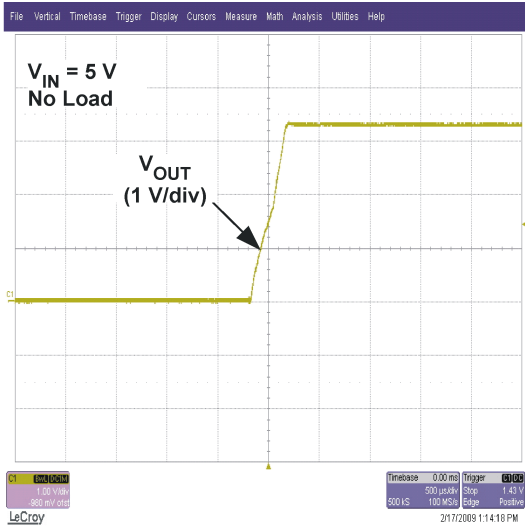
**Table 2. PMP4250 List of Materials**

REF DES	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
C1	1	4.7 $\mu$ F	Capacitor, Ceramic, 10 V, X5R, 15%	0603	Std	TDK
C2	1	10 $\mu$ F	Capacitor, Ceramic, 6.3 V, X5R, 15%	0603	Std	TDK
L1	1	10 $\mu$ H	Inductor, SMT, 120 m $\Omega$ , 1 A	0.185 in <sup>2</sup>	CDRH4D28-100	Sumida
U1	1		IC, step-down converter, 3.3 V, 3000 mA	SOT23-5	TPS62203DBV	TI

## 5 Test Results

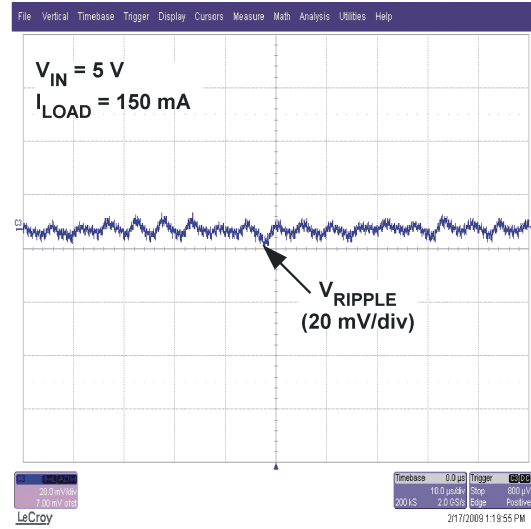
### 5.1 Test Results

For [Figure 2](#) through [Figure 5](#) are taken at 3.3-V at 150 mA.



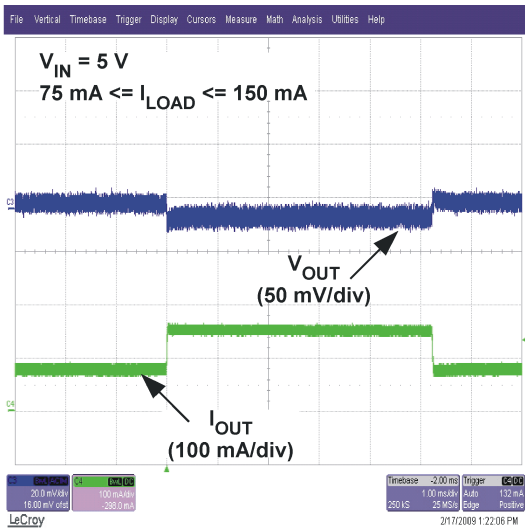
t – Time – 500  $\mu$ s/div

Figure 2. Turn-On



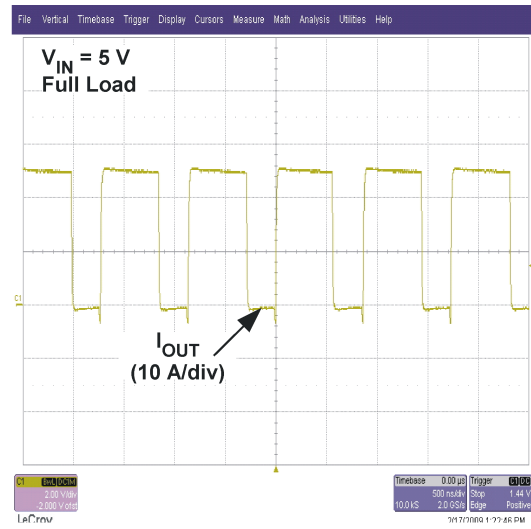
t – Time – 10  $\mu$ s/div

Figure 3. Output Voltage Ripple



t – Time

Figure 4. Transient Response



t – Time

Figure 5. Switch Node

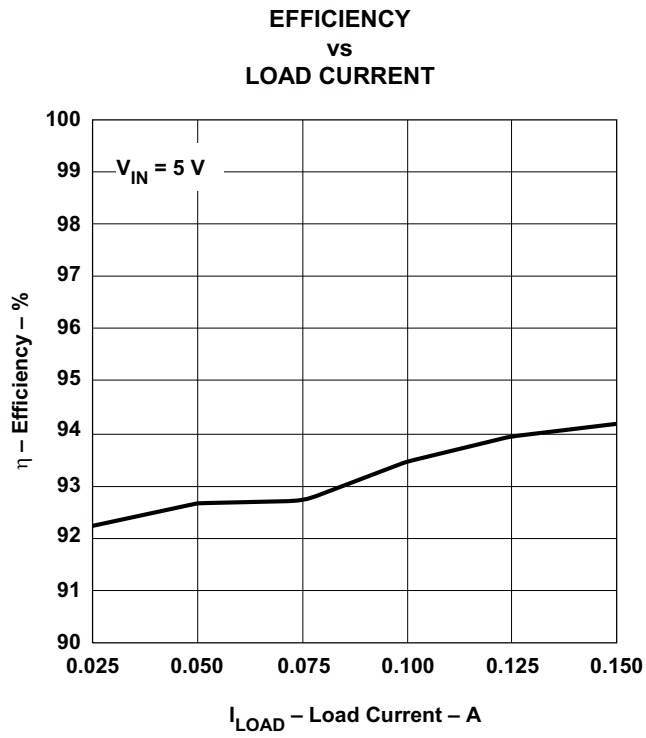


Figure 6.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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