

Battery Circuit Architecture

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ABSTRACT

Battery-pack requirements have gone through a major evolution in the past several years, and today's designs have considerable electronic content. The requirements for these batteries include high discharge rates, low insertion loss from components in series with the cells, high-precision measurements, redundant safety protection, and no upset with very high electrostatic discharge (ESD) transients. Virtually all Li-ion protector circuits for one- and two-cell applications have protector FETs in the low (negative) side of the battery. Key issues particular to a low-side Li-ion protector circuit are discussed. The transients produced when the Li-ion protector opens during a momentary short or when the battery is unplugged while under load may exceed the voltage rating of semiconductors in the battery pack. This topic describes a number of design issues and proposes solutions to resolve or improve them. Resolution of these issues requires attention to both the circuit design and the printed circuit board (PCB) layout.

I. TYPICAL BATTERY CIRCUITRY FOR A LI-ION BATTERY PACK

Fig. 1 is a block diagram of circuitry in a typical Li-ion battery pack. It shows an example of a safety protection circuit for the Li-ion cells and a gas gauge (capacity measuring device). The safety circuitry includes a Li-ion protector that controls back-to-back FET switches. These switches can be

opened to protect the pack against fault conditions such as overvoltage, undervoltage, and over-current. The diagram also includes a temperature-sensitive three-terminal fuse that will open due to prolonged overcurrent or overtemperature, or it can be forced to open by redundant protection circuitry in case there is a fault where the primary protection circuitry fails to respond. Opening this

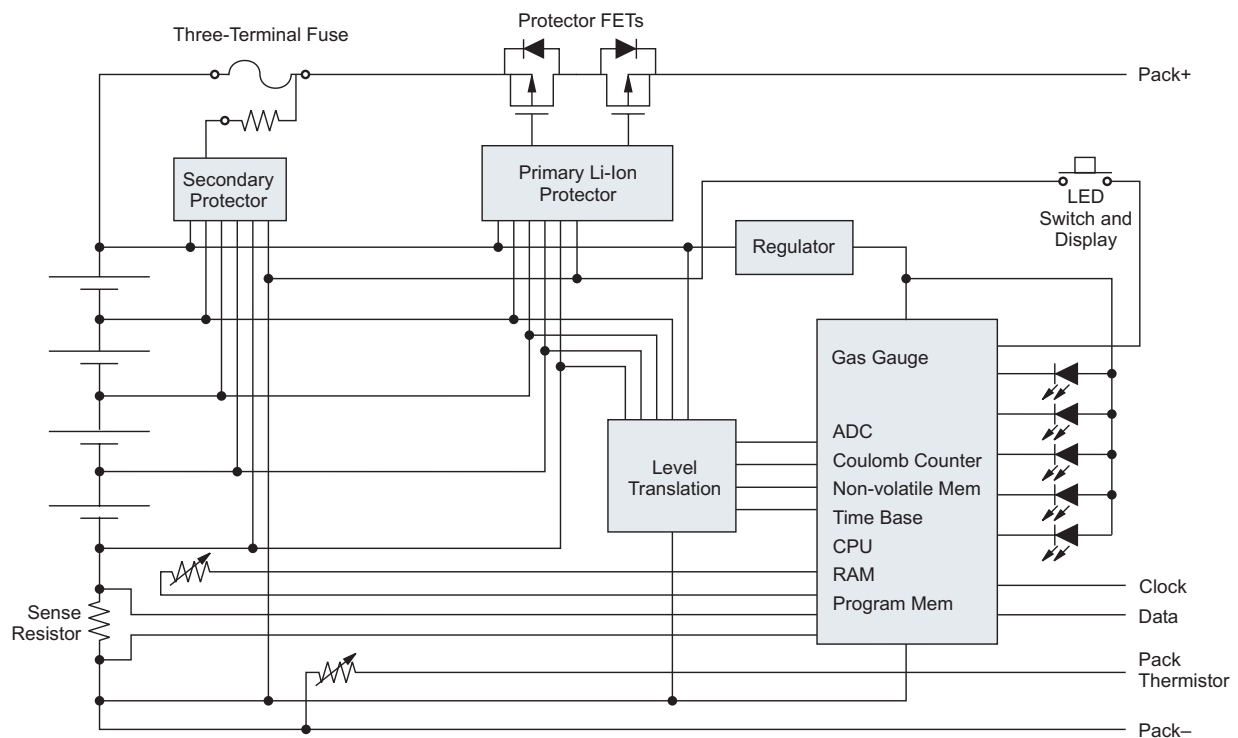


Fig. 1. Block diagram of circuitry in a typical Li-ion battery pack.

fuse is a last resort, as it will render the pack permanently disabled. The gas-gauge circuitry measures the charge and discharge current by measuring the voltage across a low-value sense resistor with low-offset measurement circuitry. The current measurement is integrated to determine the change in coulometric capacity. In addition, the gauge measures temperature and voltage, evaluates gas-gauging algorithms to determine the available capacity in the battery, and computes time-to-empty and other values required by the host. The available capacity as well as other measurements and computational results are communicated to the host over a serial communication line. A visual indication of available capacity can be displayed by the LEDs when activated by a push-button switch.

II. OPTIMIZING THE DESIGN FOR MEASUREMENT ACCURACY

Measurement accuracy requires an accurate measurement data acquisition system and measurement sensor and also requires a careful board layout. If the designer does not pay attention to all these items, the resulting system performance may not deliver the expected results.

The sense resistor and how it is connected to the data acquisition system are critical design decisions. The sense resistor may see changes in temperature that are much larger than the ambient variations of the battery pack due to power dissipation in the resistor. Use of a low-temperature coefficient resistor will improve available capacity and current-measurement accuracy. The effective sense resistance seen by the measurement circuitry may depend on how the printed circuit board (PCB) etch is connected to the sense resistor. If the sense resistor is connected in such a manner as to include some of the PCB etch resistance in the actual sense resistance seen by the measurement circuitry, the effective resistance is increased. In addition to having a larger resistance than intended, the portion of the effective sense resistance that is due to copper etch will have a very high temperature coefficient (0.39%/°C). The best practice is to connect the sense resistor into the circuitry at the location that includes the least amount of copper trace in the current path. If this

method is followed, there will be very little error due to the voltage drop across the connection, and the connection resistance will not add to the effective sense resistor value.

If single-ended measurements are made on the voltage across the sense resistor, it is critical that the V_{SS} of the measuring device be connected to the sense resistor with much care. In the single-ended system, the measurement system ground provides one of the inputs for the measurement. The value that is measured is the difference between the single-ended input and the measuring system ground. If the measuring system ground path has a voltage difference between the on-chip ground and the ground end of the voltage measurement desired, this difference will create an error. The measurement system ground should tie to a low-current ground etch. The low-current ground should be separated from the high-current ground, and the ground end of the sense resistor should be the tie point where the low-current ground is tied to the high-current ground. This will also provide a more robust design for electrostatic discharge (ESD), as discussed later.

Voltage measurements of the battery stack are also affected by PCB layout and connection drops. Some battery-pack designs may use nickel straps from the PCB connection to the battery stack. Nickel is used because it is easy to weld to the battery cells, but its resistance is five times as much as that of copper. When current flows through these straps, the voltage measured by the circuitry on the PCB connected to these straps will not measure the true cell voltage. To measure the true cell voltage, separate voltage measurement connections should be made with wiring that does not carry the load current. This drop may not be significant, but if the circuitry measures each cell voltage, such drops will cause the top and/or bottom cells to measure lower or higher (with discharge or charge currents) than the other cells. The same issue exists for copper etch routing on the PCB. A high-current-carrying conductor on the PCB will have a voltage drop across it. In general, the voltage measurement connections need to be made so that these connections have very little current flowing through them between the desired measurement point and the input to the

measurement IC. If the gas-gauge algorithm uses the lowest cell voltage for determining when the battery is empty, a small voltage drop may represent a significant capacity error and cause the gauge to report a smaller available capacity from the battery. If single-ended measurements are made of the voltage across the sense resistor and also of the voltage, accuracy considerations dictate that the sense resistor ground connection should be very close to the cell stack ground connection.

III. THERMAL ISSUES

There can be a lot of power dissipation in the battery pack. There will be some temperature rise due to power dissipation in the cells. High currents can also produce appreciable heat from the protector FETs, sense resistor, and even etch and wiring resistance. Make sure that intended temperature measurements are not elevated due to proximity of the thermal sensor to various heat sources. For example, if the substrate temperature of an integrated circuit (IC) mounted to the PCB is being measured, a narrow etch that runs under the IC may raise the reported temperature by at least 6° with as little as 2 A flowing through the etch. This is disastrous if the design is a NiMH or NiCd pack and the temperature measurement is used to determine full charge by a dT/dt charge termination. An increase of charge current can cause a false detection of a fully charged condition due to an increased dT/dt value. Excessive temperatures may also degrade the measurement accuracy of the gas gauge by causing drift in the on-chip reference. A good design practice is to avoid placing any measurement component close to the heat sources – for example, the protector FETs and sense resistor.

IV. TRANSIENT PROTECTION

Most designers will recognize the need to add transient protection across the pack output terminals if the battery is used to drive a motor or highly inductive load. However, many designs with non-inductive loads do not have any transient-limiting devices and depend only on some small capacitors to attenuate the transients. Li-ion cells have a relatively high inductance for their size due to construction techniques. If a

battery pack is removed from the system while under load, there is an opportunity for a damaging transient to occur. The battery pack should have sufficient capacitance to reduce transients or have something to clamp them. An even greater danger exists if there is a momentary short across the battery pack. The Li-ion safety protector may open to protect the cells from this short. If the FET switch in the protector opens quickly, the $L \times di/dt$ transient may be very large. Capacitance or transient-limiting devices on the output of the pack will not see this transient. The transient will appear on the cell side of the protector. There is a potential to damage any components tied to the cell side of the protector if there is not sufficient capacitance or other means to attenuate the transient across the cell stack.

V. LOW-SIDE PROTECTOR ISSUES

Virtually all one- and two-cell Li-ion protectors are low-side protectors, where the protector FETs are located between the negative lead of the battery cell stack and the battery negative terminal. There are several issues that can result depending on where the designer chooses to insert the protector FETs with respect to the battery-pack electronics.

The Li-ion protectors typically use p-channel FETs for high-side protectors and n-channel FETs for low-side protectors. The available voltage to turn on the FETs is lower for a one- and two-cell protector, and a low-threshold n-channel FET is cheaper and has better performance than a low-threshold p-channel FET.

Circuitry in a battery pack, such as a gas gauge, needs to measure the battery-cell stack voltage at all times. This drives the decision to place the Li-ion protector FETs between the ground connection of the battery electronics and the negative pack terminal. This decision creates two design issues that can exist when the Li-ion protector FETs are open. Any communication between the host and the battery electronics may be disrupted when the protector FET opens. The more serious issue involves safety. There is a sneak path for continued charging of the Li-ion cell stack. If the protection FETs are opened due to an overvoltage condition, this path allows the

cells to continue charging – the very condition that the protector is attempting to prevent.

Virtually all ICs will have an internal substrate diode from communication lines to the V_{SS} ground connection. This diode is part of the ESD protection structure in the device. A typical device will be protected to 1.5 to 2 kV by this internal structure. Typical end-equipment specifications will have an ESD requirement of 15 kV, requiring additional ESD protection components. The internal substrate diode and the external ESD protection components may both provide a return path for sneak charging currents from a charger that fails in a high-voltage fault condition. Fig. 2 shows the path where the charge current may flow. If the charger voltage exceeds the high-voltage trip threshold of the protector by more than one diode drop, the IC substrate diode will be forward-biased, and charge current can flow whenever the host drives the communication line to a logic zero. Resistance in the communication line will limit the peak current flow, and the duty cycle of a logic low on the communication line will affect the average current flow.

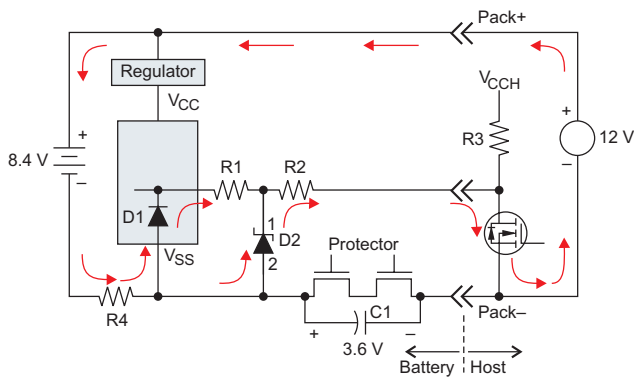


Fig. 2. Sneak charge-current path from a high-voltage charger failure.

There are basically three ways to prevent the sneak charging from a high-voltage charger when low-side protectors are used. The most popular way is to add a blocking diode in the communication line. A second way is to detect a high-voltage condition and gate the communication driver so that it cannot pull low when the high-voltage condition exists. The third way is to add a high-side FET in series with the charger and to turn it off if

a high-voltage condition exists. These methods are shown in Fig. 3. To implement the first method, a diode is placed in the communication line with a parallel capacitor and high-value pull-down resistance on the battery side of the diode. The diode is typically a Schottky diode to reduce the impact on the communication noise margin. The capacitor provides AC coupling of the communication waveform around the diode and also protects the diode from ESD damage. The pull-down resistance provides a DC restoration path for the charge on the added capacitor.

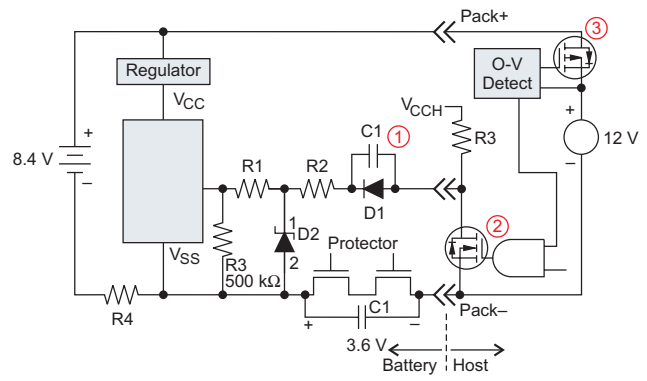


Fig. 3. Preventing the sneak charge-current path from a high-voltage charger failure.

VI. ESD CONSIDERATIONS

Most battery-pack requirements include surviving multiple ESD hits from both direct connection and air-gap spark discharges. The equipment must generally withstand both positive and negative discharges of at least 15 kV to all connector pins as well as to the case of the battery pack. Most requirements go further than just requiring survival, insisting that there be no observable disruption in performance. Since the component ratings are generally much lower than 15 kV (2 kV or less), the electronics must include protection components and design countermeasures to reduce the ESD damage and upset potential.

ESD damage control is generally provided by shunt zener diodes, transient suppressors, and capacitors. Series resistors may be used to limit the peak current flow. It is noteworthy that 15 kV may arc across the body of some small resistors, reducing or eliminating their effectiveness for

limiting current flow and for decoupling. The key to designing circuitry that meets ESD requirements is an understanding of where the peak current from the ESD event will flow, the potential for both capacitive and magnetic coupling onto other signal lines, and the possibility for secondary arcing from the input that received the discharge.

Where the Current Flows – The ESD event will result in a very fast-rising voltage and current pulse on the line that receives the discharge. The discharge will seek the lowest-impedance path to earth ground. In a battery pack, the largest capacitance to earth ground is from the battery cells through the case to a hand or other surface adjacent to the pack. If ESD is applied to the Pack+ or Pack– connector terminals, the current path is obvious. If ESD is applied to a communication or other interface signal, the current will find the lowest-impedance path to the cells.

The Effect of the Discharge – The ESD event may cause a 1-ns rise-time voltage pulse of several thousand volts and/or over 30 A of momentary current flow. The fast-rising voltage spike can capacitively couple onto any etch and components adjacent to the affected line. The fast-rising current flow from the discharge will create a large inductive voltage drop along the path of the current flow. It will also create a magnetic field from the current flow that can induce transients into other circuitry through the nearby components and etch runs.

VII. ESD DESIGN HARDENING

Start the hardening process at the connector. One popular technique for improving ESD susceptibility is to build a spark-gap structure in the outside etch layer behind the battery-pack connector. This is a low-inductance (wide) ground etch that runs close to the etch-pad connections for the other connector pins. The etch structure provides a small clearance between points, or corners, in the etch to encourage a breakdown from a high voltage across the clearance. The clearance must be kept free from solder mask, as the solder mask would increase the voltage breakdown of the gap enormously. A 10-mil gap has a voltage breakdown at sea level of about

1500 V. This breakdown voltage is typically less than the damage threshold of IC inputs. The spark gap will tend to clamp the peak voltage on the connector pins other than ground and divert much of the charge to the ground etch. If the ground etch is handled carefully, this approach can significantly improve the ESD susceptibility of a design. Fig. 4 shows a typical ESD spark-gap structure in the etch pattern around the pack connector.

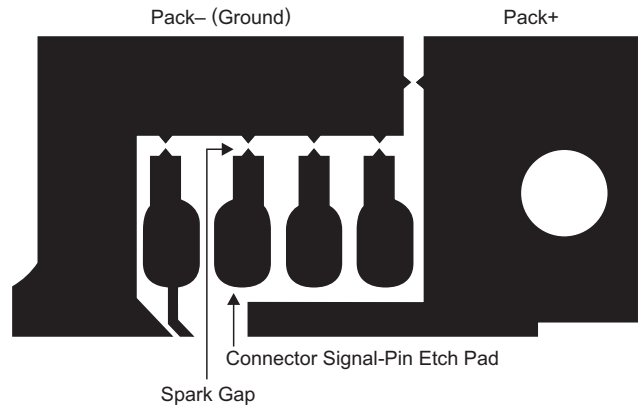


Fig. 4. Typical ESD spark-gap structure at pack connector.

Keep the etch connecting to the top and bottom of the cell stack away from all sensitive components. If the connections to the cell stack run the full length of the PCB, upset from an ESD event is much more likely due to the capacitive and magnetic coupling to nearby components and etch runs. If the Pack+ and Pack– connections can route through the protector FETs and sense resistor and then immediately leave the PCB and connect to the cell stack, a large portion of the PCB may be relatively free from coupling from an ESD event. Fig. 5 shows a sketch of component placement and etch routing that may yield a design with very high ESD susceptibility limits.

The recommended design practice is to separate the high-current ground etch from the low-current ground etch. Even a small inductance on the high-current ground etch will develop a large potential across the length of the connection due to the extremely fast dI/dt from the ESD event. If sensitive circuitry has connections to ground at different points along the high-current ground path, there may be a large differential voltage between these connections during an ESD

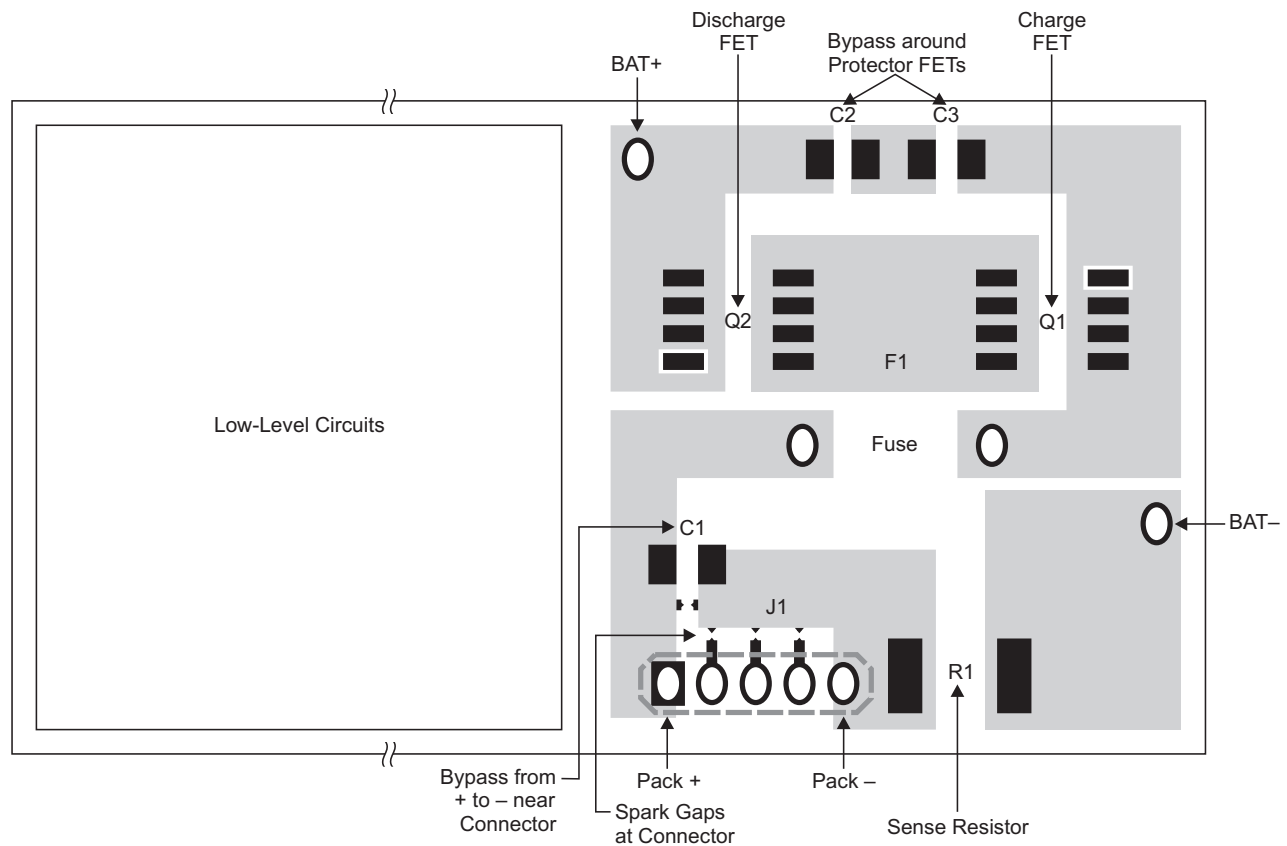


Fig. 5. Component placement and routing to achieve good ESD performance.

event. This differential voltage may allow some inputs to be momentarily pulled lower than V_{SS} , and the resulting substrate current flow can cause upset of the circuit performance. The best way to handle this issue is to connect all the low-current grounds together and then tie the low-current ground to the high-current ground at a single point. Make sure that none of the ESD protection components, such as shunt zener diodes or transient suppressors, tie to the low-current ground but tie to the high-current ground instead. This greatly reduces the possibility for ESD to cause current flow through the low-current ground and to create differential voltages between different ground connections.

Keep bypass capacitor leads short. It is very important to keep from canceling the high-frequency capability of a good ceramic capacitor by adding an inductor in series with it. This is what happens when care is not taken to keep *both* connections to the bypass capacitor short and wide. A long connection on the ground side of the capacitor is just as bad as a long connection to the

signal side. Use of a ground plane, where practical, makes this a lot easier. If an electrolytic capacitor is required to obtain the needed bulk capacitance, add an additional ceramic capacitor in parallel to take care of the high-frequency bypass requirement. The frequency components in an ESD pulse are so high that even ceramic capacitors will seem inductive. Some critical circuits may benefit from a small-value (68- to 100-pF) ceramic capacitor in parallel with a larger (0.1- μ F) bypass ceramic capacitor because the impedance of the small-value capacitor may be much less at the higher frequency due to much lower series inductance. Long connections to series components may not be a problem and, in fact, may add some inductance that will aid in decoupling. For example, some designs use small inductors in series with V_{CC} connections to aid in decoupling an ESD transient from a sensitive circuit.

Placing a capacitor across the Pack+ and Pack- connector pins very close to the connector and using short and wide etch runs can reduce the ESD susceptibility. This placement will provide

an alternate path for a portion of the current pulse from a Pack+ or Pack- ESD hit and reduce the peak current amplitude through the etch runs to the battery cells. This may provide some improvement in the peak ESD voltage transient level that the pack can withstand.

The Li-ion protector FETs will be in either the positive or negative high-current path from the connector to the battery cells. A capacitor around the protector FETs will provide a current path for ESD as well as help to minimize peak transient amplitudes when the protector FETs are switched off. The shunt capacitor will help limit the voltage transient across the FETs during an ESD event. Most designs have two capacitors in series for redundancy, so that shorting of a single capacitor won't disable the safety protection.

Protecting communication or other interface signals with zener diodes and/or transient suppressors is mandatory. The shunt suppression component should tie to the high-current ground as mentioned previously. It is very important to insure that the impedance of the path intended to shunt the transient to ground be significantly lower than the series impedance to the device input being protected. A long, thin connection to the transient suppressor may severely reduce the effectiveness of the protection components. It is generally helpful to add some series impedance both before and after the shunt zener diode or transient suppressor. Resistance between the pack connector and a shunt zener diode may reduce the peak current through the latter and keep it from failing. The zener diode normally fails as a short and will render the interface signal useless. The series resistance may need to be a larger package style that will withstand a larger voltage without arcing. This resistance may also protect the zener diode from failing due to a momentary short from the interface signal to Pack+. The larger resistor package will also withstand a momentary overload for a longer time. Resistance between a shunt zener diode and the IC input is also effective to reduce the potential for upset. The IC input will generally have an ESD protection structure that has a diode to V_{SS} . If a negative ESD transient is applied to the input, the shunt zener diode and ESD protection diode in the IC will share the current. A little resistance between the zener

diode and IC input will force most transient current to flow through the zener diode instead of sharing it with the IC. Current flow through the substrate of the IC is very likely to cause an upset condition in the IC, so removing that possibility is a big help.

Another design approach to enhance performance is to implement a reset strategy that does not always upset the information displayed to the user. If critical data is maintained even with a reset, an upset due to an ESD event may not cause any significant disruption to the user. This strategy may employ redundant copies of critical information or checksum values that may be used to determine if the critical data is still useful after a device reset.

VIII. PACK INSERTION ISSUES

Some designs have communication and/or interface signal lines to circuitry in the battery pack. In many cases the ESD protection on these lines does not clamp a positive transient to less than the V_{CC} of the battery electronics. If the circuitry in the battery pack contains a substrate diode from the communication line to V_{CC} , it is possible to disrupt the V_{CC} supply when plugging in the battery pack. This disruption may cause improper operation of the battery-pack electronics. If the host system is not applying a charging potential to the host-side pack connector, the capacitance across the battery connections will be discharged before the battery pack is inserted. Most battery connectors do not have any provision to insure that the Pack- or ground connector pin mates first. If the Pack- pin connects last when the battery pack is plugged in, there is a path to pull up the V_{CC} in the battery electronics temporarily until it almost reaches the Pack+ terminal potential. The electrical path to pull up the battery pack V_{CC} passes through the host capacitance from Pack+ to Pack-, through a substrate diode in the host interface driver from V_{SS} to the communication or interface line, and through a substrate diode from this line to V_{CC} in the battery-pack circuitry. The complete path is shown in Fig. 6. The best design practice is to use circuitry in the battery pack that does not have an internal substrate diode to V_{CC} . This has a side benefit of preventing the battery-pack electronics from

being able to clamp the communication line to a low V_{CC} value resulting from a depleted battery. The ESD protection circuitry on the communication line should also clamp the voltage on the line to less than the maximum allowable voltage. This will limit the peak transient voltage and prevent damage to the battery electronics if the ground pin makes the last connection during pack insertion.

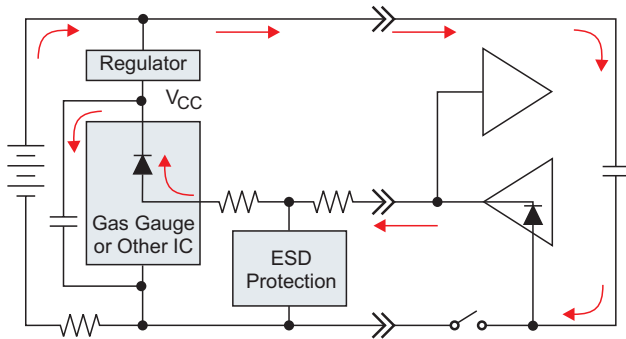


Fig. 6. Pack insertion issue when ground pin makes last connection.

IX. CONCLUSION

Battery-circuit design and layout are considerably more critical than might be expected. The combination of battery requirements includes: high-amplitude ESD to connector pins and exposed surfaces, coupling from an ESD event to nearby etch and components, heavy load currents, plugging and unplugging with power on the connector pins, multiple circuit ground references including high-current grounds, measurement of very small signals, and thermal management. Meeting these requirements and implementing the design on a circuit board that may be almost too small to hold the required components provides an extremely difficult challenge. The key to a successful design is the recognition of the various issues prior to starting the design and a close control of the PCB layout by the design engineer. A good design is a layered approach; removing any one layer will reduce the effectiveness of the others.

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