Section 3

Useful Things to Know about
High-Speed A/D Converters

Agenda

◆ Understanding the ADC Input
◆ Working with the ADC Input
◆ ADC References
◆ Clock Considerations
◆ ADC's Digital Data Outputs

Appendix:

• HS-ADC Testing

  - Bench Test Setup and Equipment

• Pipeline Architecture, Basic Overview

Today's High-Speed A/D converter feature a wide dynamic range at very high sampling rates. In order to preserve and utilize this wide dynamic range, careful attention must be given to the details of applying the A/D converter. The designer will find a lot of useful application information and circuit suggestions in the product data sheets. While the datasheets focus on model specific information, however, it typically does not go into the details that would help particularly the inexperienced designer to gain a fundamental understanding of high-speed A/D converter. This section of the seminar is designed to review some of the relevant fundamentals in and around High-Speed Pipeline ADCs.

High-Speed A/D Converter

◆ Sampling rate, Fs >10Msps
◆ Almost always 'Pipeline' ADCs
◆ Monolithic CMOS Devices
◆ Single-Supply (analog, digital)
◆ Integrated S&H -> ADS
◆ Internal Reference
◆ Low-Voltage, Single-Ended Logic Outputs (LVCMOS, typ. +3.3V, +1.8V)
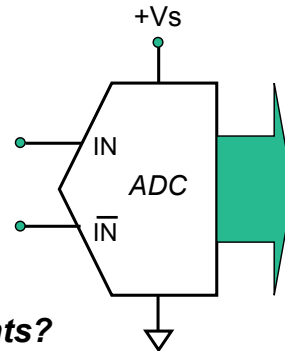◆ Emphasis on Dynamic Performance

The term 'High-Speed' can be found in combination with a lot of different product lines. For this presentation it is used for A/D converter with a sampling or clock rate of more than 10Msps. Such converter are in most cases based on the 'pipeline' architecture (see Appendix for more details on the principals of Pipeline ADCs), and fabricated using a sub-micron CMOS process. Some converter model designed for very-low power consumption operate on only 1.8V supplies, a result of a 0.18um process used. Most such ADCs are single-supply components, which poses certain restrictions on their operating conditions, a topic that will be looked at throughout this presentation. Based on switched capacitor techniques, High-Speed ADCs typically have a build-in Sample&Hold circuit, as well as internal references. The use of external reference is in most cases an available option. The supplies of the converter is usually such that it provides a dedicated output driver supply pin. This allows the digital outputs to be interfaced to a variety of logic families. Most High-Speed A/D converter are designed to achieve a certain, high level of dynamic performance, i.e. in terms of SFDR and SNR. It should be noted that in order to meet those ac-performances dc accuracy is typically compromised. For example, gain and offset error are often in the percent range.

Understanding the ADC Input

Understanding the ADC Input

What's the nature of the inputs?

◆ Differential Inputs

◆ Looking into a S&H

◆ Switched Cap Inputs

◆ Dynamic Input Impedance

◆ Effectively 'Capacitive' Load

What are the ac and dc constraints?

◆ Full-Scale Input Range (FSR in Vp-p)

◆ DC-Input Common-mode Voltage (V_{CM})

◆ Analog Input Bandwidth

Typically, a particular high-speed ADC model is selected based on its sampling speed and dynamic performance at certain frequencies or over a bandwidth of interest. For the system designer this selection process is not always easy. Often the system requirements are unique and the relevant information can not directly be extracted from the product datasheet Extrapolating the achievable performance bears some risk and to minimize the possible error sources the designer must pay careful attention to the issue of the 'interface'. The considerations on the interface include an understanding of the input of the ADC – what effect it will have on the driving source and it's constraints.

The signal inputs to the ADC are typically differential, which has a number of advantages, and will be discussed throughout the presentations. What the driving source sees is the input stage Sample&Hold amplifier, who's architecture employs switched capacitors. Here, switches are typically connected directly to the input pins and switching transients occur as a function of the clock. Consequently, the input impedance is neither constant nor just resistive, but dynamic and highly capacitive in nature.

The full-scale input range of the ADC is usually determined by the internal references. Note that there will be a significant difference in the required signal amplitude between differential and single-ended input configurations; typically a factor of two. In either case, most high-speed ADCs require their inputs to be biased up to a defined common-mode voltage. It is usually around half the supply voltage, and can be adjusted within a range without too much trade-off in performance.

One other consideration that comes into play particularly for undersampling or IF-sampling applications is the 'Analog Input Bandwidth' of the ADC.

ADC – Differential Input

Differential/Complementary Inputs

◆ Two Input Signals, Complementary
◆ ½ Signal Swing compared to SE
◆ Reduces Even-Order Harmonics, compared to SE
◆ Improves Common-Mode Noise Rejection
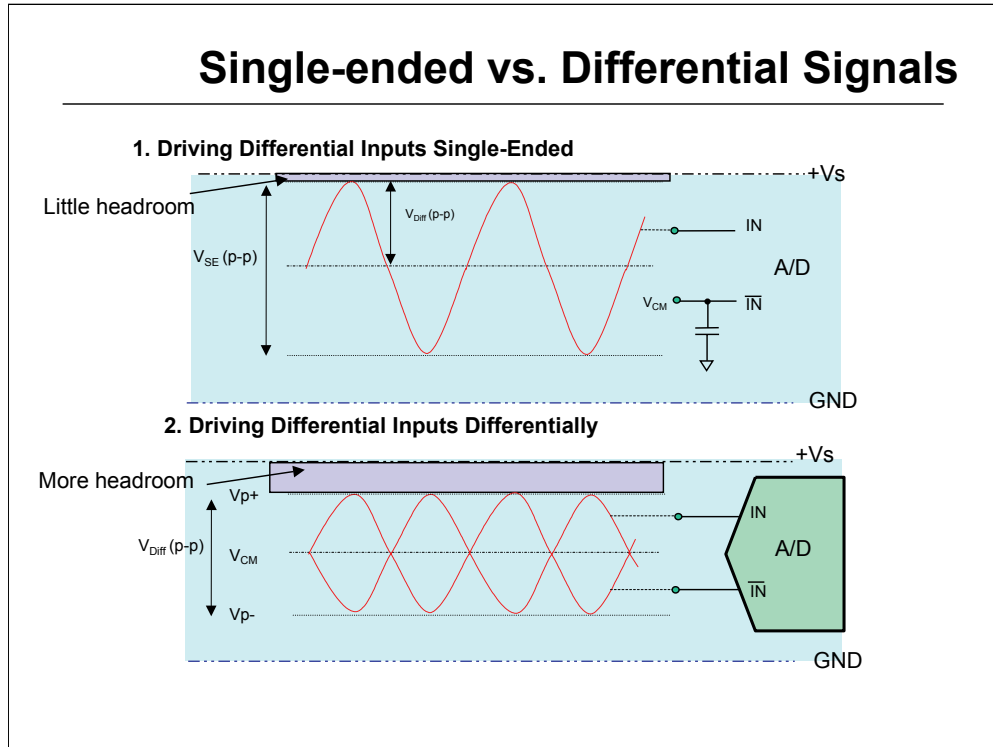◆ Full-Scale Input Range:
  • Typically 2Vp-p span for best Distortion and Noise trade-off
  • Can include Rail-to-Rail Operation

Directly Affects Requirements for Driver Circuit

Interfacing the input signal differentially to the high-speed ADCs is usually the recommended configuration as it leads to the highest achievable dynamic performance. Most ADCs are specified based on the differential input configuration.

Compared to single-ended, differential inputs require two signals that are 180degrees out of phase, but each of the two signal requires only half the signal amplitude. This is essential as it typically translates into reduced distortion from the driving source. Differential signaling also leads to a significant reduction in even-order harmonics. This is desirable since the second harmonic is often dominant and higher order harmonics can be filtered more easily. Furthermore, common-mode noise can be greatly suppressed.

Most high-speed ADCs designed for 3V to 5V power supplies operate with a full-scale input range of about 2Vp-p. This typically represents a good compromise between the achievable signal-to-noise ratio (SNR), and the distortion performance (THD, SFDR). Depending on the application, optimizations towards one or the other can be made, but will also affect the requirements for the driver circuit.

Single-ended vs. Differential Signals

1. Driving Differential Inputs Single-Ended

Little headroom

V_{Diff} (p-p)

V_{SE} (p-p)

V_{CM}

+Vs

IN

A/D

$\overline{IN}$

GND

2. Driving Differential Inputs Differentially

More headroom

Vp+

V_{Diff} (p-p)

V_{CM}

Vp-

+Vs

IN

A/D

$\overline{IN}$

GND

This slide shows the difference in required input signal amplitude between the single-ended input configuration and the differential input configuration. It also shows very clearly that for a given supply rail (+Vs) the differential signaling approach leaves significantly more headroom – the distance between the peak signal amplitude and the supply rail. Typically, as the signal amplitude approaches the supply rail distortion from the driving source, as well as the ADC, increases.

**Single-ended vs. Differential
Interface Tradeoffs**

◆ *Single-ended Inputs*

- Degraded dynamic performance (larger FSR)
- Common-mode voltage and op amp headroom may limit use for dc-coupling
- May be best suited for Time Domain application

◆ *Differential*

- Optimized performance due to lower FSR, Reduction of even-order and common-mode components
- Best for higher input frequencies (IFs)
- More complex driver circuitry

This slide summarizes the key points between a single-ended and differential interface. Even though the single-ended configuration has a number of draw backs it is still a viable option for time domain based applications. For example, for a CCD imaging system the emphasis is clearly on maximizing the signal-to-noise ratio and the increase in distortion that may result can be accepted. A related point is whether or not the system requires dc- or ac-coupling. Here, dc-coupling often places additional constraints on the interface circuit implementation.

For almost all high-speed A/D converter it can be said that in most applications, using the differential input configuration along with ac-coupling results in the best obtainable ADC performance.

Some general observations:

The distortion and SFDR performance typically improves with smaller signal amplitudes.

The SNR performance typically improves with larger signal amplitudes.

The distortion and SFDR performance typically degrades as the input frequency increases.

The SNR typically degrades as well with higher input frequencies. This is often primarily due to jitter having a higher impact. See the discussion on clock and jitter later in this presentation.

ADC – Input Common-Mode

Common-Mode Voltage Requirement

- ◆ Most A/D Converter use a Single-Supply
- ◆ Nominally at $V_{cm} = V_s/2$
- ◆ Requires the Analog Inputs to be Biased for Optimum Performance
- ◆ Possible to adjust V_{cm} within a certain Range while maintaining acceptable Performance
- ◆ Requires Attention in DC-coupled Applications
  - Matching V_{cm} Levels between Driver and ADC
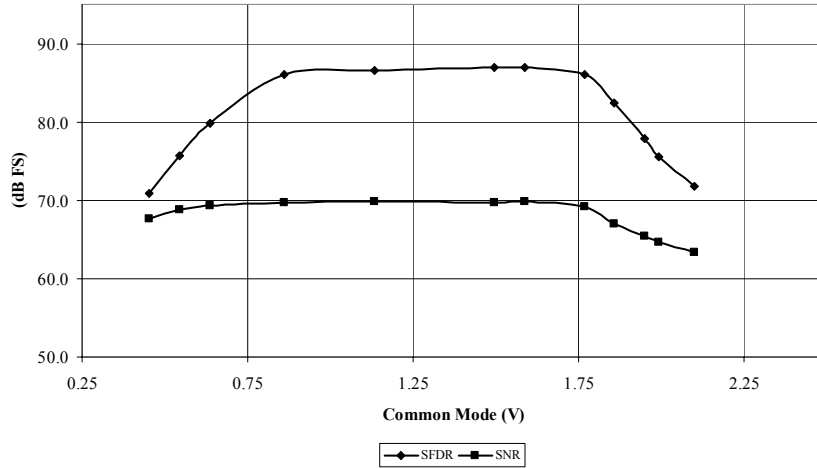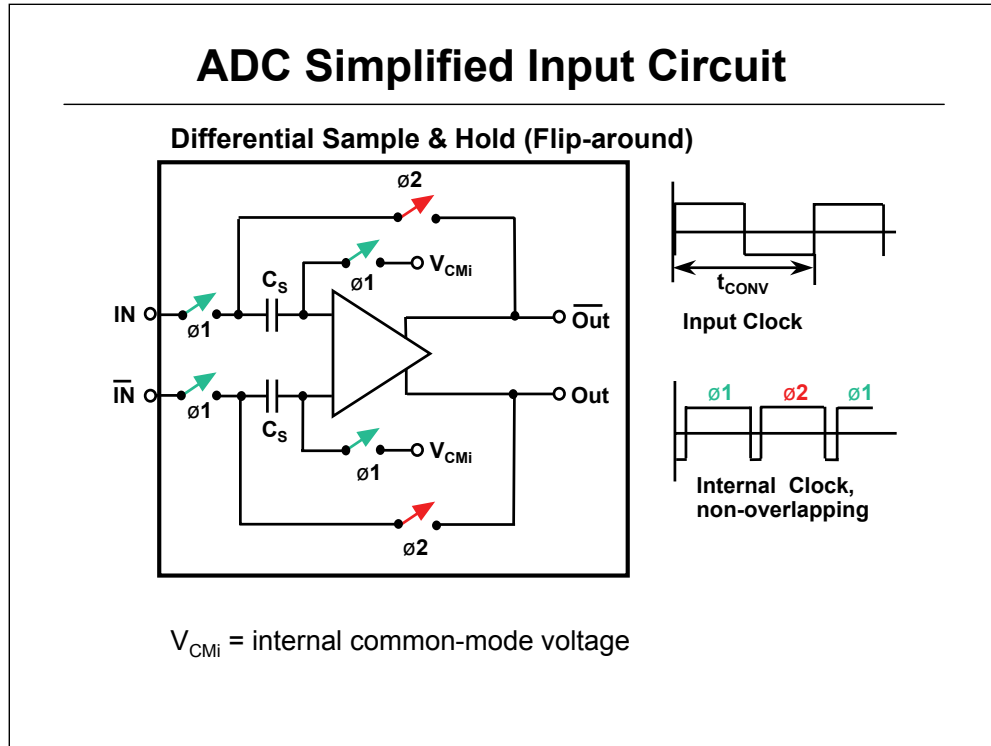 - Driver Headroom Issue

27

As mentioned before, one of the constraints that needs to be considered when designing with high-speed ADCs is the input common-mode voltage requirement.

The internal reference of the A/D converter often includes a pin for the common-mode voltage. This V_{cm} pin can be used to provide the input biasing to the ADC. For example, the V_{cm} pin may be tied directly to the center tap of a transformer. In any case, the V_{cm} pin requires local high-frequency bypassing to shunt any clock feed through to ground.
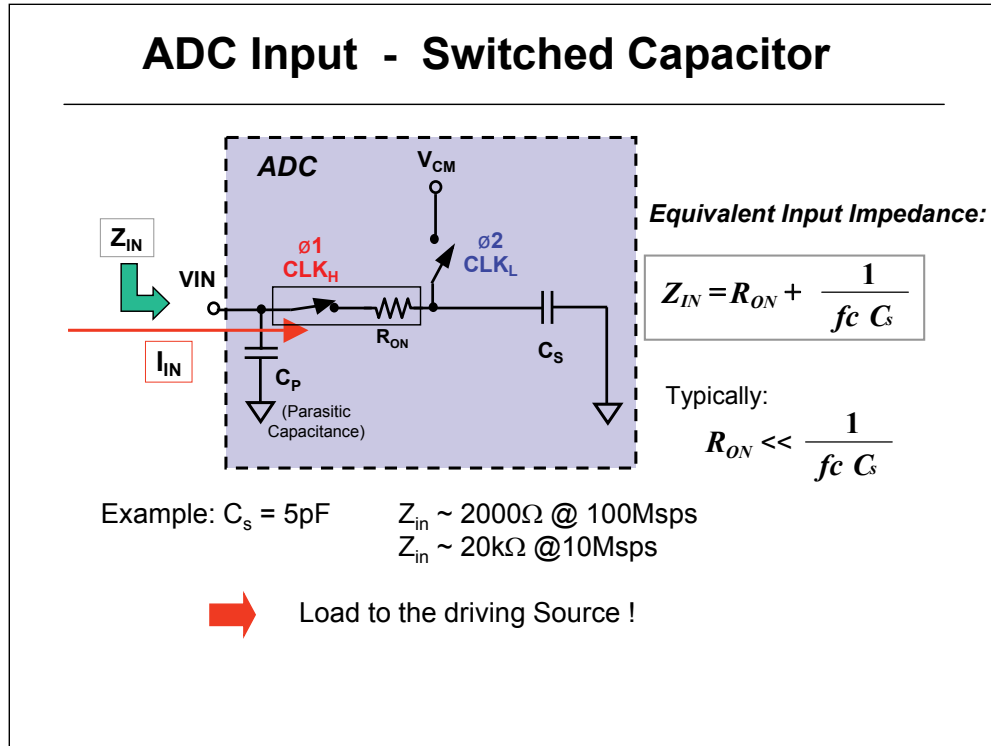
AC Performance vs Common-Mode Voltage

Example of an ADC's AC Performance over a range of
Input Common-Mode Voltage

ADC Simplified Input Circuit

Differential Sample & Hold (Flip-around)

V_{CMi} = internal common-mode voltage

Analog Input Sample & Hold Amplifier Circuit

The sample and hold amplifier is implemented using switched cap techniques. A simplified functional block diagram is shown here. The SHA is in sample mode when the clock is high and in hold mode when it is low. In sample mode the F 1 switches are closed and the differential input signal is sampled onto the capacitors Cs. As the CLK falling edge occurs, the F 1 switches are opened and the SHA is now placed into hold mode. The F 2 switches are subsequently closed, and the voltage across the sampling capacitors is then transferred to the output of the S/H amplifier.

ADC Input - Switched Capacitor

Equivalent Input Impedance:

$$Z_{IN} = R_{ON} + \frac{1}{fc\ C_s}$$

Typically:

$$R_{ON} << \frac{1}{fc\ C_s}$$

Example: C_s = 5pF Z_{in} ~ 2000Ω @ 100Msps
Z_{in} ~ 20kΩ @10Msps

Load to the driving Source !

Because the input to the sample and hold amplifier is a switched capacitor circuit, the input impedance is dynamic and dependent upon the sampling rate of the converter. The effective resistance of the dynamic load for each input is defined by the following equation.

Input Impedance: Z_{in} = 1 / (F_s * C_s)

Where C_s = Sampling Capacitor; F_s = Sampling clock frequency in Hz; Ron = ON resistance of MOS switch

Z_{in} : - High Static (no clock) Input Impedance, >1Mohm

- Dynamic Input Impedance Proportional to Sampling Clock

Small sampling capacitor values allow for very fast charging times, which corresponds to fast acquisition times. However, the trade-off here is the noise. The generated switching induced noise is equivalent to en= √kT/C_s. It can easily be seen that reducing the sampling capacitor value is reciprocally affecting the noise.

The components R_{on} and C_s also determine the ADCs 'Analog Input Bandwidth', a topic that will be discussed later in this seminar.

The time averaged charging of the sampling capacitor will cause a net dc current to flow into the ADC's input. The magnitude of this current changes depending on the clock frequency. Current (I_{in}) inrush to charge C_s to V_{in}. Q = C_s * ($V_{in} - V_{cm}$)

The implementation of this transmission gate type switch typically includes the use of 'bootstrapping'. The purpose is to maintain a constant VGS on the transistors and linearize the voltage dependency of the on resistance. This will help minimizing the distortion generated. This is particularly critical for IF sampling applications. Another advantage is that the ADC's performance becomes less sensitive to the external common-mode voltage.

Driving the ADC Input

Input Driver Requirements

◆ Driver must charge or discharge ADC sampling cap to the new input voltage

◆ Settle to ½LSB in the sample period of $f_s/2$

◆ Differential Inputs require Symmetrical Settling

◆ Incomplete Settling may degrade SFDR performance

◆ Source Impedance looking back from the ADC should be low up to high frequencies
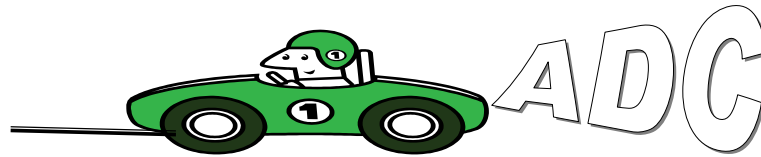
During the sampling phase (typically half the clock period) the driving source must charge or discharge the sampling capacitors to the new value. The condition encountered by the driver is a rapid change of its load and it must recover from this transient and settle to the new value. The worst case would be a full-scale excursion, but in most cases the input slew rate is significantly less. But even in this case the instantaneous demand of charging current could be challenging for a driver, e.g. an op amp, especially since the signal should be settled to within ½ LSB. Unsymmetrical or incomplete settling will result in an increase in distortion and reduction in the achievable SFDR performance. Ideally, the source impedance seen by the inputs of the high-speed ADC should be low and constant over a wide bandwidth.

Most ADC input driver configurations benefit from adding low value series resistors at the inputs of the ADC as well as shunt capacitors. Those simple components can be instrumental in achieving the listed requirements.

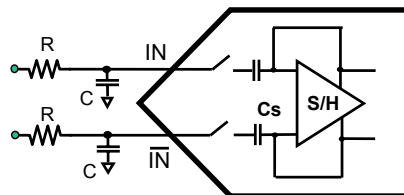# Driving the ADC Input – R & C

Optimizing Driver Performance

Insert Series Resistor, R

◆ Reduces peak transient current

◆ Decouples driver from capacitive ADC input
  (improves settling time due to reduced ringing)

Add Shunt Capacitor, C

◆ Supplies/absorbs charge from internal Cs during
  sampling phase

◆ Shunts switching related current transients to ground

This slide describes the use and functions of the series resistors, R, and the shunt capacitors ,C. References to the resistors and capacitors as shown here can be found in most product datasheets as a means to optimize the performance of input driver configuration for pipeline ADC. While the values may be different their use is typically recommended for transformer based as well as amplifier based circuits.

Driving the ADC Input – R & C

◆ **Results in 1st order RC low-pass Filter**
- Limits Wideband Noise to the ADC
- Noise Bandwidth, NBW = $\pi/2$ x 1/(2 πRC)
- Higher Order LP/BP-Filter possible

◆ **Typical Values**
- R: 10 to 100ohm typ.
- C: 1 to 100pF typ

◆ **Values should be optimized based on**
- Input Frequency and Sampling Rate (ADC model)
- Application; Time-Domain, Frequency-Domain
- ADC and OPA Datasheet Recommendations

The R and C together form a simple real-pole low-pass filter. Placing this pole at about 10 times the highest frequency of interest ensures that it has no adverse affect on the signal and driving source. For example, at the pole frequency the amplifier sees a load equal to v2 R. With the resistor value being as low as 10ohm, the amplifier output would be heavily loaded resulting in a significant increase in distortion.

Noise Bandwidth refers to a brick-wall filter frequency response. To account for the difference in the -3dB bandwidth of this first-order RC filter (BW=1/(2πRC)) and the Noise Bandwidth a factor of π/2 is used.

Optimizing the ADC Interface

Observations:

◆ Increasing R and/or C

- improves SNR, due to lower f_{-3dB} point of RC-LP
- reduces SFDR, due to longer settling time
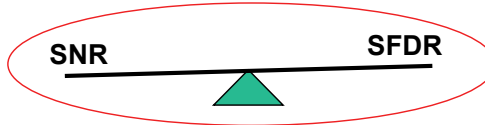
➢ Note:

- R's have 1% tolerance typ.
- C's have 10% tolerance typ.

Trying to optimize the interface circuit including the adjustments of the R and C values the designer should be aware of their effects and the resulting constraints. Generally, the values can only be changed within a certain range before the ADC's performance is negatively impacted. Also, choosing component values that seem to improve the SNR may carry a penalty on the distortion and SFDR performance, and visa versa. In the context of differential signaling attention should be paid to the component tolerances as it may lead to unsymmetrical settling times.

Driving the ADC Input

RC Input Filter
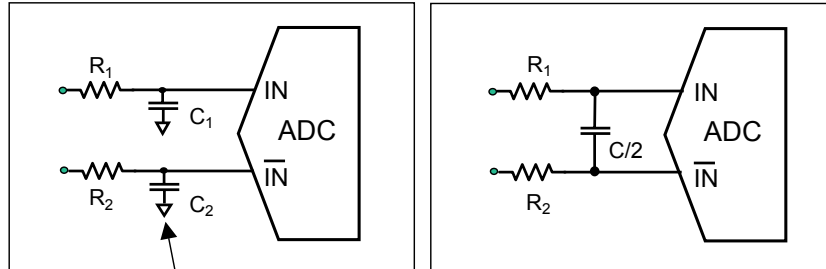
Critical ground node – view as 'signal input' during pcb layout

Important Considerations:
- Match RC time constants ($R_1C_1=R_2C_2$) for optimal differential signaling
- Match pc-board trace length

In addition to selecting the right values of R_s and C_s for the chosen ADC model and application, their configuration might be of importance as well. Shown here are the two common configurations one can also find in the product datasheets. While the circuit on the right uses two shunt capacitor in a single-ended configuration the left-hand circuit example employs only one capacitor placed across the inputs of the ADC. At the same time its value is reduced by half to maintain the same time constant.

Designers considering to use the left-hand implementation should pay close attention to the ground connection of the two shunt capacitors. If their ground is noisy or carries other interferences such signals can be directly coupled into the signal path resulting in reduced performance (e.g. higher noise). Both capacitors should be grounded to the same low-noise ground point such that any frequency coupled in occurs as a common-mode signal and can be suppressed by the ADCs common-mode rejection.

Working with the ADC Input

ADC – Analog Input Bandwidth

Common Definition:

◆ The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Alternative Definition:

◆ "Effective Resolution Bandwidth", (ERB)

◆ The analog input frequency at which the ENOB (SINAD) is reduced by 0.5Bit (3dB), based on an FFT.

Analog Input Bandwidth definition as it is used on high-speed ADCs:

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB. Depending on the manufacturer the Analog Input Bandwidth may be based on a small-signal or full-scale input amplitude. Consequently, the specified numbers can vary widely. In this context the Analog Input Bandwidth of the ADC is mainly determined by the Ron-resistance of the input switch and the size of the sampling capacitor.

It should be noted that the Analog Input Bandwidth is a rather theoretical number because it does not describe how well the ADC maintains its ac-performance. SFDR, SNR, THD and ENOB performance curves should be analyzed to determine the ac performance.

An alternative definition of the Analog Input Bandwidth that is based on the ADCs decline in performance is the 'Effective Resolution Bandwidth'.

ADC – Analog Input Bandwidth

- ◆ Large Signal vs Small Signal
- ◆ Input S&H of ADC determines the input bandwidth
- ◆ Full-Power Bandwidth is directly related to the Full-Scale Input Range of the ADC
- ◆ FPBW is a 'theoretical' number

Analog Input Bandwidth

The S&H performance of an ADC is the most significant function that determines the input bandwidth:

The slew-rate capability of the S&H determines the 'Full-power Bandwidth' (FPBW) for large signals, typically with the input amplitude set near full-scale (-1dBFS).

The frequency response of the S&H determines the small signal bandwidth for small signals. The input signal amplitude is significantly below FS, for example at -20dBFS.

Typically, when specifying the 'Analog Input Bandwidth' of an ADC, it is based on the Full-Power Bandwidth. It is directly related to the full-scale input range of the ADC and therefore can be used as an initial selection criteria when comparing converter for their undersampling capabilities.

ADC – Analog Input Bandwidth
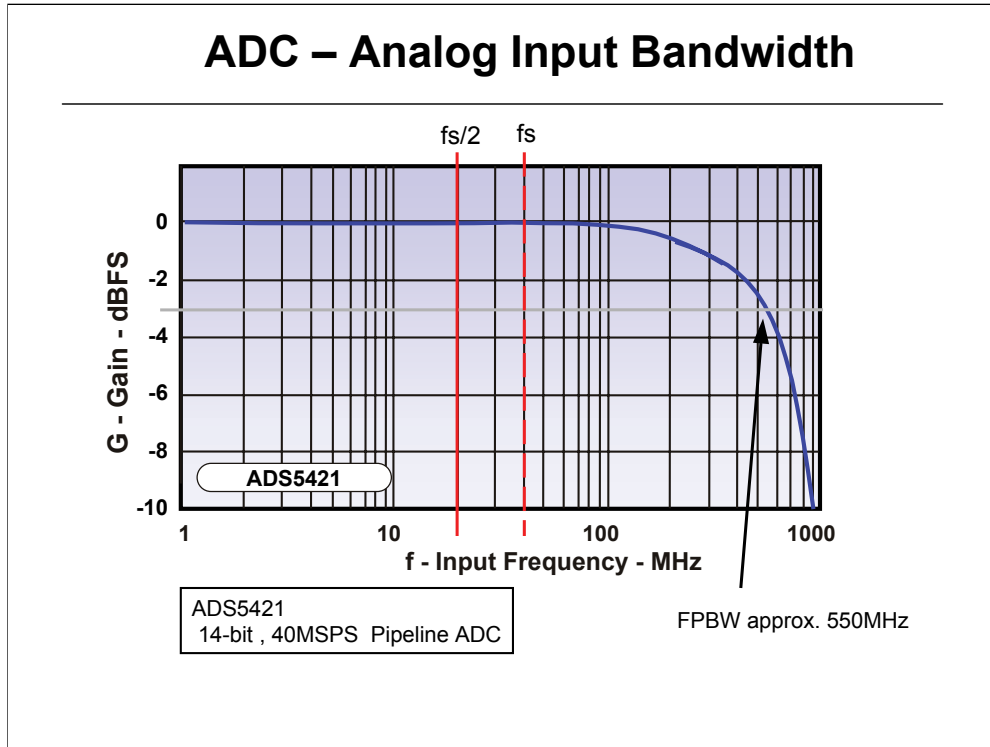
Shown here is the frequency response of the ADS5421, a 14-Bit, 40Msps pipeline A/D converter as an example of its 'Analog Input Bandwidth'. This CMOS converter uses a differential sample-and-hold circuit. The switched capacitor architecture allows for a very wide analog input bandwidth.

Also indicated by the red line markers are the Nyquist frequency at 20MHz, and the sampling frequency at 40MHz.

The information obtained out of such a bandwidth is that one can estimate the attenuation to the input signal based on the ADCs frequency response. For example, inputting a 200MHz signal into the ADS5421 would cause an attenuation of about 0.5dB.

Again, there is no indication on what the dynamic performance will be at this high input frequency. Specifying an 'Effective Resolution Bandwidth' would make this connection.
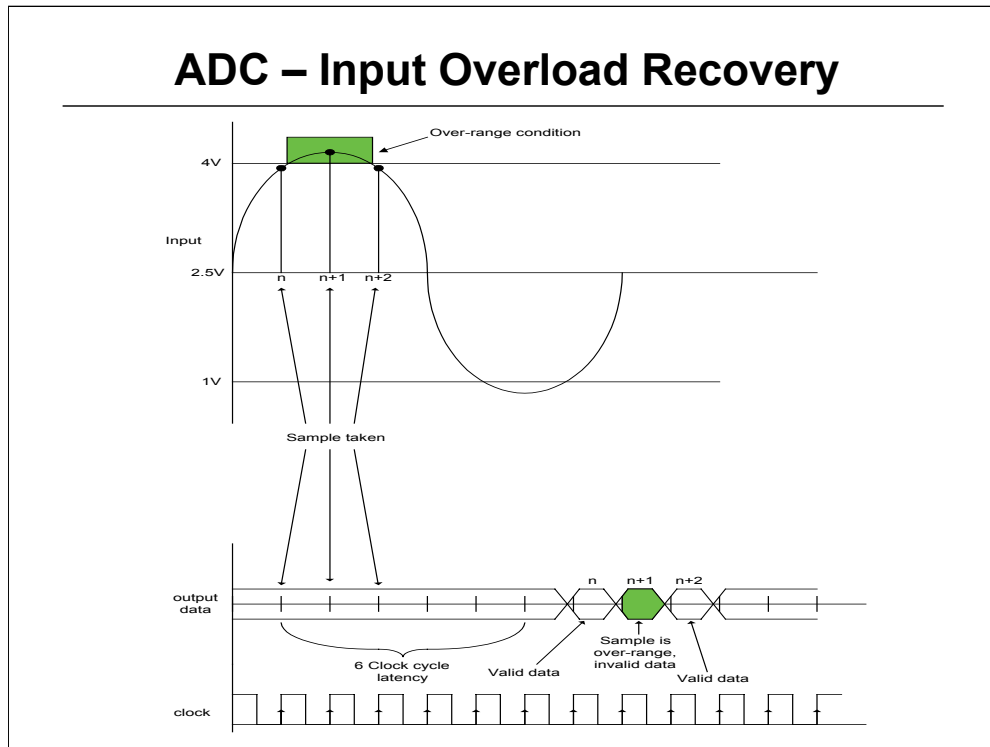
OVERVOLTAGE RECOVERY TIME

There is no one condition, except that the signal amplitude must stay below the supply voltage. If the ADC has internal ESD diodes on its inputs they may start to conduct. For most CMOS based design this is usually 0.3V above and below the supply rails. If the input voltage exceeds the full-scale range of the ADC the input capacitors of the input S&H are still being charged to reflect that value. Assuming now, the overload condition instantly disappears, within one clock cycle the charge on the input caps will be removed and biased back to a normal value. It will take as many pipeline delays as the converter has until valid data is available on the data outputs. In this example it will take 6 clock cycles.

ADC – Input Overload Recovery

Two cases:

◆ **Vinput < Vsupply**

Peak input voltage exceeds specified full-scale ADC input range, but remains within the supply rails:

- ADC output at all '1' or '0' during overload
- Once overload condition removed, ADC acquires new valid sample with the next clock cycle

◆ **Vinput > Vsupply**

Peak input voltage exceeds the supply rail(s):

- ADC output at all '1' or '0' during overload
- Internal ESD diodes may conduct and short circuit signal

DC-coupled input configuration:

- Possible excessive current flow
- Possibility of damage – need to add external protection, e.g. R's and diodes, or Voltage Limiting Amplifier (e.g.OPA698)

When the input voltage at any pin exceeds the power supplies (that is, V_{IN} < AGND or V_{IN} > VA or VD), the current at that pin should be limited to less than 10mA.

ADC References

High-Speed ADC References

◆ *Internal References*

- Typically designed to meet ac specs
- Not a 'precision', low-drift Reference
- Limited drive capability
- Inherently good matching for multi-channel ADCs, e.g. octal ADS5121

◆ *External References*

- May be used to improve gain matching between devices
- Typically complex circuit
  - Needs high-speed properties
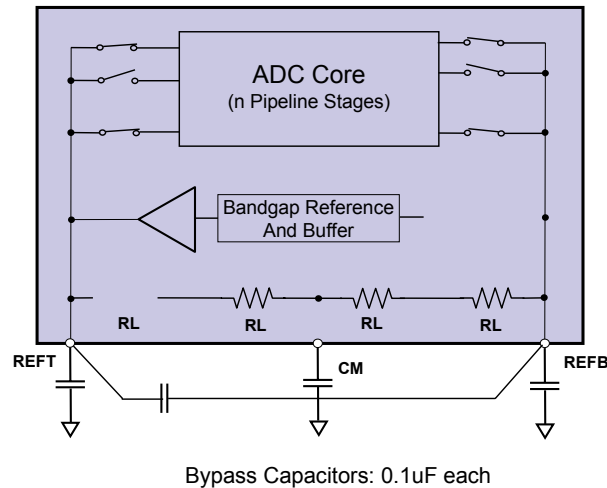 - Drive capability and Cload stability
  - May not be tracking; Range, drifts

Often the specification around the internal references are scarce. In some cases the reference performance is included in the overall ADC specifications such as gain error, or gain error drift.

In other instances errors caused by the references are separated from the rest of the converter. For example, the ADC may have a gain error spec which is based on operating it in the external reference mode. In order to understand the total gain error one would have to combine the ADC error and the reference error.

In most cases the ADC and its reference form an entity designed primarily to achieve the ac-performance goals. DC precision is usually compromised. This might be a limitation especially for dc coupled time domain applications. The drift performance of the internal reference is typically moderate with around 20ppm/°C.

Also, the internal references are designed to accommodate the demands of the ADC core. There is usually very little drive capability left to supply any external circuitry. In most cases external buffer are required.

ADC - Reference Bypassing

ADC Core
(n Pipeline Stages)

Bandgap Reference
And Buffer

RL   RL   RL   RL

REFT   CM   REFB

Bypass Capacitors: 0.1uF each

Very Important !

- Switching Noise on Reference lines
- Need to be bypassed to maintain stable Reference Voltages
- Bypass close to the pins
- Use very low inductance caps

Once sampled the input signal is compared to the reference voltage all throughout the pipeline stages. The digital result of this comparison is based on the momentary ratio of the signal to the reference.

Typically, internal to the ADC a top (REFT) and a bottom (REFB) reference voltage is generated. Connected to those reference points are the many sample&hold stages of the pipeline ADC core with their many switches. As these switches open and close at the rate of the clock they generate charge injection and ultimately add to the converter's noise. In order to minimize the noise contribution of this clock feedthrough the reference pins require solid high-frequency bypassing. This is usually accomplished by placing ceramic capacitors as close to the pins as possible. The lead inductance of those capacitors should be minimized. Choosing surface mount components in a small size (i.e. 0603, 0402 size) yield typically the best results. Depending on the converter model the addition of low ESR tantalum capacitors may be recommended.

In addition to the bypass caps going to ground, a cap between the REFT and REFB pins may further improve the performance.

The reference ladder typically have an impedance ranging from several kohms down to 100ohm. This should be considered when opting for external reference operation. While the REFT and REFB nodes are in most cases buffered, the mid-point of the ladder, the Common-mode point (CM) is usually not. Using this CM pin for biasing any input driver circuits may be limited.

Clock Considerations

ADC Clock Considerations

Clock Quality a Major Factor for achieving high Dynamic Performance!

Very low Jitter required to maintain good SNR

• Especially at high Input Frequencies (IF)

$$SNR_j = 20\log \frac{1}{2\pi \times f_{IN} \times t_{aj}}$$

t_{aj} = rms aperture jitter
f_{IN} = Input Frequency

• Independent Jitter Sources sum by Root-Sum square

$$t_{ajtot} = \sqrt{(t_{ajADC}^2 + t_{ajExt}^2)} \qquad \text{[psrms]}$$

The degradation in SNR is dependent on the input frequency and the total aperture jitter.

Since jitter is a random occurrence and sources are typically not correlated they add by calculating the square-root of the sum of the squares.

The slew-rate (dv/dt) of undersampled IF input signals is very high. Consequently, the effect of clock jitter is pronounced and therefore requires special consideration.
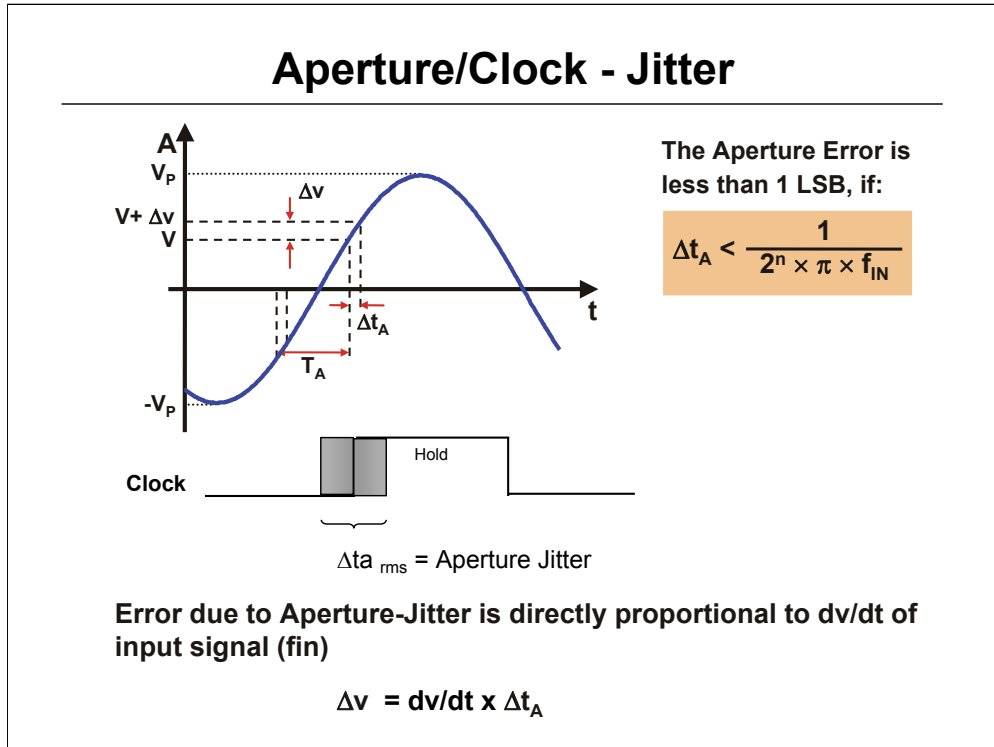
ADC Clock Considerations

Clock 'Quality'

◆ Use Differential Clock Signal
◆ Observe symmetry of Clock line and Impedances
◆ Fast rise/fall times
◆ Use 50% Duty Cycle at max. Sampling Rate
  • less important, if A/D operated below max. sampling rate
◆ Maintain Clock within the recommended range
  • Amplitude (Vp-p), and Common-Mode Level (V_{CM})
  • Use proper Termination Techniques to avoid Reflections
  • Avoid any Over- or Undershoot
◆ Use higher turns ratio for Transformer coupled Circuit to increase amplitude

Consider using logic circuits that have sufficiently fast rise and fall times (1ns) to minimize their contribution to the total jitter error.

If this option is available, the ADC's clock input should be driven differentially. Applying a single-ended clock to differential clock inputs may not yield the optimum performance due to asymmetric rsie and fall times that will also affect the duty cycle.
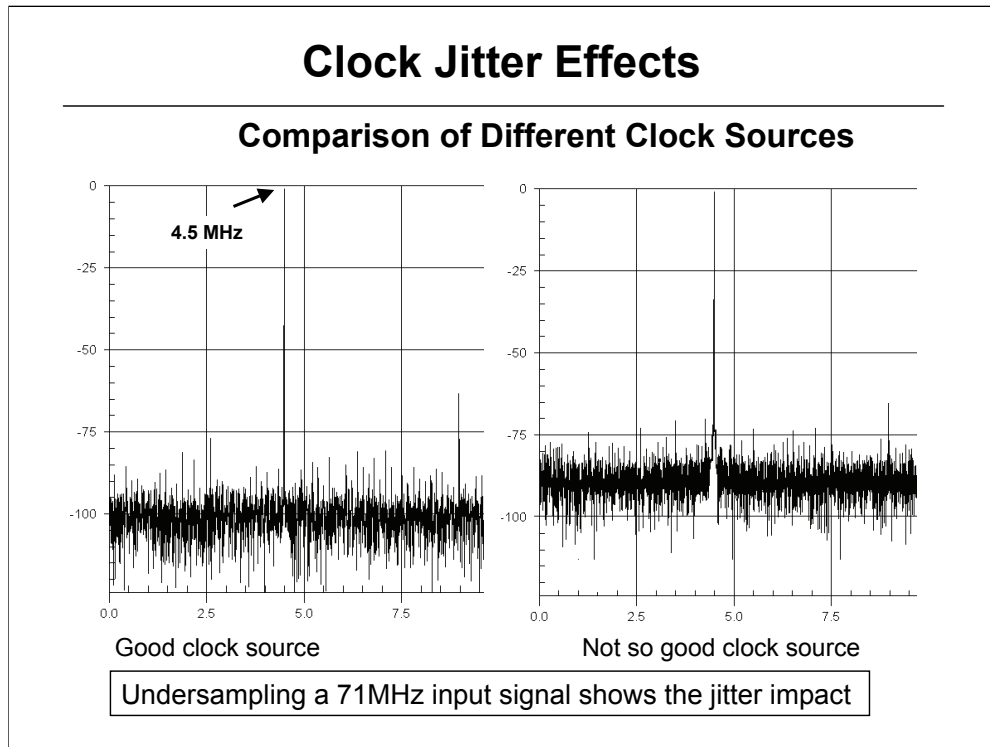
If the A/D converter is operated below its maximum sampling rate the duty cycle requirement for the converter clock may be relaxed, meaning it can vary from the ideal 50% point.

Aperture/Clock - Jitter

The Aperture Error is less than 1 LSB, if:

$$\Delta t_A < \frac{1}{2^n \times \pi \times f_{IN}}$$

Clock

Hold

Δta_{rms} = Aperture Jitter

Error due to Aperture-Jitter is directly proportional to dv/dt of input signal (fin)

$$\Delta v = dv/dt \times \Delta t_A$$

Jitter is the time domain representation of clock noise.

Aperture Jitter = The rms variation in the aperture delay due to random noise effects.

Aperture Delay = The time delay between the external sample command (typically the 50% point of the rising clock edge) and the time at which the signal is actually captured. Clock path propagation delays contribute (inside the IC) to aperture delay. Is usually considered a constant.

Clock Jitter Effects

Comparison of Different Clock Sources

Good clock source

Not so good clock source

Undersampling a 71MHz input signal shows the jitter impact

For this rather basic comparison the setup of the ADS5421 was used. The converter is digitizing at 37.75Msps with an input frequency of approx. 71MHz (-1dBFS). In this undersampling situation it becomes critical to understand the impact of the clock source's jitter performance. Since the jitter of the clock essentially translates into the achievable SNR a side-by-side comparison of the FFT plots makes it relatively simple to make a quantitative assessment by comparing the noise floor. As can be seen in this example, a good clock source, like the HP8644, results is a lower noise floor than a not so good clock source.

Also, the skirt on the fundamental exhibits a somewhat wider spread, indicating a reduced frequency resolution. The system uses coherent sampling and the clocks of the generators are phase locked together.

$F_s/2 = 18.88$ MHz

71

18.9   37.5   56.6   75.51

4.5 MHz
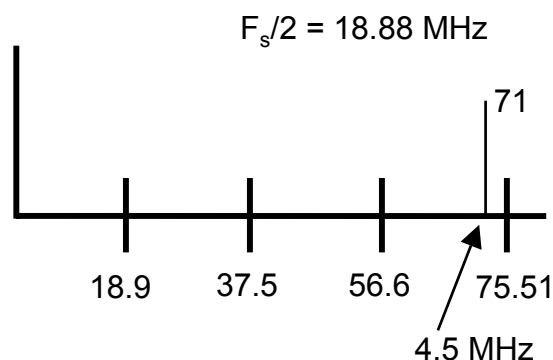
Notes on Clock & Jitter   1

◆ If the noise floor (SNR) appears to be higher than expected when evaluating a High-Speed ADC (FFT plot), check the jitter contribution of the clock source

◆ Typically, higher frequency crystal clocks (f_c>10MHz) have a low jitter of less than 10ps rms

◆ Lower frequency clocks usually have higher jitter

◆ Therefore, consider a higher F_c and divide down

Dividing a higher frequency clock can be beneficial, however each additional logic gate etc. can potentially add phase noise and may increase the total jitter. Therefore, division factors are usually limited to 8 or less. This also depends on the clock source and desired end frequency.

Notes on Clock & Jitter 2

◆ Clocks from FPGAs, uP, DSP etc., are usually not suitable for high-speed converter, especially not for undersampling applications

◆ Noise on the ADC power supply directly affects the internal clock circuitry and may lead to increased jitter

◆ Noise and spurs on the clock will be 'mixed' during sampling and lead to a decrease in dynamic range

◆ Many A/D converters now feature differential clock input designed for sine-, and square wave inputs

◆ Don't route clock line parallel to other signal lines

Clock signal may be band limited (BP filtered) to reduce existing spurs and noise before applying to the ADC.

Clock Input - Differential

Differential Clock Inputs:

◆ Accept low-level Sine Wave
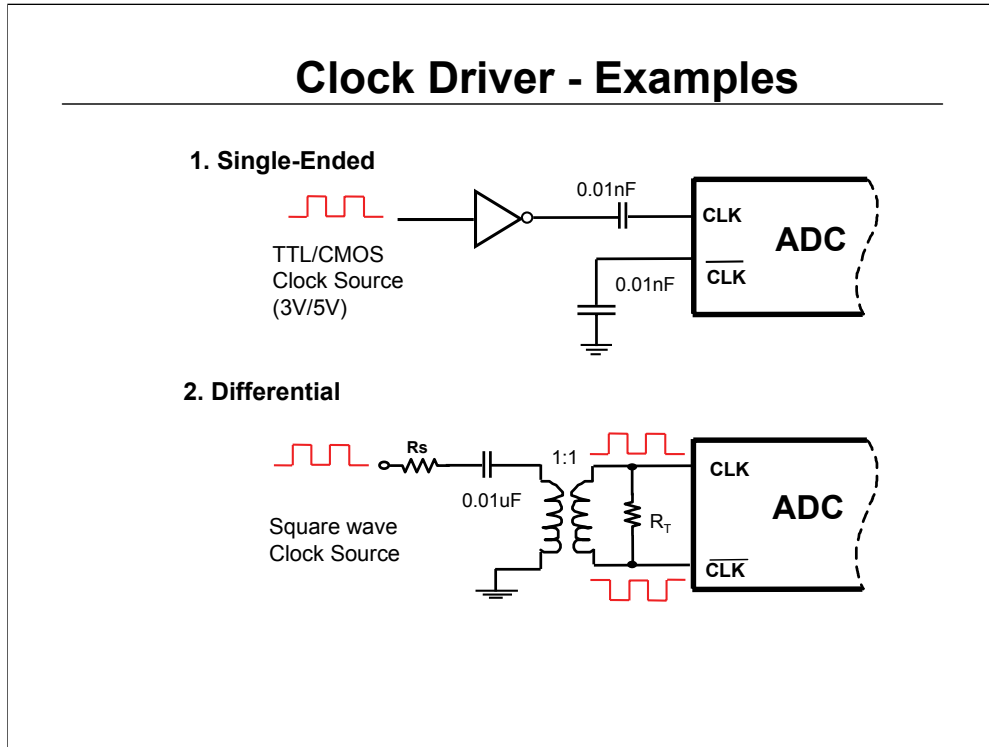
◆ Clock inputs are internally biased -? ac-coupling
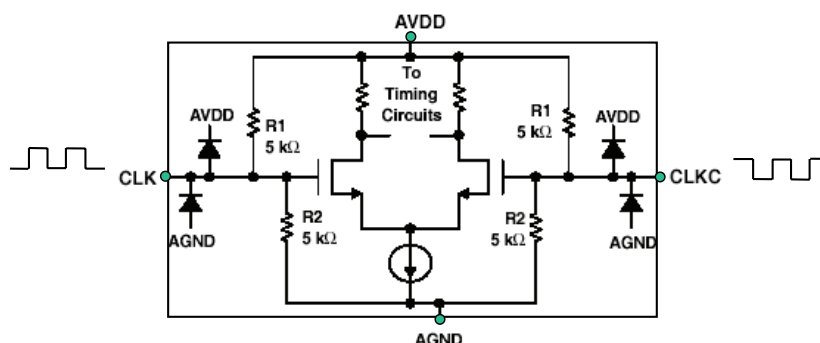
The majority of newer high-speed ADCs feature aside from the differential analog inputs also differential clock inputs, which offers certain advantages. For example, distributing the clock as a low level, differential sine wave helps minimizing the EMI of the system. The clock input circuitry of the A/D converter uses a high-gain amplifier stage to convert the sine wave into a square wave for internal distribution to the various circuit blocks. Noise coupling onto the differential clock line is a common-mode signal and will be rejected.

AC Performance vs Clock Common-Mode

Example of an ADC's AC Performance over a range of Clock Common-Mode Voltage (*ADS5413, 12-Bit, 65Msps*)
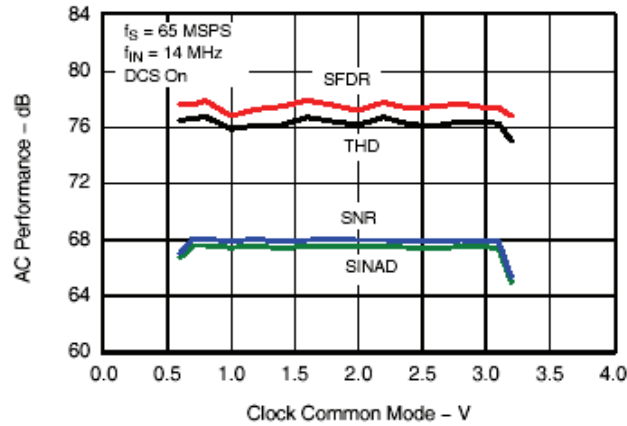

Again, in analogy to the signal inputs the clock inputs require a common-mode voltage or biasing as well. While in most cases internal resistors provide the bias and set the threshold the common-mode voltage can be adjusted within a certain range. Shown here in this performance is the dependency of the ADS5413's ac-performance on the applied clock common-mode voltage. DCS is the internal clock Duty Cycle Stabilizer.

Clock Driver - Examples

1. Single-Ended

TTL/CMOS
Clock Source
(3V/5V)

2. Differential

Square wave
Clock Source

In case the A/D converter has a differential clock interface it is usually still possible to run the converter directly from a single-ended clock source. Then the other unused clock pin typically requires to be ac-grounded. However, it is necessary to read the specific application recommendation from the manufacturer.

Clock Driver - Examples

Sine Wave to TTL Conversion, Differential
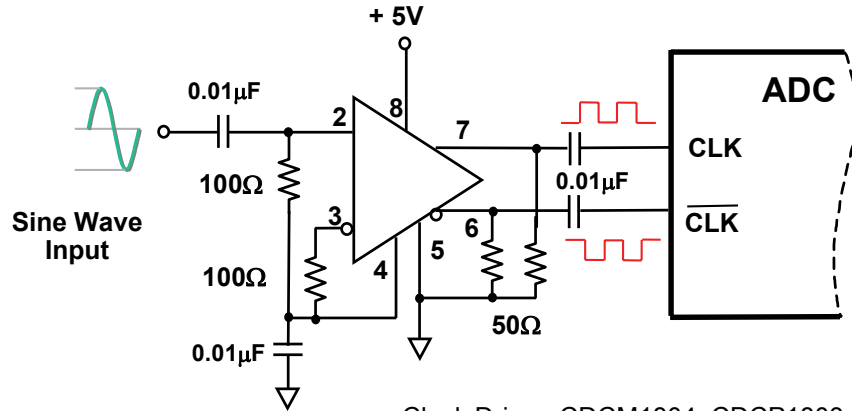
Clock Driver: CDCM1804, CDCP1803, CDC7005; or other PECL translator devices

---

Minimum Sampling Frequency

High-Speed Pipeline ADC

- ◆ Sampling Capacitor Values typically < 1pF
- ◆ Non-ideal Components
- ◆ Internal Leakage Current

⟹ Causes *Droop*

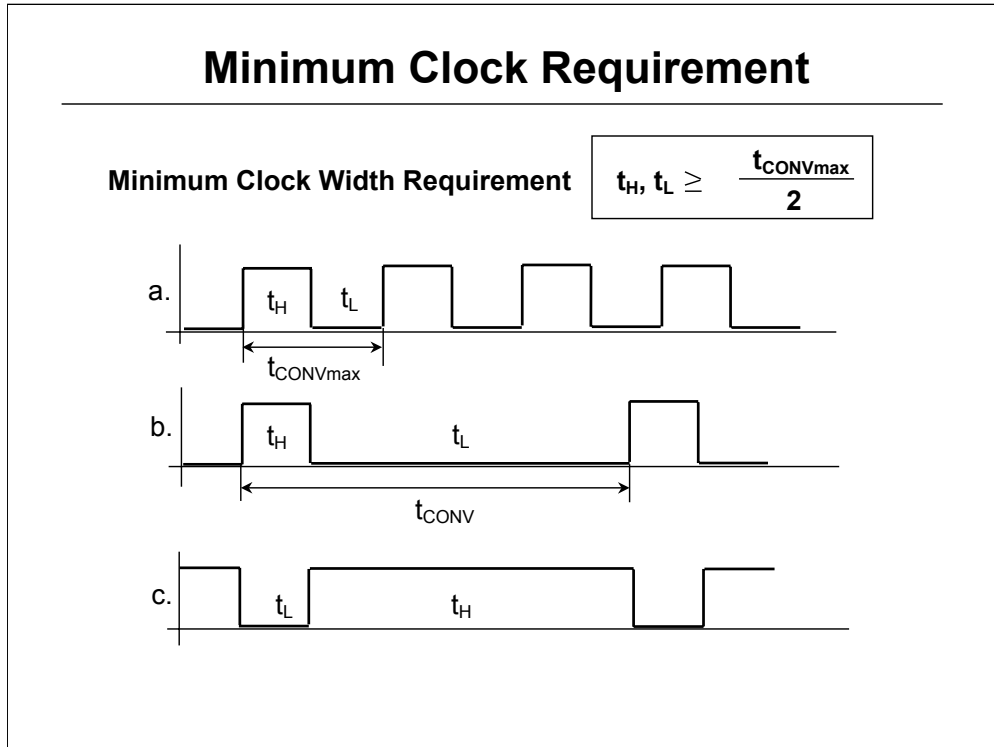Requires a Minimum Sampling Frequency to Move Signal Charge and 'Refresh' the Capacitors to a Defined Voltage (V_{CM}).

Datasheets of High-Speed Pipeline ADCs often specify a 'Minimum Sampling Frequency', and this frequently prompt the questions why that is and what happens if the clock frequency drops below the specified value. Back when the Sample&Hold stage had to be implemented with an external Sample&Hold amplifier one big concern was the droop rate, which is a functions of the Hold time and the capacitor size. The on-chip Sample&Hold circuit has just the same constraints. The size of the sampling capacitor is very small and internal leakage currents (charge) can affect the charge representing the actual sample. As the sampling frequency is reduced the hold time becomes longer and droop occurs.

Non-Continuous Clocking

Burst-Mode Operation possible on some ADCs

◆ Observe Minimum Clock Requirement for Uninterrupted, Continuous Sampling. Typically: fs_{min} >1MHz.

◆ Data in Pipeline may become Invalid if Clock is Stopped for a Longer than specified Time.

◆ Some ADCs may go into an automatic power-down mode if sampling rate drops below a certain limit

◆ Will not work with ADCs that have internal clock stabilizer, which is usually DLL based.

Operating the ADC within certain clock conditions is typically required in order to obtain the specified dynamic performance. One of those clock conditions is to deliver a 50% clock duty cycle to the converter, a requirement particularly important towards the maximum sampling rate. To ease this requirement for the systems designer, newer ADC model incorporate a clock duty cycle stabilizer circuit. Those circuits typically look at the sampling clock edge, e.g. the rising edge, as a reference and retime the non-sampling edge, providing an internal clock that maintains a fixed 50% duty cycle. The advantage is that it allows a wide range of clock input duty cycles without compromising the ADC's performance. Such duty cycle stabilizer typically use delay-locked loops (DLL). As a result, any change in the applied sampling rate requires the DLL to acquire and lock to the new rate, which can take up to several hundred clock cycles. For that reason such an ADC may not be the right choice for applications that require a fast response to instantaneous changes in the sampling rate.

Minimum Clock Requirement

Minimum Clock Width Requirement $\quad t_H, t_L \geq \dfrac{t_{CONVmax}}{2}$

While we discussed before the requirements for a certain duty cycle and maximum, or minimum sampling frequency it comes down to a 'Minimum Clock Pulse Width' requirement.

Shown in a) is the clock signal as it is required to run the ADC at its maximum sampling rate – with a duty cycle at or close to 50%.

When operating the ADC below the maximum sampling rate, the duty cycle may deviate from this requirement to the extent that the minimum clock pulse width is satisfied. Line b. shows the clock high time being the shortest, but no less than half the sampling rate. Line c. has the clock low time being short.

For example: for an ADC with a maximum sampling rate of 40Msps (Clock period = 25ns), the minimum ½ cycle width is 11.25ns.

ADS5413 Duty-Cycle Sensitivity
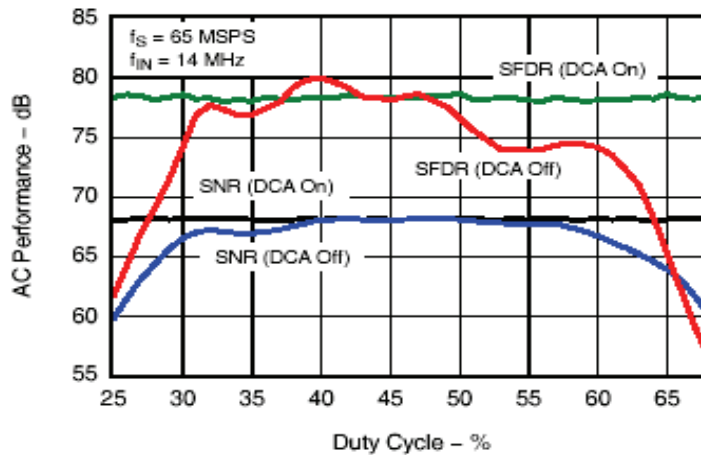
Shown here is the duty-cycle sensitivity of the ADS5413, a 12-Bit 65Msps Pipeline A/D converter. This particular model employs an internal clock duty-cycle stabilizer (DCA). While it's performance holds up fairly well with this stabilizer being inactive, it further improves the performance towards the extreme ends of the duty-cycle.

Power Consumption vs. Fclk

Supply Current (I) versus CLK
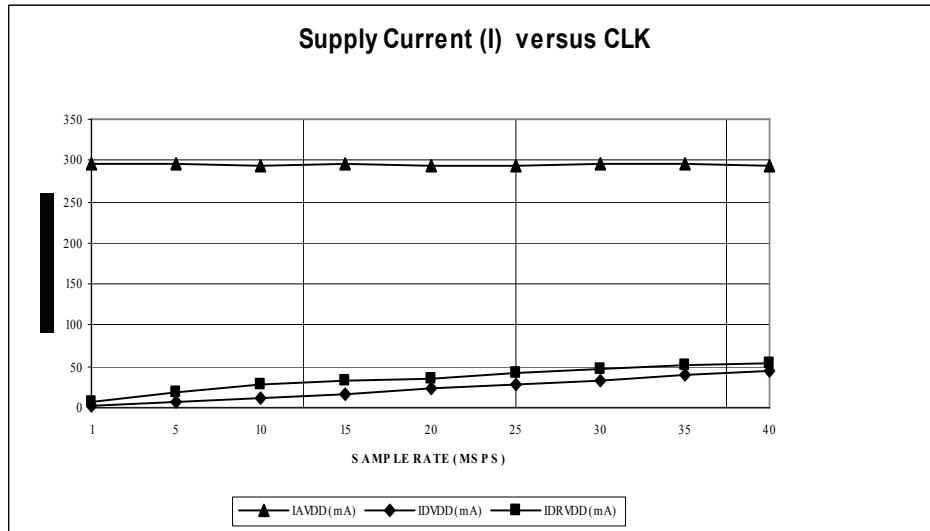
In general, the power consumption on (High-Speed) converters do not scale linearly, even though their CMOS nature may imply this. While 'scaling' is true for pure logic devices, converter are essentially 'analog' components. The internal circuits devices need biasing in order to achieve the maximum speed the converter is designed for. Therefore most of the supply current is a constant current and is not affected by the clock speed. On almost all of the high-speed converter, only about 20% to 30% of the total power consumption is affected by a change in the clock speed.

The shown curves are taken on the ADS5120, an eight-channel, 10-Bit, 40Msps Pipeline converter operating on a low 1.8V supply (3.3V output driver supply).
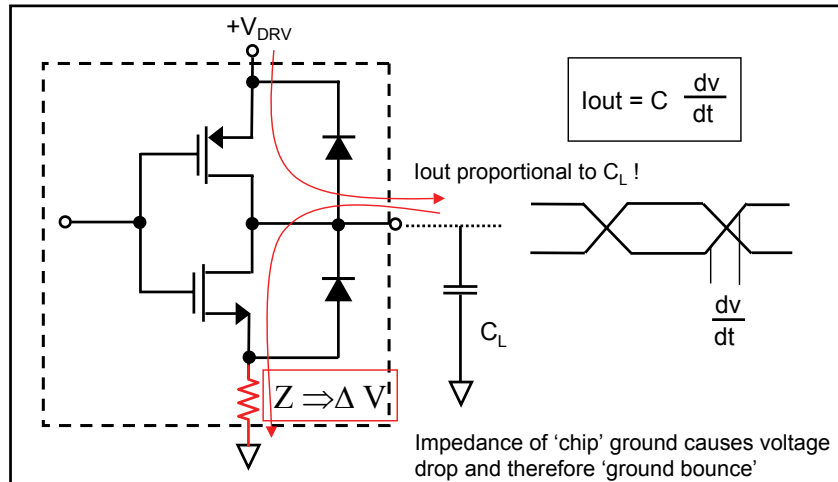
ADC's Digital Data Output

Digital Data Outputs of HS- ADCs

◆ Usually has only Limited Output Drive

- Typ. around 15mA per Output

- External Latches or Buffers Recommended

◆ Dedicated Output Driver Supply Pin (V_{DRV})

- Allows Flexible Interfacing to +5V/+3.3V/+1.8V Logic

- $I_{VDRV} = V_{DRV} \times f_{clk} \times C_L \times N$ (worst case)
  - C_L = load capacitance
  - N = number of data output pins

The maximum output driver current flows when all outputs are switching on every clock cycle, e.g. when a full-scale square wave signal is applied. While this is a rather theoretical case, the sampling rate along with the characteristics of the input signal will result in an average number of bits switching.

Digital Data Outputs of HS- ADCs

$$Iout = C \frac{dv}{dt}$$

Iout proportional to C_L !

C_L

$\frac{dv}{dt}$

$Z \Rightarrow \Delta V_i'$

Impedance of 'chip' ground causes voltage drop and therefore 'ground bounce'

$+V_{DRV}$

Shown here is the simplified model of an digital output driver within the ADC's output stage. Here the upper transistor will charge the load (capacitive, C_L) while drawing the current from the supply pin +VDRV. The lower transistor will be active for discharging the load capacitance. This charge will be conducted to the converter's ground (possibly the substrate), and due to it's finite resistance it may momentarily raise the ground potential. This could effectively add noise degrading the noise performance of the converter. When transitioning from logic 'L' to 'H' or 'H' to 'L', a high transient current flows through the output MOSFETs either from the +VDRV supply or to ground. This current depends on the capacitive loading (C_L), according to Iout = C dv/dt.

Therefore, a large capacitive load (parasitic) can create a large current to flow in the output stage and cause a current spike in the supplies.
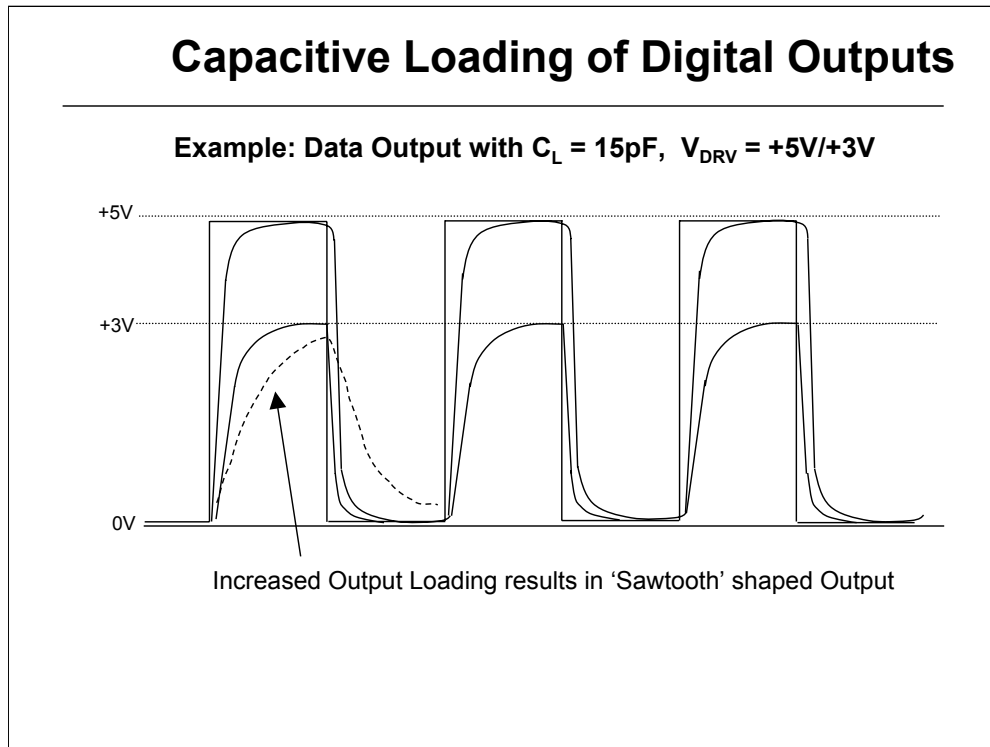
Digital Data Outputs of HS- ADCs

Capacitive Loading of Digital Outputs

◆ Limit capacitive loading to <15pF for each output pin

◆ Datasheet Specifications use 10pF total output loading:
        5pF - pcb parasitics
        5pF - input capacitance of one logic gate

◆ Typical output slew rate of logic gate is 0.8V/ns.

Example: 15pF x 0.8V/ns = 12mA

The current requirements for the output driver of the ADC is directly proportional to its capacitive loading. Hence the requirement for keeping the capacitive loading as low as possible. However, with a target of keeping the loading at one pin to less than 10 or 15pF, it is easy to accumulate this quickly.

Capacitive Loading of Digital Outputs

Example: Data Output with C_L = 15pF, V_{DRV} = +5V/+3V

Increased Output Loading results in 'Sawtooth' shaped Output

Excess capacitive loading will alter the time constant and could eventually prevent from the data capture window being sufficient. Or, the required threshold levels are no longer being crossed. It is often recommended to insert small series resistor between the ADC's data outputs and the following logic device. While this method can help avoiding possible over- and undershoot and limit the instantaneous current, a too high of a value can be detrimental.

What's New? …….LVDS!

Low Voltage Differential Signaling

- ◆ High-Speed, Low Power Data Transmission Standard
- ◆ Differential Output Swing is 350mVp-p (typ.)
- ◆ Current mode (I_{out} =3.5mA)
- ◆ 100Ω Differential Termination at Receiver
- ◆ V_{CM} =1.2V, V_H = 1.38V, V_L = 1.03V

ANSI/TIA/EIA-644 Standard

Only defines driver output and receiver input characteristics

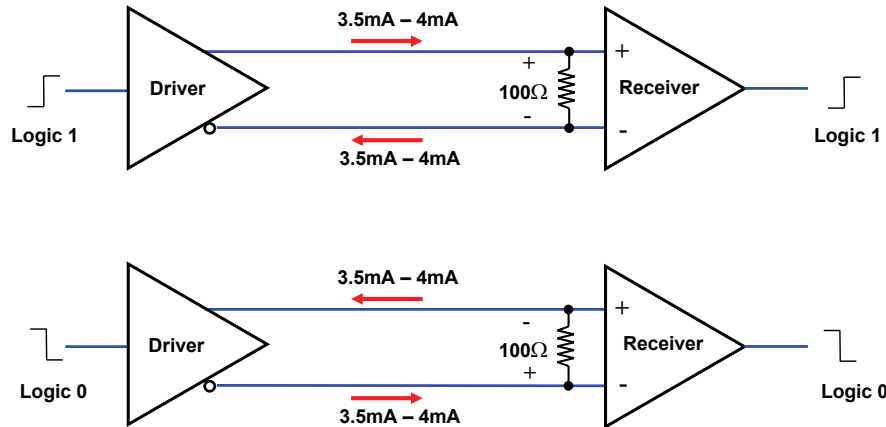Provides guidelines for bus configuration, cables and termination

Does not define protocol, connectors, and bus structure

Does not define a maximum data rate

Newer standard (ANSI/TIA/EIA-644-A): multiple receivers

Low Voltage Differential Signal (LVDS)

LVDS uses constant current, which makes it largely supply voltage independent

The LVDS interface operates in a current mode, with a typical current of 3.5mA.

LVDS Advantages

◆ Allows low noise/ low EMI system design

◆ It is supply independent
  ▪ Easy migration path to lower supply voltages

◆ Class A operation has low dI/dt noise

◆ Wide common mode range
  ▪ Better common-mode noise immunity.

Advantages compared to LVTTL, LVCMOS, or (P)ECL

Fewer pins for higher resolution

Reduced Signal Swing

Lower Noise Interface for Data Converter

Lower EMI

Higher Data Rates Possible

Lower Voltage Supplies

LVDS: Parallel vs. Serial

Parallel LVDS

Serialized LVDS

a) Non-Embedded Clock

b) Embedded Clock
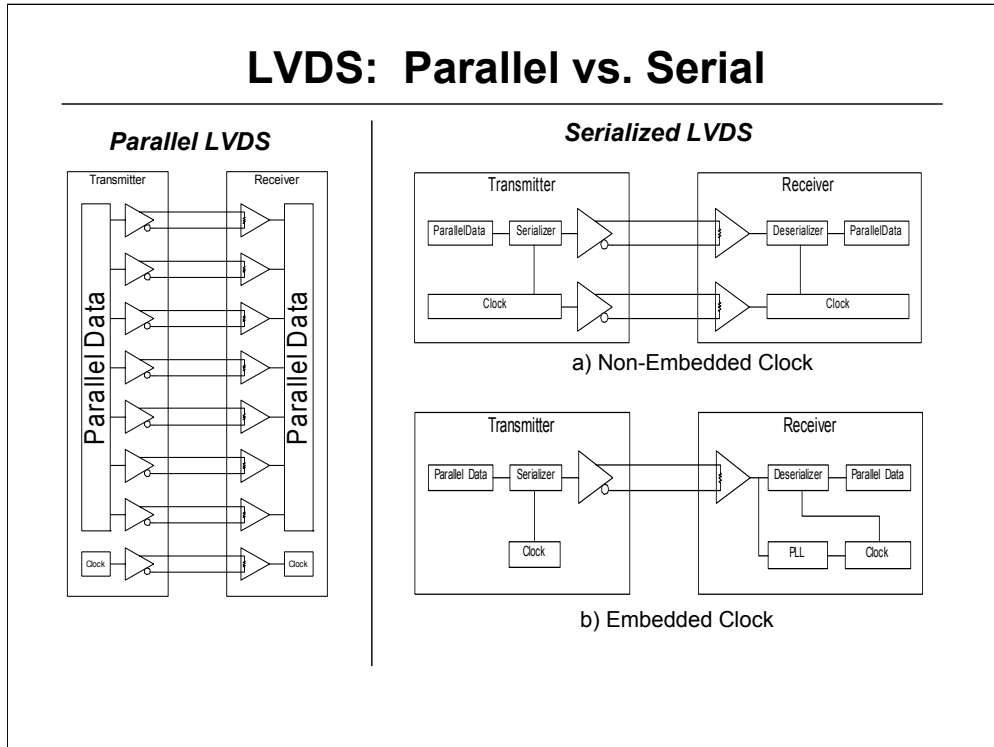
There a three possible implementations of an LVDS interface. The first is using LVDS for each data pin resulting in 'Parallel LVDS'. Compared to a single-ended CMOS interface this will double the number of interface lines between the transmitter and receiver. If a large number of channels is required this could become a severe restriction. Here, implementing a serial LVDS interface would reduce the number of required lines significantly. Serialized LVDS interfaces can come in two types: one is the 'non-embedded clock', the other uses an embedded clock.

Serialized LVDS - Formats

Non-Embedded Clock

◆ No special data format
◆ No PLL needed in receiver to recover data
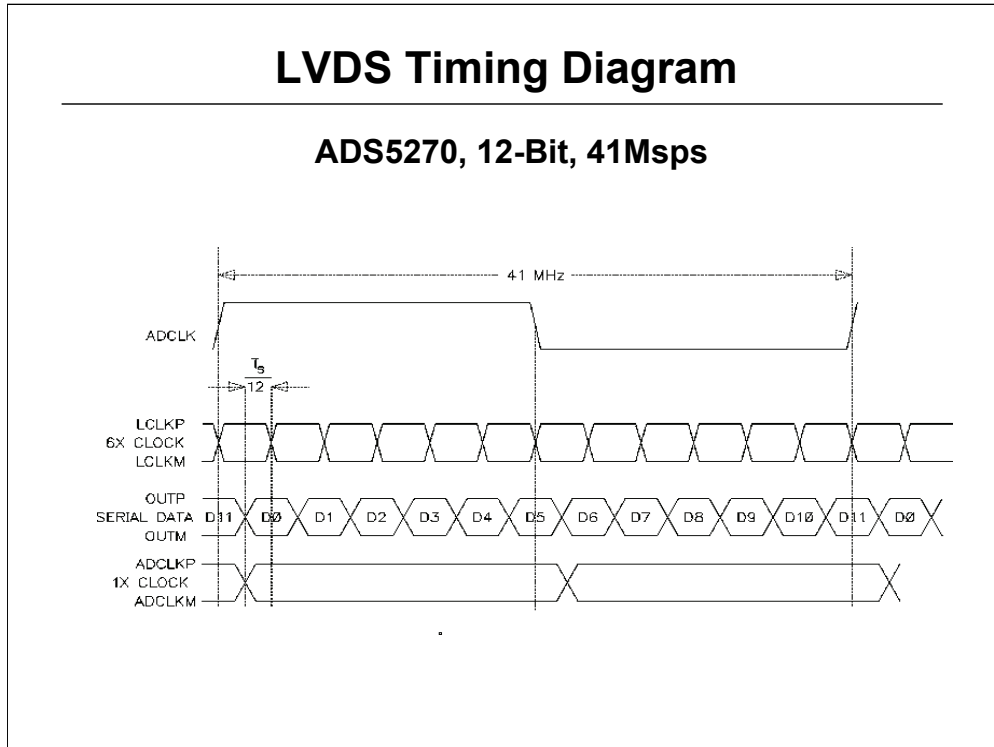◆ Can implement Double Data Rate (DDR)
◆ More I/O lines needed

Embedded Clock

◆ Special data format (8b/10b)
◆ Higher transmission speed required for same amount of data
◆ PLL required in receiver, which increases complexity
◆ Fewer I/O lines needed

Double Data Rate (DDR) Clocking

◆ DDR clocking reduces frequency of Data Clock by a factor of 2

◆ DDR clocks Data bits on both *rising* and *falling* edges of the Data Clock

Non DDR System

For example:
600 Mb/s

600 MHz

DDR System

600 Mb/s

300 MHz
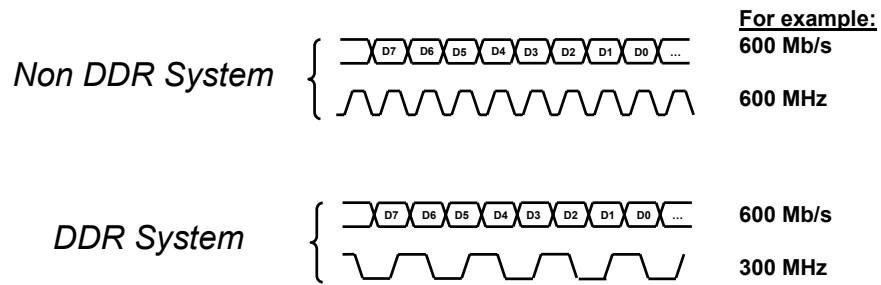
◆ DDR is supported by major FPGA manufacturers

LVDS Timing Diagram

ADS5270, 12-Bit, 41Msps

The timing of the ADS5270 is based on double data rate clocking. Hence, six clock cycles are used for 12 bits of data.

# 8-Channel 40/50 MSPS 12-Bit ADCs with LVDS Interface

ADS5270, ADS5271

Features

40/50 MSPS Sample Rate
8 Simultaneous Sample and Hold
LVDS Data Clock and Word Clock Outputs
Serialized LVDS Outputs
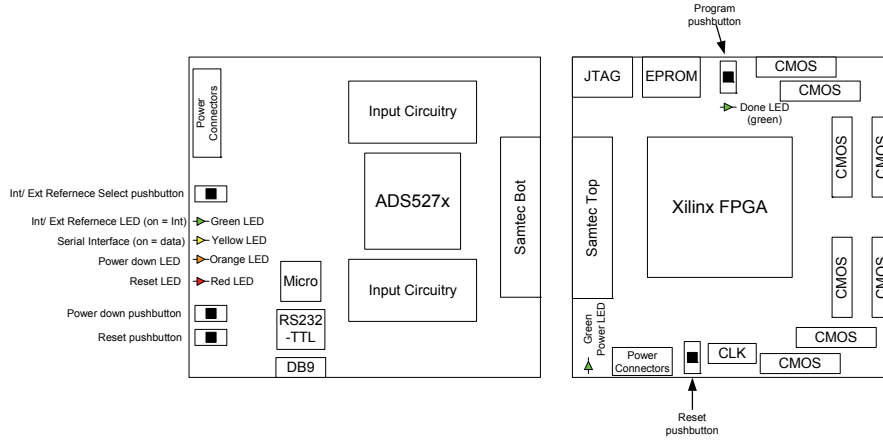**Internal and External References**
Samples available
Introduced
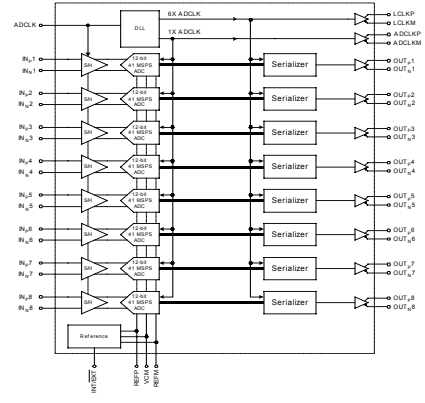
Key Specs

ADS5270 Parameters	Min	Typ	Max	Unit
Analog Supply	3	3.3	3.6	V
Digital Supply	3	3.3	3.6	V
SNR @ Fin = 10MHz	68	70		dB
SFDR @ Fin = 10MHz		85		dB
Total Power		950		mW

HTQFP-80
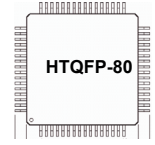
LVDS ADC and Deserializer EVMs

ADS527x family: 10-/12-Bit, 40/50Msps
8-Channel ADCs with serialized LVDS

Appendix

- – HS-ADC Testing
- – Pipeline Architecture, Basic Overview

Typical ADC Bench Test Setup
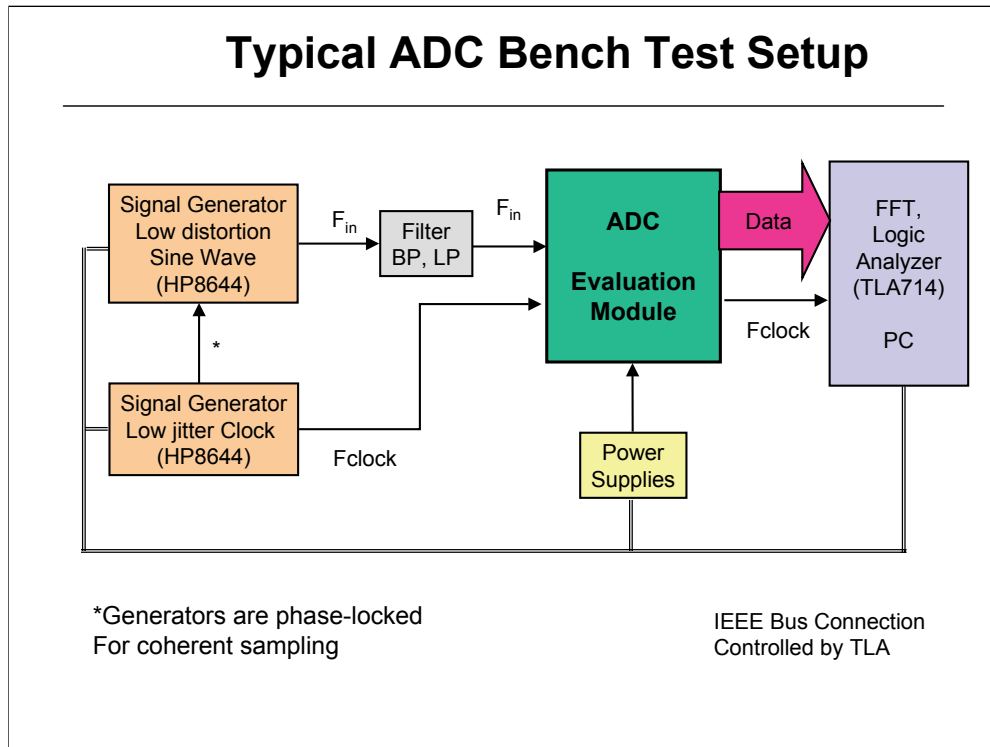
Equipment and configuration of a typical bench test set-up for high-speed A/D converter testing. One critical element is a very low jitter signal generator for the clock. The generator should also have a very high frequency resolution to perform coherent sampling and avoid windowing on the FFTs.

Signal Filter: using bandpass filter usually results in lowest noise.

Most manufacturer use passive high-order LC filter; e.g. from TTE or Allen Avionics

Note that those LC filter may generate distortion itself when driven with a large signal amplitude.

ADC Performance Specifications

◆ Primary focus on Dynamic Performance (ac)
- SFDR
- THD, SINAD, ENOB
- SNR

Most relevant for
Frequency Domain Applications

◆ Static Performance (DC)
- INL, DNL

Relevant for
Time Domain Applications

What's the Application/EE ?

Time Domain

- ◆ **Imaging (CCD)**
    - ▪ Camcorders
    - ▪ Digital Cameras
    - ▪ Scanner
    - ▪ RGB/Comp. Video
    - ▪ Test Instrumentation
    - ▪ Medical
- ◆ **Important Specs:**
    - ▪ SNR
    - ▪ Slew-Rate/ tset
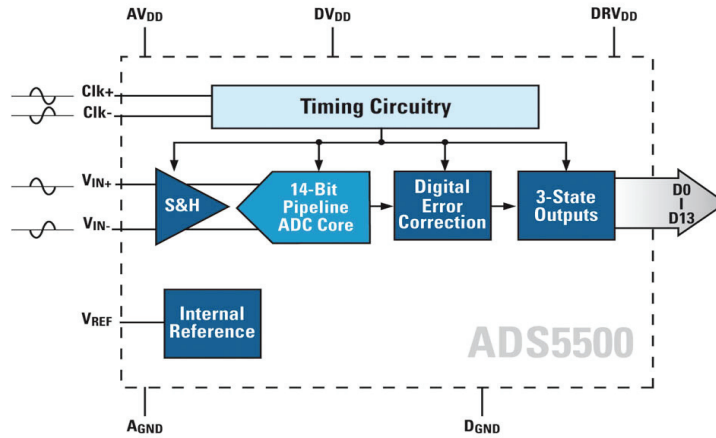   - ▪ DNL
    - ▪ DC-Accuracy/ Drift

Frequency Domain

- ◆ **Communications**
    - ▪ Set-Top Box
    - ▪ Cable Modem
    - ▪ Basestation
    - ▪ IF Digitizer
    - ▪ GPS
    - ▪ Frequency Synthesizer
- ◆ **Important Specs:**
    - ▪ SFDR
    - ▪ ENOB
    - ▪ Analog Input Bandwith
   - ▪ Jitter

ADS5500 – 14-Bit Pipeline A/D

Pipeline A/D Converter

- ◆ **High Conversion Rate, f_{CONV} > 200MHz**
- ◆ **Very Low Power Consumption**
- ◆ **Wide Analog Input Bandwidth (>500MHz)**
- ◆ **Optimized Error Correction**
- ◆ **Usually with Internal Reference (FSR options)**
- ◆ **Monolithic , small Packages**
- ◆ **Switched Inputs, Capacitive**
- ◆ **Data Latency**
- ◆ **Minimum Clock Frequency**

The last architecture that will be discussed is the pipeline technique, which can be considered also another derivative of the "one bit" comparator topology of the successive approximation converter and the "all bits at once" design of the flash ADC. As the next logical step after the sub-ranging architecture, pipeline converters are just beginning to emerge on a broad basis throughout the IC industry, although, the proof of concept was done about eight years ago.

Because of their concurrent digitizing technique pipeline converters achieve comparably high conversion rates. Built as monolithic ICs on CMOS processes one of their biggest advantage is the low power consumption. Even though pipeline converters use the flash architecture as a subcircuit in their processing path they do not exhibit the problem with sparkle codes. This is essentially due to the fact that each flash converter is of low resolution (1 to 2 bits). This means that the number of comparators is very small, which results in a good separation of their threshold voltages compared to pure flash converter. The appearance of false codes, or "sparkle codes" due to the false trigger of one of the comparators is not an issue with pipeline A/D converter.

Pipeline A/D Converter
Architecture Overview
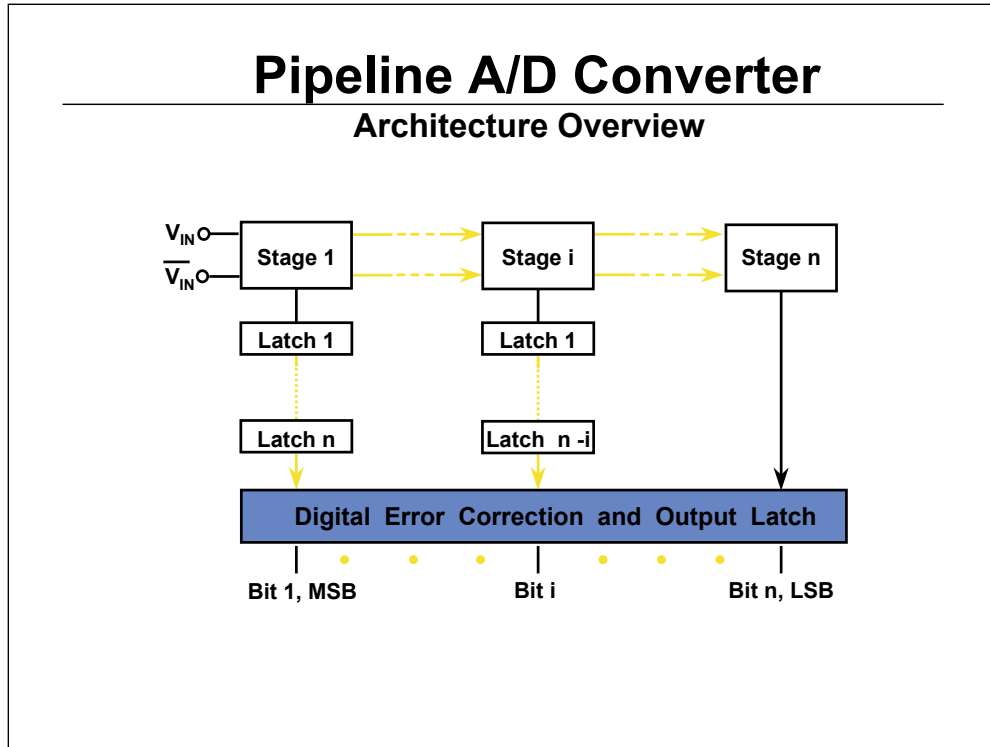
A pipeline A/D converter consists of a number of consecutive stages. The number of stages is often similar to the number of bits of resolution. The stages are similar in their function, as will be discussed later, and each stage only resolves one or two bits. Each individual stage consists of a sample and hold, a low resolution flash A/D converter, a low resolution D/A converter and a summing stage including an interstage amplifier for providing gain. The outputs of each stage are combined in the output latch.

Stage 1 takes a sample of the input voltage and makes the first coarse conversion. The result is then the MSB and its digital value is fed to the first latch (Latch 1). As the residue of the first stage gets resolved in the subsequent n-stages the MSB value is rippled through the n number of latches in order to coincide with the end of the conversion of the last stage. Then all data bits are latched in the output and are available to the data bus.
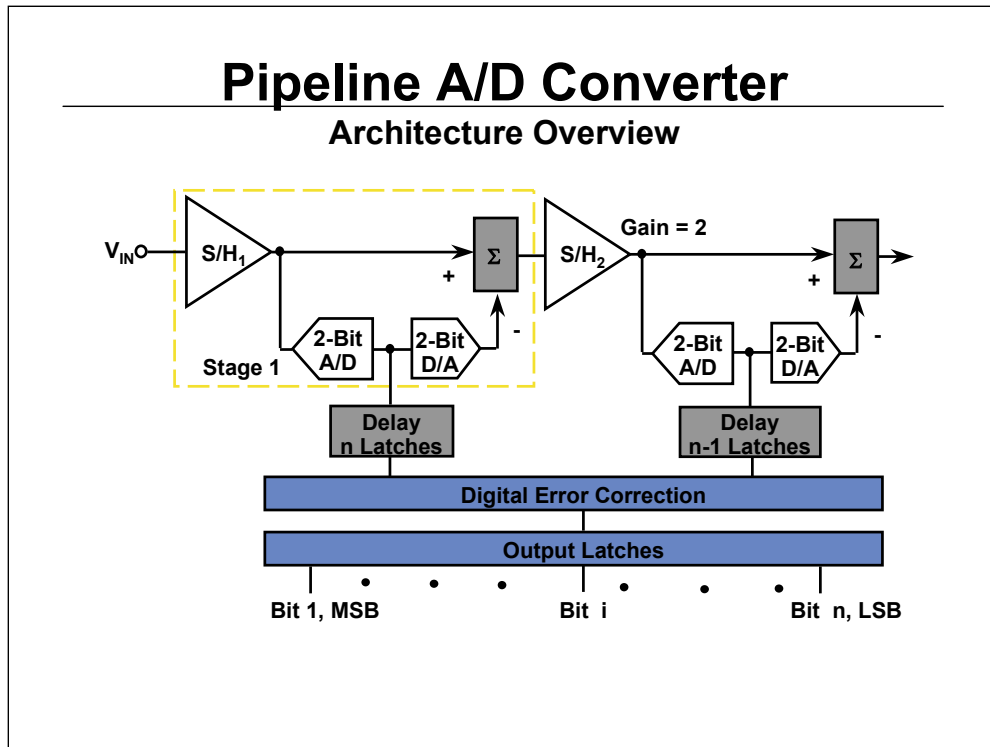
This figure depicts the conceptual blocks inside a pipeline A/D converter. The structure is highly repetitive where each of the pipeline stages consists of a S/H, a flash A/D converter, a D/A converter, a subtractor including a gain stage and latches for delay. Both, the A/D and D/A converter are of low resolution, in this case 2 bits. To begin a conversion, the input is sampled and held. The held input is then converted into a digital code by the first stage low resolution A/D converter and back into an analog signal by the D/A converter. The difference between the D/A output and the held input is the residue that is amplified and sent to the next stage where this process is repeated. At any instant, while the first stage processes the current input sample, the second stage processes the amplified residue of the previous input sample from the first stage. Because sequential stages simultaneously work on residues from successively sampled inputs, the digital outputs from each stage correspond to input samples at different times. Digital latches are needed to synchronize the outputs from the n-stages.

Each stage includes an amplifier to amplify the signal before passing it on to the next stage. The gain error in each of those amplifiers is often the main contributor to the ADCs differential linearity error (DNL).

Pipeline A/D Converter

◆ Pipeline architecture
  ▪ Low resolution ADCs in each inter-stage
  ▪ Better error correction due to extra bit per stage

◆ Pipeline uses separate S/Hs for each stage
  ▪ Allows the remainder signal to be passed down to next stage
  ▪ This frees up the previous S/Hs to process the next sample

◆ Parallel processing increases the throughput rate
  ▪ Multiple samples are being converted at the same time in different stages

Due to the small dimensions (die size) and low power consumption, the pipeline architecture is more suitable for high-resolution applications than flash converters, but is also susceptible to circuit imperfections, such as offset/gain error, and nonlinearities.

Pipeline A/D Converter

Signal Encoding: SAR vs. Pipeline
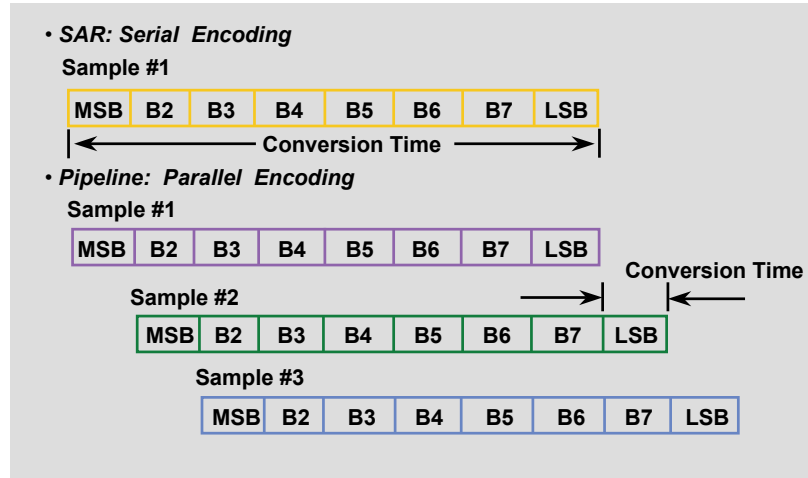
The main advantage of pipeline ADCs is that they can provide a high throughput rate with moderate IC design complexity and low power consumption. This is because of the concurrent operation of the n-stages. The associated "data latency" is not a limitation in most applications. Two main clock phases are required per conversion; because the pipeline ADC uses flash converters. Therefore the maximum throughput rate can be high.

After the initial data latency time, the data representing each succeeding sample is output with every following clock pulse.

Pipeline A/D Converter

Timing and Data Latency
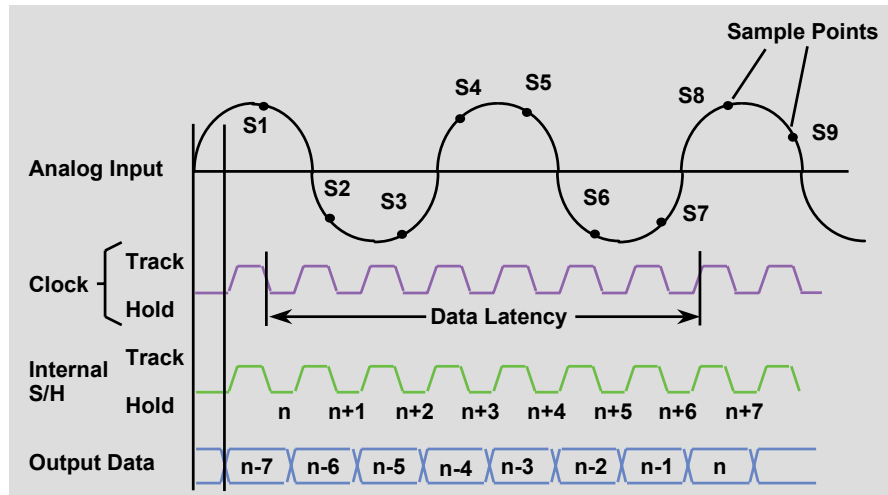
To obtain the best performance from pipelined A/D converter the designer needs to make careful considerations about the timing and the clock source. This is basically true for all high speed A/D converter architectures. Clock jitter can introduce a significant error and needs to be kept low to avoid a degradation of the resolution.

With pipeline A/D converter the rising and the falling clock edge are used to initiate certain operations. Each converter stage in the pipeline will be sampling during one phase and amplifying in the other phase. The internal S/H clock applied to each sub-converter is offset by 180° phase from the previous stage clock signal with the result that alternate stages will perform the same operation (concurrent operation).

The duty cycle of the external clock should be held at 50% with a low jitter especially when digitizing a high frequency input signal and operating the maximum sample rate. A deviation from the 50% duty cycle will effectively shorten some of the allowed interstage settling times, thus degrading the SNR and DNL performance.

The first valid digital data of the pipeline architecture will have an associated delay before it becomes available at the bus. This delay is called "Data Latency" and is dependent on the number of internal converter stages .