Section 6

High Speed Applications

Applications Outline

- Basic Video Distribution
- Transimpedance Amplifier Design
- Differential ADC Solutions
- Transconductance Amplifier Design
- Back Matching Controlled Impedances
- Low-Pass Topologies
- Equalization Circuits

Composite and Component Bandwidths with DC Requirements

Standard/Application	Symbol	TV-NTSC	TV-PAL	DTV	DTV	DTV	DTV	VGA	SVGA	XGA	SXGA	UXGA
Total Horizontal Active Pixels	H_{PA}	451	538	640	704	1280	1920	640	800	1024	1280	1600
Total Vertical Active Lines	V_{LA}	483	576	480	480	720	1080	480	600	768	1024	1200
Horizontal Visual Resolution (TV Lines)	TVL	338	403	336	336	504	756	336	420	538	717	840
Max Video Signal BW	**BW_S**	**4.2**	**5.1**	**7.9**	**11.5**	**26.0**	**26.0**	**10.7**	**17.6**	**28.5**	**51.9**	**71.4**
BW(-3B) Nominal for **0.5dB flatness** (Mhz)	BW 0.5	18	22	34	49	111	111	46	75	122	223	306
BW(-3B) Nominal for **0.1dB flatness** (Mhz)	BW 0.1	41	50	78	113	255	255	105	172	280	510	701
Slew Rate Nominal (V/µs)	SR	53	64	100	144	327	327	135	221	359	653	897

Standard Voltages	Composite NTSC	Composite PAL	Graphics RGB	NTSC S-VHS	PAL S-VHS	NTSC RGB	PAL RGB
SETUP	53.6mV	0mV	0mV	53.57mV	0mV	53.6mV	0mV
VIDEO	714mV	700mV	700mV			714mV	700mV
SYNC	-286mV	-300mV	-300mV	-286mV	-300mV	-286mV	-300mV
Y				714.29mV	700mV		
V				835.6mV			
C					885.1mV		
BURST	286mV	300mV					

Broadcast and Consumer Video

Composite Video (Color and Brightness on one line)

Studio's also use serial digital coded video for distribution

Computer and High End Graphics

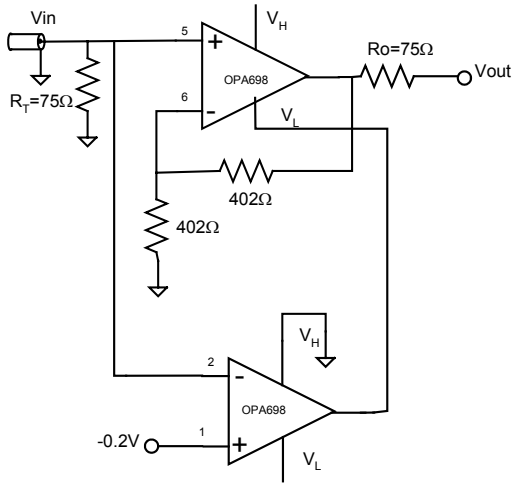
RGB, YUV – 3 Inputs to get full color information

CCD Imaging outputs – Right out of imager this is a series of pulses – However camera video outputs are Composite format

Video Sync Stripper

Typical Application

- **OPA698 VFB High-Speed Amp with Limiting Output**
- **High Linearity for precision Limiting accuracy ±15mV**
- **Fast Recovery from Overdrive: 2.4ns typically**
- **Slew Rate: 1000V/µs**
- **Gain of 1 Bandwidth 530MHz**



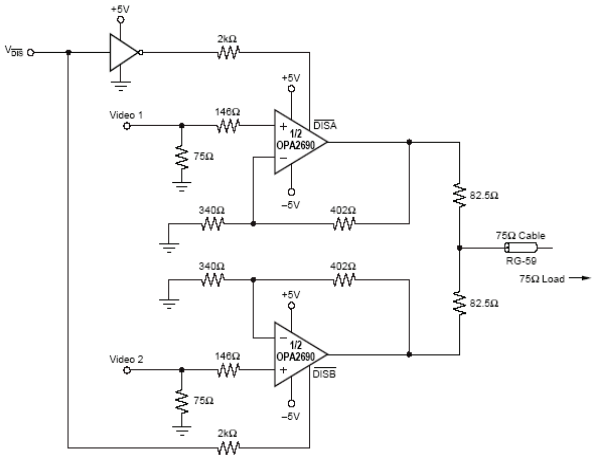
The sync stripper uses two OPA698 output limiting op amps to strip the sync tip from video signals. The lower OPA698 is configured as a limiting inverting comparator where its plus input is referenced to the clipping level (ex -0.2V). The signal is clipped for any voltage greater than -0.2V. The unused voltage limiting is set to a default of -3.5V. The output of the comparator (OPA698) then sets the V_L limiting of the signal amp therefore striping the voltage of the sync levels in the composite signal. The signal amp gain is set for 2 and dc coupled to account for the loss of signal due to back matched cable termination, where loss is ½.

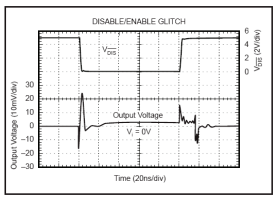
The OPA698 has many applications. The amp easily creates a full or half wave rectifier an easier task since the parasitic components of external diodes are eliminated, see the data sheet for circuit schematics. Also for AC couple systems where dc of the signal needs to be restored, one can use an OPA698 and OPA660 as shown in the data sheet to restore dc levels. Finally, Analog to Digital converters often want to limit the voltage to improve saturation of the ADC, using OPA698 will improve the recovery time and protect the ADC from consist overdriving conditions.

DC Coupled Two to One Video Switch

Typical Application

- Output impedance matches the transmission line impedance.
- When part is on ±5 operation a standard digital output part can be used.
- On +12 volt operation an open collector transistor is recommended for the disable.





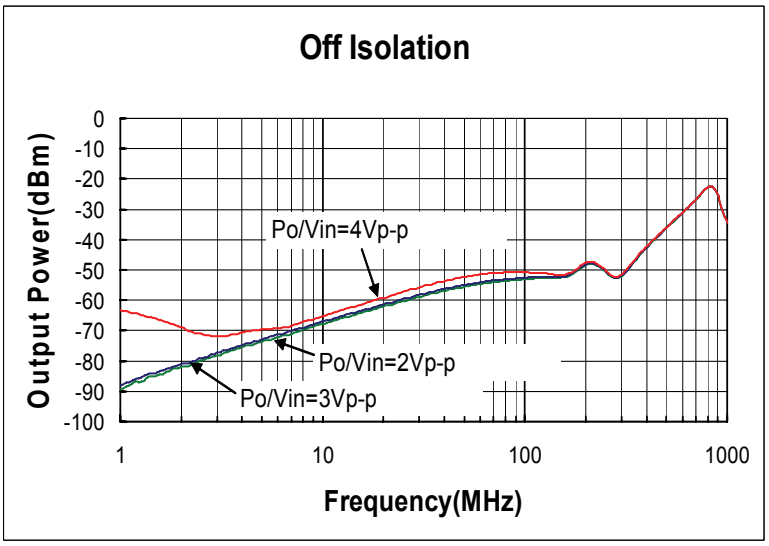
Device	BW-3db G=+2,(MHz)	SR (V/µs)	Iout (mA)	$V_{n\text{-}1MHz}$ (nV/√Hz)	Iib (uA)	V_{IO} (mV)	DG (mA)	Dϕ (dB)	V_S (V)	Package
OPAx690	**220**	**1800**	**190**	**3.1**	**3**	**1**	**0.06**	**0.03**	**+5 to ±6**	**D,DBV**

Video speed amplifiers with disables, allow the designer to create video “Wired-OR Multiplexers. Typically channel switching is done on sync or retrace time in the video signal. The two inputs are approximately equal at this time, therefore the “make-before-break” disable characteristic ensures that one amplifier controls the output line when used in the wired-OR-configuration. Since both amplifiers are on for a very short period of time the transition between channel’s outputs are combined through the output impedance matched resistors 82.5? . When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal before entering the cable. Therefore the gain is slightly increased to accommodate for this loss.

The video multiplexer connection insures that the maximum differential voltage across the inputs of the unselected channel do not exceed the rated ±1.2 V maximum for standard video signal levels.

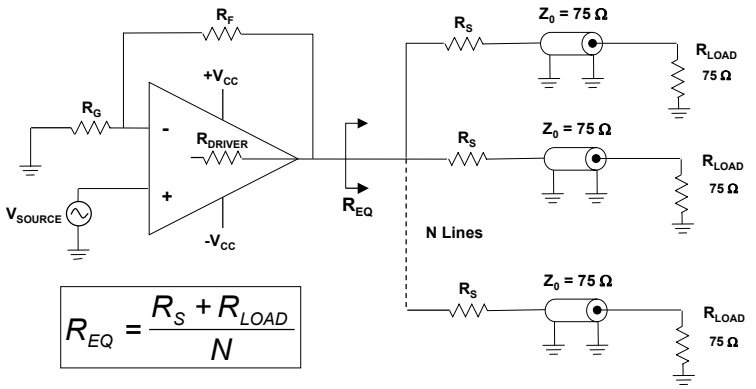
The plot on Disable shows the turn-on and turn-off switching glitches using a grounded input for single channel. The glitch is typically less than ±50mV. As two amplifiers are used then the make-before break will tend to reduce the glitch to around ±20mV.

DC Coupled Two to One Video Switch – Off Isolation OPA2690



The OPA690 provides excellent isolation in a “Wired-OR-Configuration”. As the plot shows for various input voltage levels the isolation in normal video applications will be -76dBc for 3.5Mhz NTSC video and -74.6 for Pal Video

DC Coupled Amps for Driving Multiple Loads



$$R_{EQ} = \frac{R_S + R_{LOAD}}{N}$$

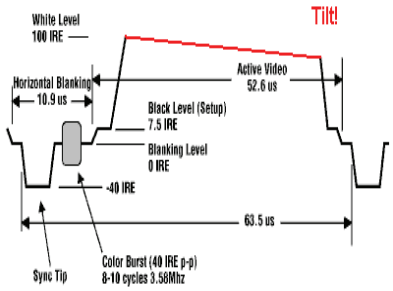
Suggested Line Driver Amplifier

OPA691	OPA2691	OPA3691
THS6002	THS6012	THS6022
OPA2674		

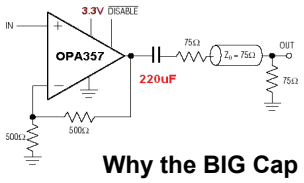
Driving multiple loads put added stress on the amps ability to drive the load. Therefore amps with higher output current are better for parallel loads when trying to maintain professional level of differential Gain and differential ϕ.

Here the amplifier sees N parallel loads even though the characteristic impedance is 75Ω.

Composite Video – Signal



- **Brightness** is coded in **Signal Level**
- TV line is **64µs** long
  - 30 Frames / s
  - 525 lines



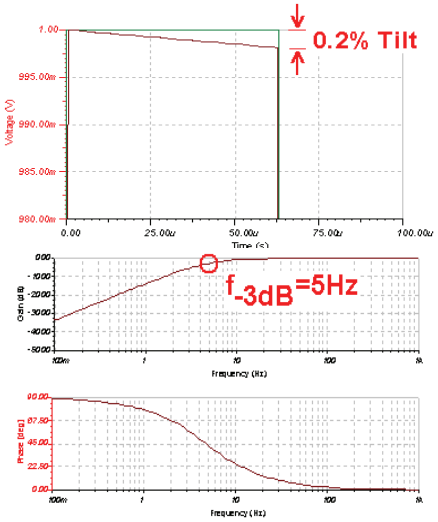
Why the BIG Cap ???

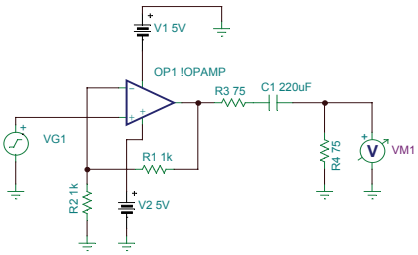
- Output is **AC coupled**
- **Avoid "Tilt" or "Sag"**
  - Change in Brightness
- **Solution: SAG Correction**

Composite Video Signal (NTSC):

- Brightness, Color, Saturation, Synchronization all in one Signal
- Brightness coded in Signal LEVEL (7.5 IRE = Black, 100 IRE = White)
- Color is coded in PHASE DIFFERENCE between Burst Signal and color modulation signal
- Color Saturation coded in AMPLITUDE of color modulation signal

Standard Video Driver– 220µF



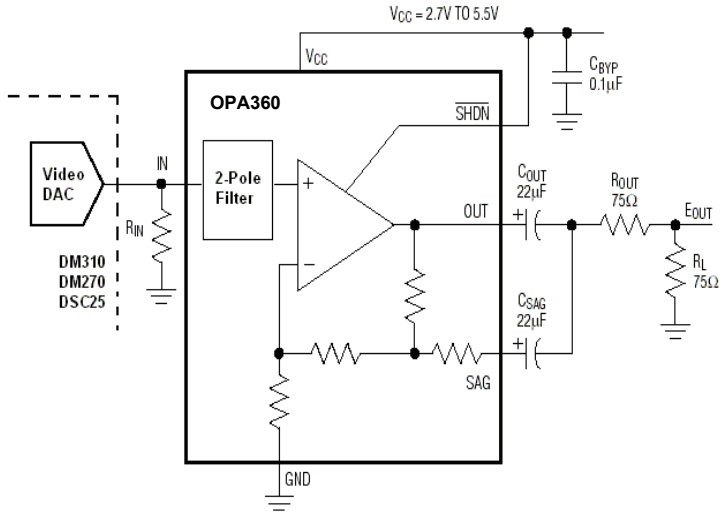


- 220µF is **BIG** in size
- **THICKNESS** is ~3mm
- **EXPENSIVE**

The output capacitor (220microFarad) is used for the SAG correction. However, this capacitor is large and expensive for many low cost video applications. The capacitor is necessarily large since the white signal (flat pulse) will discharge over time, and the large capacitor gives you a filter corner frequency (220 µF x 150Ω x1/2p = 4.8 Hz). Note that there is still a small amount of SAG (i.e. .2%), which is generally acceptable.

To nearly eliminate the SAG, would require a corner frequency of about 2 Hz, and require a capacitor of 470 µF.

SAG Correction



Alternate SAG correction using two smaller 22 µF capacitors instead of the one large 220 µF capacitor on the output.

How does it work?

Keeps 6dB Gain at 5MHz

Boosts Gain at Low Freq.

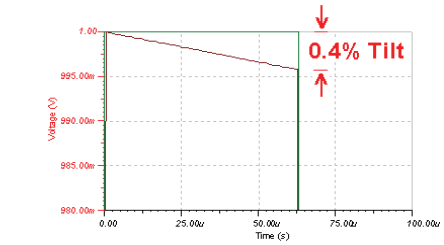
Benefits

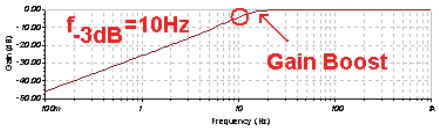
Reduce Cap size / height (substitute two 22 microfarad caps for one 220 microfarad cap)

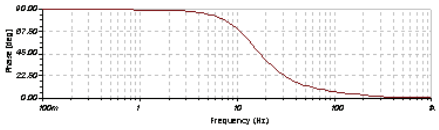
Reduce Cap cost

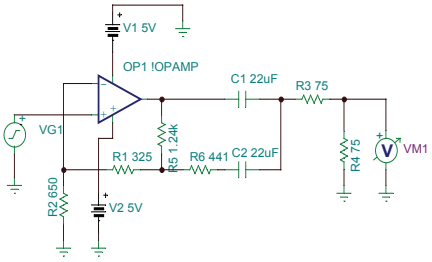
Improve Field Tilt

SAG Correction







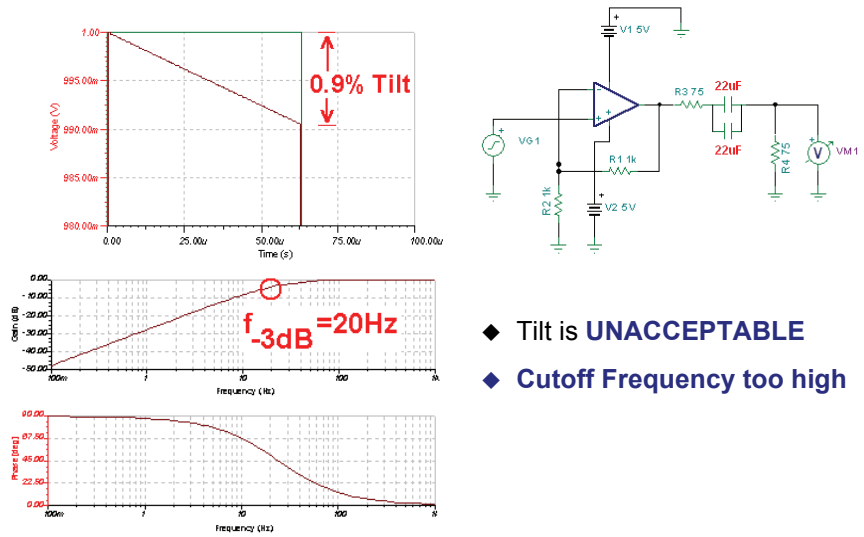


- Dramatic **SIZE REDUCTION**
- Acceptable Tilt
- **LOWER COST** Caps

Using the modified SAG correction circuit produces an acceptable output signal for a lower cost. Note that this circuit reduces the SAG to .4%. This amount of SAG is marginally acceptable

You can further reduce the SAG by increasing the capacitors 33 µF will reduce the SAG to about .2%.

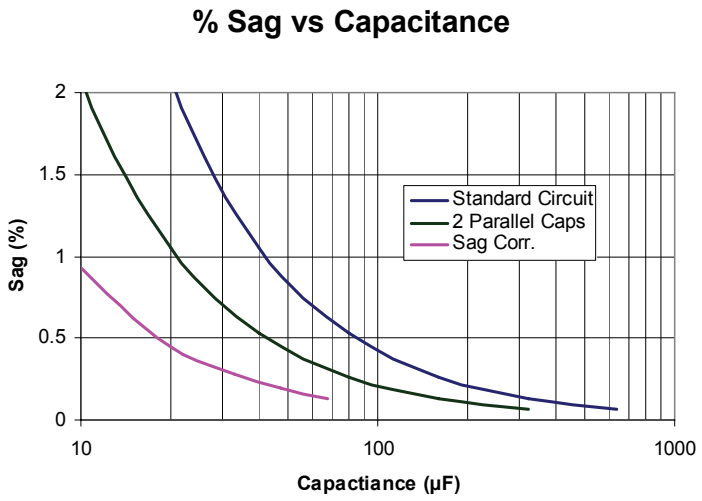
Standard Video Driver– 2x22uF



- Tilt is **UNACCEPTABLE**
- **Cutoff Frequency too high**

Attempting SAG correction with two 22 microFarad caps in parallel yields poor correction results. Note the same components in a slightly different configuration caused drastically different results.

Comparison of Techniques



SAG improves cap size reduction

- By a factor of 4 over conventional circuit
- By a factor of 2 for 2 caps in parallel
- SAG offers the best “tilt” performance with the smallest and cheapest caps.

Transimpedance Amplifier Design

Design Issues Covered

1. 2nd order transfer model for transimpedance circuits
2. Simplifying and solving for design solutions

$$\frac{V_O}{I_D} = R_F \cdot \frac{\frac{A_{OL}\omega_A}{R_F(C_s + C_F)}}{s^2 + s\left(\omega_A\left(1 + A_{OL}\frac{C_F}{C_s + C_F}\right) + \frac{1}{R_F(C_s+C_F)}\right) + \left(\frac{(A_{OL}+1)\omega_A}{R_F(C_s + C_F)}\right)}$$

Transimpedance Gain

Where: $A_{(s)} = \frac{A_{OL}\omega_A}{s + \omega_A}$

Single pole, open loop gain model

$\frac{A_{OL}\omega_A}{2\pi}$ = Gain Bandwidth Product (GBP)

Detecting and amplifying the often very small current signal coming from a photodiode, can present a considerable challenge. The achievable gain, bandwidth, and input referred noise current are all coupled together in a few design variables.

While dedicated transimpedance amplifiers exist for OC-x standards, a myriad of other applications can benefit from the design flexibility offered by a voltage feedback operational amplifier solution.

Quite a lot of earlier design discussions have suggested placing the feedback pole at the intersection of the rising noise gain and the open loop gain curve - this works but yields a slightly peaked response causing unnecessary pulse response overshoot and ringing.

1. Op Amp based, high performance, transimpedance designs can be analyzed using a single pole op amp model to give a 2nd order closed loop transfer function. Although the full transfer function doesn't suggest a design approach, some judicious simplifications will lead to a very simple, and accurate, amplifier compensation methodology.

2. A simple equivalent input noise current equation, correctly including all of the high frequency terms (but neglecting 1/f effects), will allow an easy comparison between design solutions for their achievable sensitivity

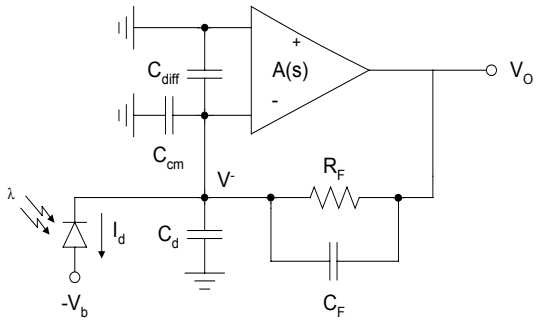
Although we are normally are very interested in the higher frequency open loop poles for the op amp, they can be ignored in this analysis to greatly simplify the results.

Using just a dominant single pole open loop gain model for the op amp, and developing the closed loop transfer function from Id to Vo for the transimpedance configuration, gives a relatively complicated looking 2nd order transfer function.

It is a valid approximation to ignore the higher order poles since we will be dropping to unity loop gain at a relatively low frequency due to the noise gain shaping experienced in this circuit.

Transimpedance Frequency Response Analysis Circuit

- Deceptively simple looking circuit - that causes considerable difficulty in application. C_d is the diode capacitance plus wiring parasitics.



This circuit is complicated by the effect of C_d on the noise gain for the op amp. To get a correct solution for C_f to hit a target closed loop frequency response, include the differential input capacitance for the op amp and one common mode capacitance (that on the inverting node).

Controlling the Frequency Response

Key variables required to determine C_f to get the desired frequency response

- **Total Capacitance on the Inverting node**
- **Gain Bandwidth Product of the op amp**
- **Desired transimpedance gain or bandwidth**

- Total Capacitance on the Inverting node
- Be careful to include the op amp input parasitic capacitance. C_d is the detector diode capacitance under the expected reverse bias.

2. Gain Bandwidth Product of the op amp

- The higher the gain bandwidth, the higher the resulting closed loop transimpedance bandwidth.
- In general, the op amp does NOT need to be unity gain stable. As will be shown, loop gain x-over typically occurs at a very high noise gain - so very wideband, non-unity gain stable, op amps can be used to get their lower input voltage noise.

3. Desired transimpedance gain or bandwidth

- These are interrelated - for a particular op amp selected, targeting the gain will set the maximum bandwidth or, conversely, targeting the bandwidth will set the maximum gain.

Standard Wo and Q form for this 2nd Order Transfer Function.

$$\frac{V_O}{I_D} = R_F \cdot \frac{A_{OL}}{A_{OL}+1} \cdot \frac{\omega_O^2}{s^2 + s\frac{\omega_O}{Q} + \omega_O^2}$$

$$\omega_O = \sqrt{\frac{(A_{OL}+1)\omega_A}{R_F(C_S+C_F)}} = F_O(2\pi)$$

$$Q = \frac{\sqrt{\frac{(A_{OL}+1)\omega_A}{R_F(C_S+C_F)}}}{\omega_A\left(1+A_{OL}\frac{C_F}{C_S+C_F}\right)+\frac{1}{R_F(C_S+C_F)}}$$

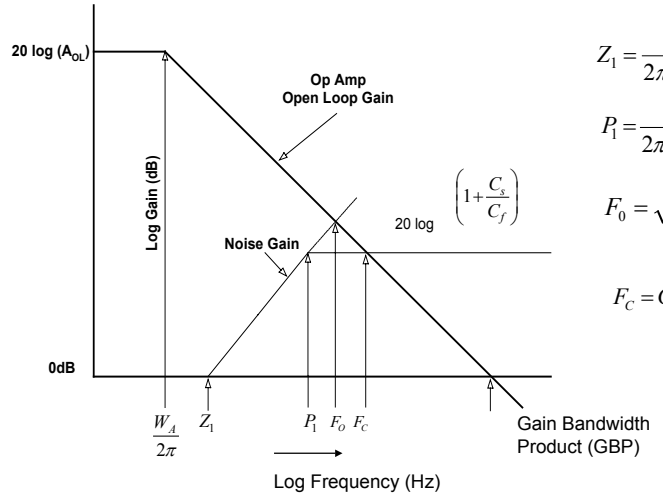
Manipulating this full transfer function into a filter analysis format - gives the ω_o and Q shown above.

If we have picked an amplifier, the Gain Bandwidth Product is set.

If we have picked a diode, the inverting node capacitance is set.

We are then left with just R_f and C_f to control both ω_o and Q. Should be able to arrive at a solution.

Bode Plot of the Loop Gain for the Transimpedance Op Amp Configuration



It is often instructive to look at the op amp circuit in loop gain form to view what each of the critical elements in the design mean graphically.

The plot shows the open loop characteristic of the op amp with the noise gain superimposed - that gain starts out at 1 (0dB) then rises at Z_1 with single zero response caused by the feedback resistor and inverting input capacitance up to the pole formed by R_f and C_f. Several important points to note.

- F_o is in fact the characteristic frequency of the closed loop response.
- Noise gain at cross-over is $1+C_s/C_f$ which can be very high - hence, unity gain stability is not required.

Analysis Simplifications

Algebraic simplifications to get an easy compensation solution.

1. With $C_s >> C_f$, drop C_f from Z1 Equation
2. Let $(Aol + 1)Wa/2\pi$ = GBP (gain bandwidth product in Hz)
   - This is simply neglecting the "1"
3. Drop the "1" in $(1 + Aol(C_f/(C_s+C_f)))$

An exact solution for C_f to get a target Q is extremely complicated - it can be considerably simplified by ignoring a few terms with a very minor error in the resulting value for C_f.

Simplified Expressions for Fo and Q

$$F_O = \sqrt{Z_1 \cdot GBP}$$

$$Q = \frac{F_O}{Fc} = \frac{P_1}{F_O}$$

These two equations give a very simple path to transimpedance design.

The 2nd order characteristic frequency is fixed by the Amplifier Gain Bandwidth Product and the zero formed by the transimpedance gain resistor and the source capacitance

The Q of the 2nd order closed loop transfer function is simply the ratio of the pole frequency set in the feedback path to the characteristic frequency (P_1/F_o) which is also equal to the ratio of the characteristic frequency to the intersection of the open loop response with the high frequency noise gain ($1+C_s/C_f$) - this is F_o/F_c.

Further Design Simplifications

If a target of Q = 0.707 is set, a very simple design methodology results.

- At Q = 0.707, the 2nd order closed loop response gives an $F_{-3dB} = F_o$
- So, if we set P1 = 0.707*Fo, we get an $F_{-3dB} = F_o$

Assuming this - and then targeting an F_{-3dB}, sets the F_o target in a design.

$$F_{-3dB} = F_O = \sqrt{Z_1 GBP} \text{ (With Q = 0.707)}$$

$$Z_1 = \frac{(F_{-3dB})^2}{GBP} = \frac{1}{2\pi R_F C_s}$$

Maximum achievable gain given C_s, GBP, and target F_{-3dB}

$$R_F = \frac{GBP}{(F_{-3dB})^2 2\pi C_s}$$

This slide steps through finding the maximum available transimpedance gain for a given op amp and diode if a maximally flat Butterworth response is the target design. This target is interesting in that if we set P1 at 0.707*F_o, it circles back to give us a F_{-3dB} equal to F_o. Kind of unique and interesting design point.

More general targets with peaking can be design using the initial equations.

A very useful alternative way to use these equations is to know your desired transimpedance gain and bandwidth and use them to solve for the minimum required GBP. Then using an amplifier with a GBP > than that minimum, along with this target transimpedance gain, can be designed using the C_f calculation on the next slide.

Simplified Design Continued

With maximum achievable gain (R_F) set, can go back and set C_F to put P1 where it needs to be for Q = 0.707

$$\frac{1}{2\pi R_F C_F} = P_1 = 0.707 \cdot F_O = 0.707 \cdot F_{-3dB}$$

$$C_F = \frac{1}{R_F (0.707) 2\pi F_{-3dB}}$$

$$i_{EQ} = \sqrt{i_b{}^2 + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n 2\pi F C_s\right)^2}{3}}$$

Using the F_{-3dB} from the previous slide (which, with the Q=.707 constraint, occurs at the geometric mean of the GBP and the zero in the noise gain) and this maximum R_f, C_f can be solved

Lower R_f's, if needed by the design, can be used and placed into this equation as well.

The total input referred current noise equation that often appears in the TI-Tucson High Speed de-compensated voltage feedback op amps uses several simplifying assumptions to arrive an approximate expression. Specifically -

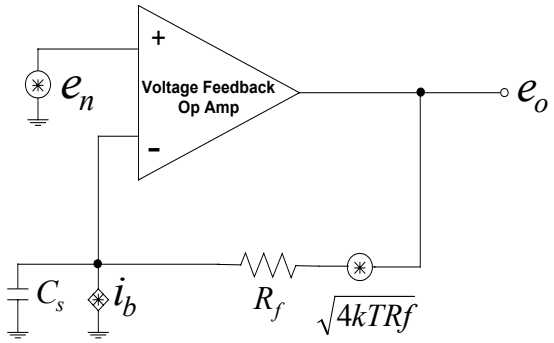
1. This is an integrated noise analysis that uses spot noise over frequency - not intended as a spot noise equation for narrowband applications.

2. We are assuming the application is DC coupled, pulse oriented where the integrated noise is of interest.

3. The final signal bandwidth for both the transimpedance design and any post filtering is >10X the 1/f noise corner for any of the op amp noise terms - this allows those effects to be neglected for integrated noise purposes

4. While the amplifier must be compensated with a feedback capacitor, it is much simpler for noise calculation purposes to assume a noise power bandwidth lower than this that will be set further downstream in the signal path. This means the target transimpedance bandwidth should be set > than the bandwidth that will be set by postfiltering.

Transimpedance Noise Analysis Circuit



A thorough expression for transimpedance output noise can be extremely complicated This principally arises from two issues -

- Including 1/f effects in the analysis - neglecting those for broadband applications creates a slight error but considerable simplicity.
- Allowing each noise term to be combined at the output with a frequency response set only by the transimpedance amplifier design itself. If we assume the transimpedance stage is designed to provide > than the desired final signal bandwidth, a postfilter downstream can be assumed for noise power bandwidth limiting purposes. That frequency “F” can then be used to calculate integrated noise.

The input noise terms needed for a transimpedance design are shown here. This includes -

- Non-inverting input voltage noise (e_n - this will have a gain to the output of “1” at DC then increasing at 20dB/dec. beyond $(1/2\pi R_f C_d)$Hz which is the zero frequency (Z1) in the noise gain.
- Inverting input current noise (i_b)
- Feedback resistor noise voltage = $\sqrt{(4kTR_f)}$

These are all shown as spot noise voltage and current density terms - they can be combined at the output times their gain then squared to get power. No feedback cap. is shown for this analysis but is absolutely required for stability.

Total Output Noise Power

- To get the total output noise power, take each noise term times its gain to the output, square it, then add.
- Note that this circuit does not show a feedback capacitor - that capacitor (Cf) is absolutely required for stability but is not shown here to since the noise integration frequency is assumed to be less than the pole set by (1/2πRfCf)Hz = P1

$$e_o^{\,2} = 4kTR_f + (i_b R_f)^2 + e_n^{\,2}[1 + (2\pi f C_s R_f)^2]$$

The resistor voltage noise power shows up directly at the output with no gain.

The amplifier's inverting input current noise shows up at the output times the feedback resistor. Square that to get the noise power

The amplifier's input voltage noise has a gain to the output that traces out the noise gain curve shown earlier in the Bode analysis. Only the zero is considered here since we will assume a frequency of integration that is less than the pole and set by a post filter. Again, square this output noise voltage term to get power.

Input Referred Equivalent Input Noise Current

Input refer e_o^2 by dividing by R_f^2

$$i_{eq}^2 = \frac{4kT}{R_f} + i_b^2 + \frac{e_n^2}{R_f^2} + e_n^2(2\pi f C_d)^2$$

Frequency dependent term

To compare different designs, it is more common to compare equivalent input referred current noise. We are essentially trying to develop an equivalent input noise current value that is flat over frequency that will integrate to the same output noise power over the “F” noise power bandwidth as the actual amplifier output noise would.

Getting an average value for the last term.

For f = 0 → F

Average the noise power
of the 4th term over the noise power bandwidth - "F"

$$\frac{1}{F}\int_0^F (e_n 2\pi f \times C_d)^2 df = \left[\frac{(e_n 2\pi \times C_d)^2}{F} \times \frac{f^3}{3}\right]_0^F = \frac{(e_n 2\pi C_d F)^2}{3}$$

Input Referred equivalent input noise current

$$i_{EQ} = \sqrt{i_b{}^2 + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{(e_n 2\pi F C_s)^2}{3}}$$

The final term in the total input referred noise current expression increases with frequency - this is the differentiated input noise voltage of the op amp that will appear at the output. To get an average equivalent value, this must be integrated over F then divided by F. Strictly speaking, a starting integration value of 0Hz is not physically correct - but can be used as a simplification.

This average value over "F" for the last term may now be combined with the other 3 terms that have no frequency dependence to get the total equivalent input referred current noise expression.

This input referred spot noise current will integrate to the same total output noise power as the actual output noise spectrum if the frequency span of integration is limited to "F". This expression is what shows up in the data sheets.

Equivalent Input Spot Current Noise for Output Noise Integrated to F < P1

$$i_{EQ} = \sqrt{i_b{}^2 + \frac{4kT}{R_F} + \left(\frac{e_n}{R_F}\right)^2 + \frac{\left(e_n 2\pi F C_s\right)^2}{3}}$$

Where:

i_b = Inverting input spot current noise for the op amp

$4kT = 16 \times 10^{-21}$ J at 290K

R_F = the feedback resistor value

e_n = Non-inverting input spot voltage noise for the op amp

C_s = Total capacitance on the inverting node of the op amp

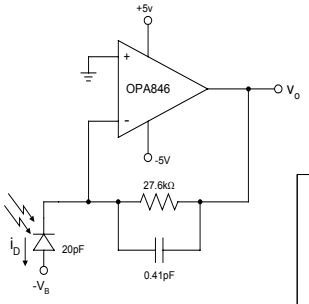
F = Frequency limit of noise integration ($\leq P_1$)

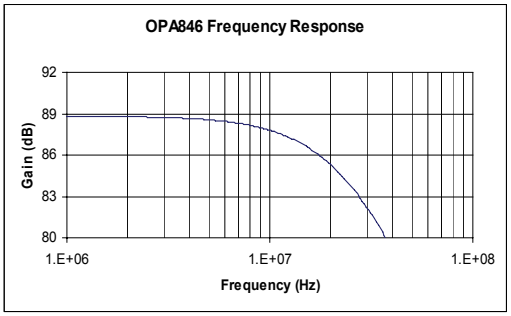
Design Examples - Getting a Target Bandwidth Given a Source Capacitance

- Select an Op Amp with a particular GBP - include its input parasitic capacitance + the source diode capacitance to solve for Z1 given the desired bandwidth and actual GBP. With Z1 set, solve for achievable maximum gain, = R_f to get the minimum input referred noise current.
- Set P_1 at Q *F_o. Use this and R_f to solve for C_f.
- Check that 1 + C_s/C_f > minimum stable gain for the op amp selected

VOLTAGE FEEDBACK AMPLIFIERS SUITABLE FOR TRANSIMPEDANCE APPLICATIONS										
THIS IS LIMITED TO GBP > THAN 200MHz										
Part #	Input Type	GainBandwidth	Minimum Stable	Input Voltage	Input Current	Min. Supply	Max. Supply	Supply	Multi-Channel	
		Product(MHz)	Gain (V/V)	Noise (nV)	Noise (pA)	Voltage	Voltage	Current(mA)	Versions	
OPA820	Bipolar	240	1	2.4	1.6	5	12.6	5.6	Quad	
OPA690	Bipolar	300	1	5.5	3.1	5	12.6	5.5	Dual,Triple	
OPA842	Bipolar	200	1	2.6	2.7	7	12.6	20.2		
OPA843	Bipolar	800	3	2	2.8	7	12.6	20.2		
OPA846	Bipolar	1750	7	1.2	2.8	7	12.6	12.6	Dual	
OPA847	Bipolar	3900	12	0.85	2.5	7	12.6	18.1		
OPA656	JFET	230	1	7	0.002	7	12.6	14		
OPA657	JFET	1600	4	4.8	0.002	7	12.6	14		
THS4021	Bipolar	1400	7	1.5	2			8.1	Dual	
THS4031	Bipolar	200	1	1.6	1.2			8.5	Dual	
OPA355	CMOS	200	1	4	0.002			8.3	Dual,Triple	

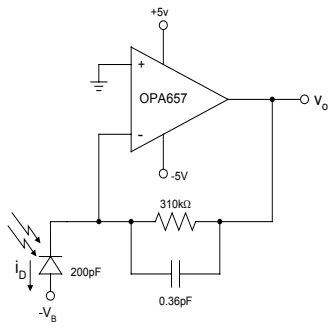
Example Design Using a Wideband Bipolar Input Op Amp.

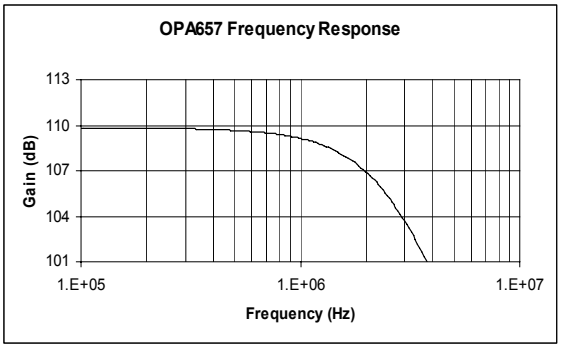




OPA846 WIDEBAND, LOW NOISE, OP AMP								\$1.59/(in thousands)		
Gain Bandwidth Product (non-unity gain stable)								1750MHz		
Non-inverting Input Voltage Noise								1.2nV/root Hz		
Inverting Current Noise (Bipolar Input)								2.8pA/root Hz		
Common-mode parasitic Input Capacitance								1.8pF		
Differential parasitic Input Capacitance								2.0pF		
Diode source Capacitance								20pF		
Desired Butterworth (Q=0.707) Bandwidth								20MHz		
Maximum allowed Rf to get Bandwidth								27.6kohm		
Required Cf								0.41pF		
High Frequency Noise Gain (1 + Cs/Cf)								59V/V		
Equivalent Input Current Noise Density (integrated to P1= 0.707*20MHz)								3.3pA/$\sqrt{Hz}$		
Equivalent Input Integrated Noise ($I_{RMS} = I_{ER}\sqrt{P1}$)								12nA_{RMS}		

Example Design Using a Wideband JFET Input Op Amp





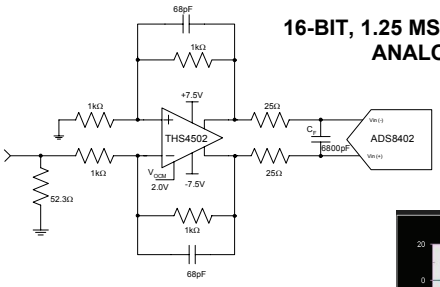
OPA657 SPECIFICATION AND DESIGN	$3.59/(in thousands)
Gain Bandwidth Product (non-unity gain stable)	1600MHz
Non-inverting Input Voltage Noise	4.8nV/√Hz
Inverting Current Noise (Bipolar Input)	1.3fA/√Hz
Common-mode parasitic Input Capacitance	4.5pF
Differential parasitic Input Capacitance	0.7pF
Diode source Capacitance	200pF
Desired Butterworth (Q=0.707) Bandwidth	2MHz
Maximum allowed Rf to get Bandwidth	310kohm
Required Cf	0.36pF
High frequency noise gain (1 + Cs/Cf)	570V/V
Equivalent Input Current Noise Density (integrated to P1= 0.707*2MHz)	5pA/√Hz
Equivalent Input Integrated Current Noise ($I_{RMS} = I_{RQ\sqrt{P1}}$)	$6nA_{RMS}$

Conclusions for Transimpedance Compensation and Noise Analysis

- The closed loop response is a 2nd order low pass,where:
  - The characteristic frequency is always the geometric mean of the zero in the noise gain and the op amp's gain bandwidth product.
  - Placing the feedback pole only changes the Q of the response. Setting P1 = $0.707*F_0$ will give a closed loop Butterworth response with $F_{-3dB} = F_0$
- Since the noise gain always crosses over the open loop gain at a high value if compensated correctly, the op amp does not need to be unity gain stable.
- The output noise can be strongly influenced by the peaked up voltage noise term.
- Generally, Bipolar Inputs are better for low to moderate gains at wider bandwidths while JFET inputs are better for high transimpedance gains at lower bandwidths.
- With Bipolar inputs, a resistor equal to Rf is placed to ground on the non-inverting input to improve DC accuracy - this must be bypassed with a capacitor to kill its noise contribution.

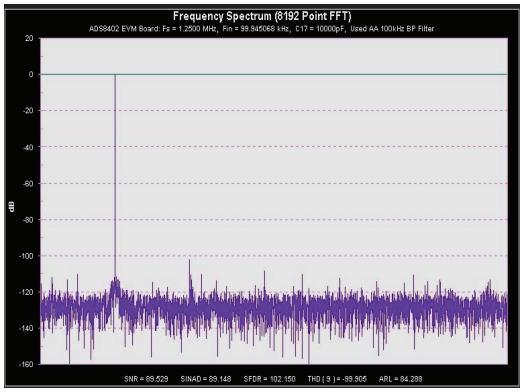
Differential ADC Solutions

THS4502 Driving the ADS8402



16-BIT, 1.25 MSPS, UNIPOLAR DIFFERENTIAL INPUT ANALOG-TO-DIGITAL CONVERTER

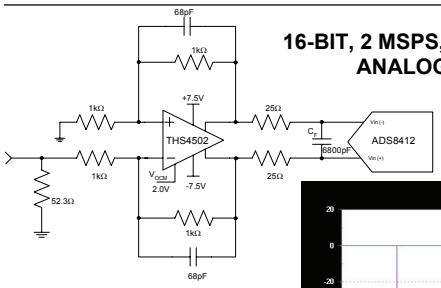
THD = 99.905 dB
SNR = 89.529 dB
SNRD = 89.148 dB
ENOB = 14.579
SFDR = 102.15 dB
$V_{IN\ (@\ ADC)}$ = 8 Vpp
F_S = 1.25 MHz
F_{IN} = 99.945068 kHz
C_F = 6800pF



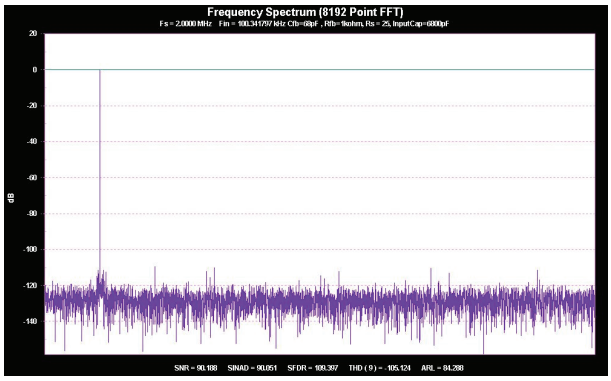
Using the THS4502 to drive the ADS8402 shows no degradation of the ADCs performance at 100kHz input.

The op amp is used to convert the single-ended input signal from a 50 source generator to differential to drive the data converter. A high-order (8^{th} order eliptical) low-pass filter is used between the signal source to clean up the harmonics generated there.

THS4502 Driving the ADS8412



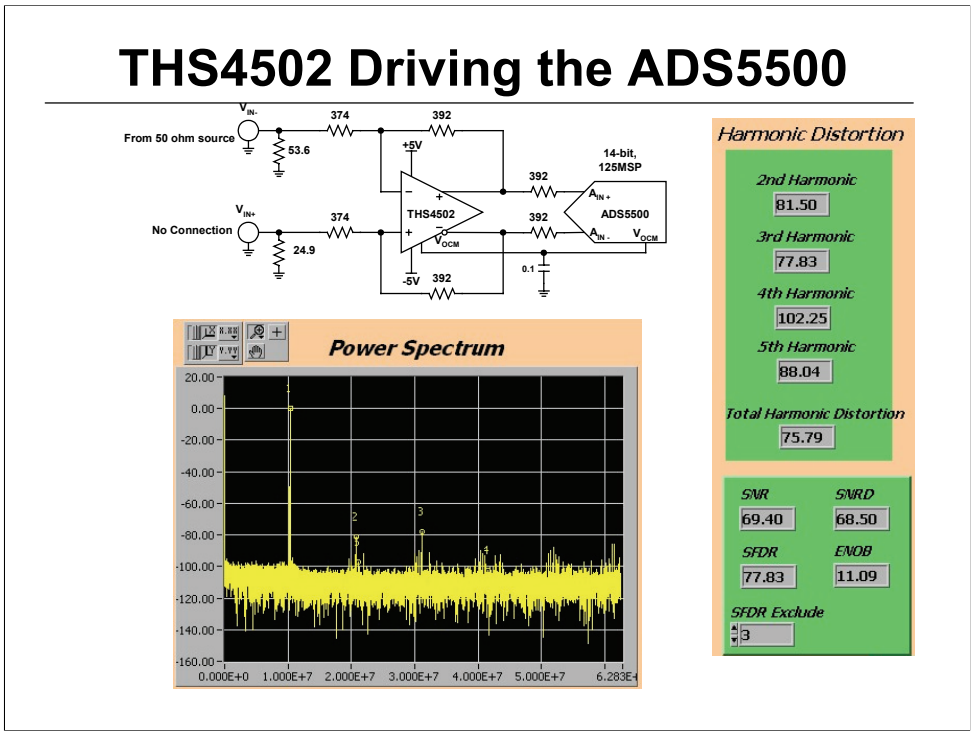
16-BIT, 2 MSPS, UNIPOLAR DIFFERENTIAL INPUT ANALOG-TO-DIGITAL CONVERTER



THD = 105.124 dB
SNR = 90.188 dB
SNRD = 90.051 dB
ENOB = 14.689
SFDR = 109.397 dB
$V_{IN\ (@\ ADC)}$ = 8 Vpp
F_S = 2 MHz
F_{IN} = 100.341797 kHz
C_F = 6800pF

As with the previous slide, using the THS4502 to drive the ADS8412 shows no degradation of the ADCs performance at 100kHz input.

The op amp is used to convert the single-ended input signal from a 50 source generator to differential to drive the data converter. A high-order (8^{th} order eliptical) low-pass filter is used between the signal source to clean up the harmonics generated there.

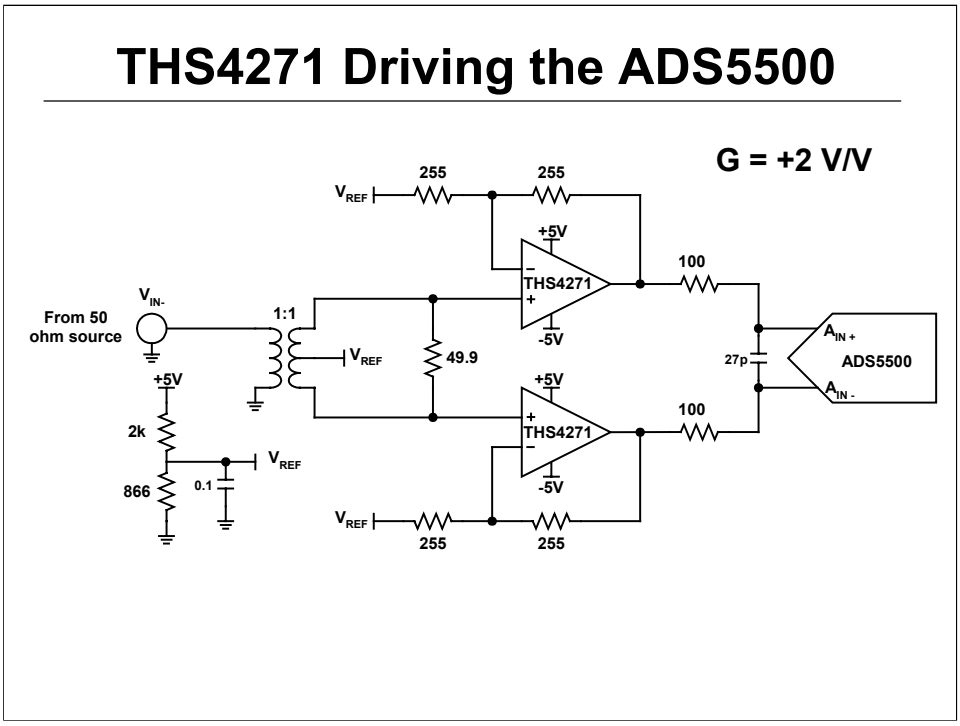


Shown above is the THS4502 driving the ADS5500 with 10MHz input tone. The SNR of the system is the same as the ADC by itself, but the harmonic performance is limited by the op amp circuit.

The op amp is used to convert the single-ended input signal from a 50 source generator to differential to drive the data converter. A high-order (8th order eliptical) low-pass filter is used between the signal source to clean up the harmonics generated there.

The circuit was built on the ADS5500 EVM. You may note that fairly high value resistors (392Ω) are used between the op amp and ADC and no capacitor. This was done to reduce the SNR and maintain the highest possible distortion performance. Lower value resistors and capacitors were tried along with LC filers, but the performance was best as shown.

The ADS5500's distortion performance is extremely good and presents a challenge for drive amplifier solutions at higher frequencies.



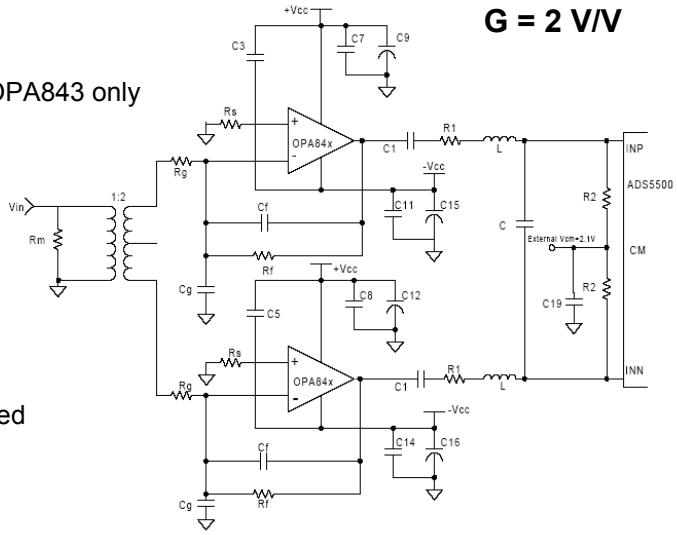
This THS4271 circuit was used to benchmark this single ended VFB amp against the fully differentials and current feedback amplifiers. The THS4271 is a 1200 MHz amplifier with 1000 V/microsecond slew rate, and 2.8 nanovolts per root hertz noise.

OPA84x Driving the ADS5500

G = 2 V/V

For OPA842 & OPA843 only

Rm = 68.8 ohm
Rg = 390 ohm
Rf = 806 ohm
C1 = 1000 pF
R1 = 13 ohm
L = 0.91 µH
C = 2.2 pF
R_2 = 270 ohm
C_f and C_g not used

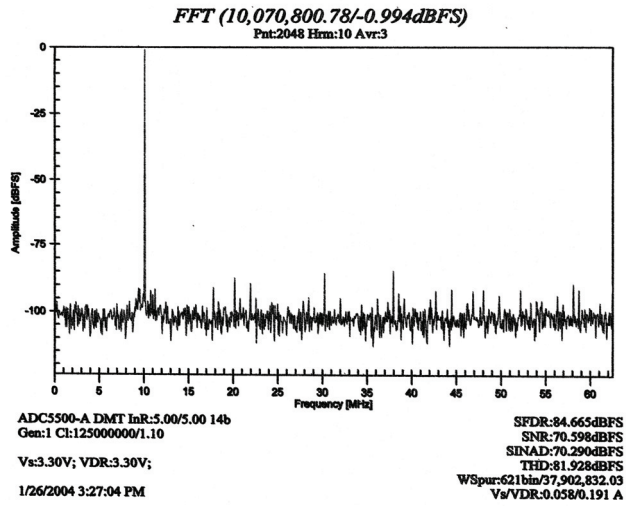


Configuration shown above is the recommended method for driving the ADS5500 with single operational amplifier in differential configuration.

It can be separated in 4 blocks: the single-ended to differential conversion, the amplification by the amplifier, the filter stage and the converter.

- The single-ended to differential conversion is realized with a 1:2 transformer. The resistor R_m from input to ground is set so that the source sees a 50ohm matched impedance.
- The amplification stage is realized through two single amplifiers forming an inverting differential circuit. For unity gain stable amplifier, only R_f and R_g resistors are needed. For decompensated amplifier such as the OPA843, OPA846 and OPA847, if used at a low gain, the low frequency gain is set by R_f and R_g and the high frequency gain is set by C_f and C_g. Using a decompensated amplifier at a low gain allows for improved SFDR. The amplifiers are operation from ±5V supplies.
- The filter stage is realized using “RLC Filter Design for ADC Interface Applications” application note from Michael Steffes. It allows limiting the noise power bandwidth of the amplifier to the desired bandwidth and a more agressive attenuation of the 3rd-order harmonic distortion at the high end of the analog input range.
- The last stage is the converter. It is operating from +3.3V supply.

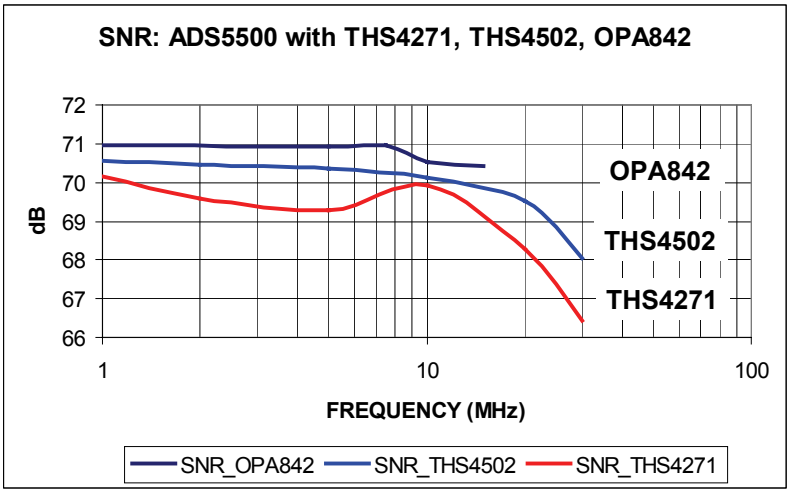
OPA842 Driving the ADS5500



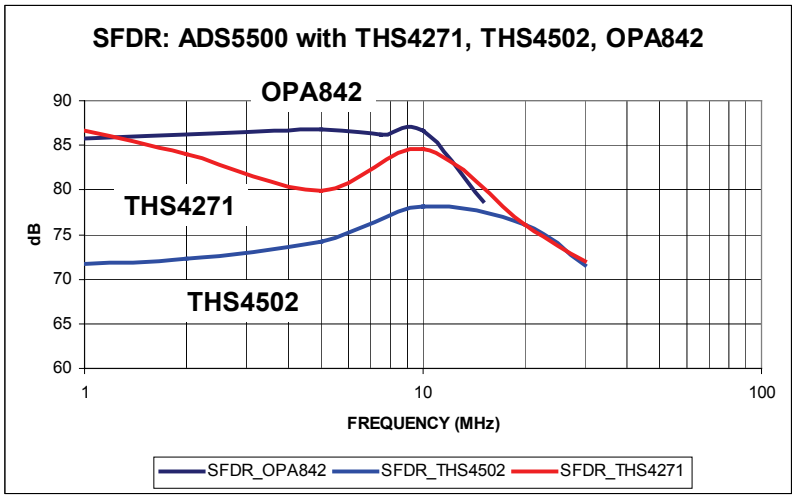
This slides shows the OPA842 driving the ADS5500 using the previously mentioned method. At 10MHz, SNR is 70.6dB and SFDR is 84.6dBFs for the system OPA842, 45MHz RLC Filter, ADS5500. This is down from 72dB SNR and 87dBFs SFDR for the ADS5500 alone.

In the tested configuration, each amplifier sees an effective load of about 260 ohm.

Summary of Available ADS5500 Op Amp Drive Solutions



Summary of Available ADS5500 Op Amp Drive Solutions



Driving the ADS5500 Summary

- Recommended Operational Amplifiers for use with ADS5500
  - DC-to-15 MHz operation (THS4503)
  - 0.1-to-15MHz operation (OPA842) (Both SNR and SFDR performance maintained)
  - 1-to-30 MHz operation (OPA847) (Both SNR and SFDR performance maintained)
  - 1-to-100MHz operation (OPA695) (SNR performance maintained over range)
  - Also consider: THS3202, THS3201, THS9000
- Transformer Coupled – dual transformer design to improve symmetry and CMRR (From ~5 MHz to 225 MHz).

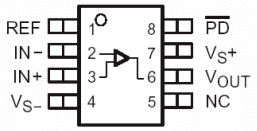
Testing is under way for OPA847 and OPA695 driving the ADS5500.

THS4225/6: Power-Down Mode

FEATURES

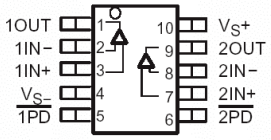
- Rail-to-Rail Output Swing
- - VO = -4.8/4.8 (R_L = 2 k)
- High Speed VFB
- - 230 MHz Bandwidth (-3 dB, G= 1)
- - 975 V/µs Slew Rate
- Ultra-Low Distortion
- - HD2 = -90 dBc (f = 5 MHz, R_L = 499)
- - HD3 = -100 dBc (f = 5 MHz, R_L = 499)
- High Output Drive, IO = 100 mA (typ)
- Excellent Video Performance
- - 40 MHz Bandwidth (0.1 dB, G = 2)
- - 0.007% Differential Gain
- - 0.007° Differential Phase
- Wide Range of Power Supplies
- - VS = 3 V to 15 V
- Power-Down Mode (THS4225/6)
- Evaluation Module Available

THS4225
D, DGN, OR DGK PACKAGE
(TOP VIEW)



NC − No internal connection

THS4226
DGQ PACKAGE
(TOP VIEW)



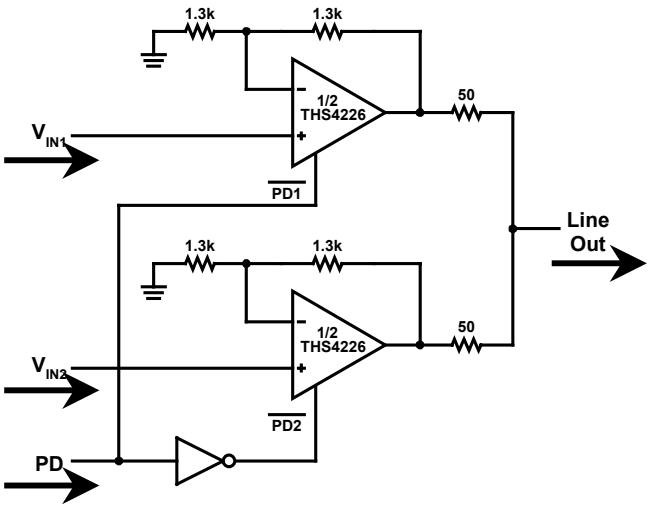
Multiplexing analog signals

Op amps with power-down capability can be used for various applications including multiplexing multiple signals to one line. The THS4225 (single) and THS4226 (dual) are high-speed voltage feedback op amps suitable for such use. The THS4226 is tested in the following example.

DESCRIPTION

The THS4222 family is a set of rail-to-rail output single,and dual low-voltage, high-output swing, low-distortion high-speed amplifiers ideal for driving data converters, video switching or low distortion applications. This family of voltage feedback amplifiers can operate from a single 15-V power supply down to a single 3-V power supply while consuming only 14 mA of quiescent current per channel. In addition, the family offers excellent ac performance with 230-MHz bandwidth, 975-V/µs slew rate and harmonic distortion (THD) at –90 dBc at 5 MHz.

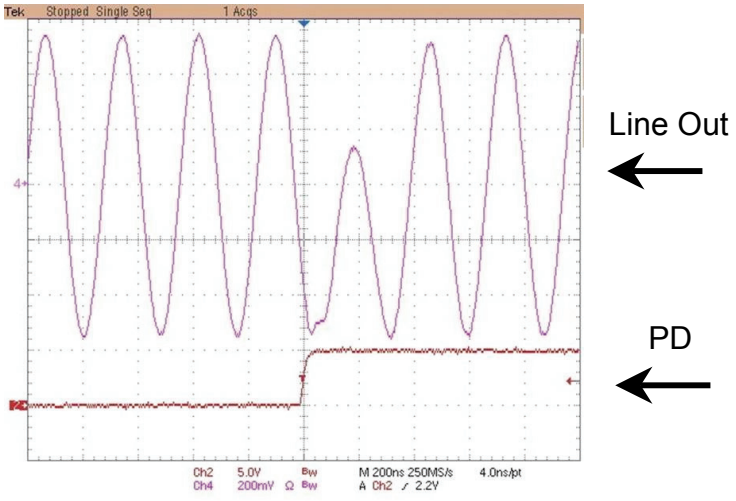
Example Circuit: Line Switch



The circuit shown could be used for a single ended output line buffer for applications like switching between two sources. Video multiplexing is a typical application.

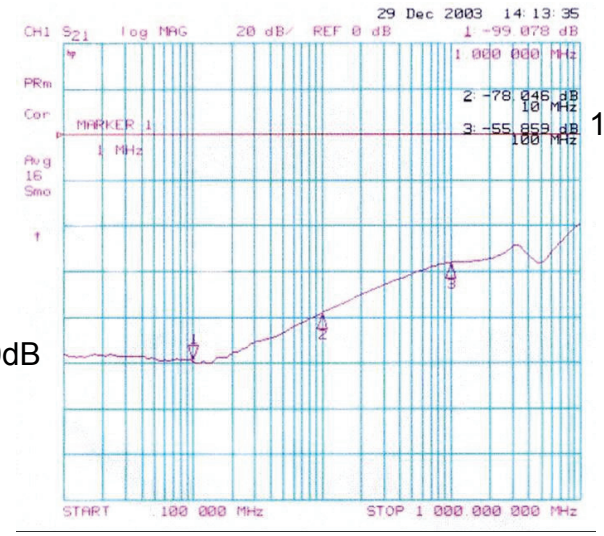
The 1.3kohm resistance is recommended by the datasheet for the THS4226 for gain of 2, and optimal flatness in the frequency.

Switching Glitch



Depending on the instant when the amplifiers are switched, glitches of different shapes and characteristics occur at the output due to the finite time for one op amp to power-down and the other op amp to power-up. The graphic shows a typical transition waveform at the output with a 1Vp-p 3.6MHz tone applied to the input of the amplifiers.

Crosstalk To Power-Down Amp



20dB/div

100kHz to 1GHz

-100dB

The graph above shows the cross-talk from the active amplifier to the power-down amplifier over the frequency range from 100kHz to 1gHz. The scale is 20dB per division. Below 1MHz the cross-talk is around -100dB.

High-Speed Op Amps with Power-Down

Voltage Feedback

Device	# of Channels
OPA690	1
OPA2690	2
OPA3690	3
THS4215	1
THS4226	2
THS4275	1
OPA847	1

Fixed Gain

OPA692	1
OPA3692	3
OPA693	1

Current Feedback

Device	# of Channels
OPA695	1
OPA683	1
OPA684	1
OPA3684	3
OPA691	1
OPA2691	2
OPA3691	3
THS3115	2
THS3125	2
THS3095	1
THS3096	2

Listed are some high-speed voltage and current op amps available from TI that offer power-down modes. This list is not exhaustive, and is meant as an example of product available.

Due to the fact that current feedback op amps can be biased on by higher amplitude input signals, they may not be suitable for some applications. As always, testing is required to prove the suitability of any amplifier in your system.

Transconductance Amplifier Design

Transconductance Applications

- High frequency (>30MHz) filters
- Laser drivers
- Line drivers
- High speed comparators
- DC restore

Transconductance Definition

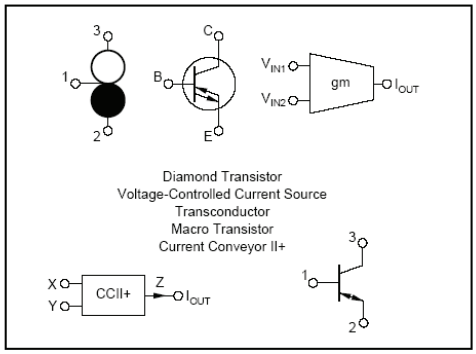


FIGURE 1. Symbols and Terms.

- Regardless of its depiction, an OTA combines:
  - high-input impedance (B-input),
  - low-input/output impedance (E- input)
  - high impedance current source output (C-output).

OTA – *Operational Transconductance Amplifier*
Voltage in – Current out

The transconductance element provides an output current proportional to the input voltage.

There are several representation and nomenclature for it:

- Voltage-Controlled Current Source
- Diamond Transistor
- Transconductor
- Macro Transistor
- Current Conveyor II+

In the rest of this discussion it will be referred as OTA and represented as a Diamond Transistor.

Regardless of its depiction and nomenclature, an OTA combines:

• a high-input impedance (B-input),

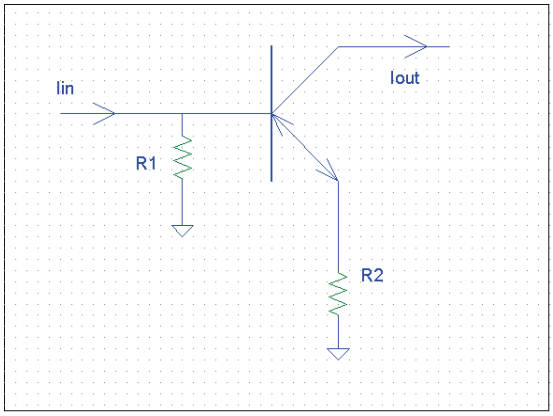
• a low-input/output impedance (E- input)

• a high impedance current source output (C-output).

One of the major points of emphasis is that the output stage is high impedance

Basic Gm Block

Current Amplifier



$$I_{Out} = \frac{R_1}{R_2} \cdot I_{In}$$

An OTA can be used as easily in Voltage-Mode or in Current Mode configuration.

Many of the same intuitive techniques that applies to transistor design apply to OTA circuits as well. However there are some important differences:

• The current flows out of the C-Output for positive B-E input voltage and conversely the current flows into the C-Output for a negative B-E input voltage.

• It is self biased (an advantage over discrete transistors)

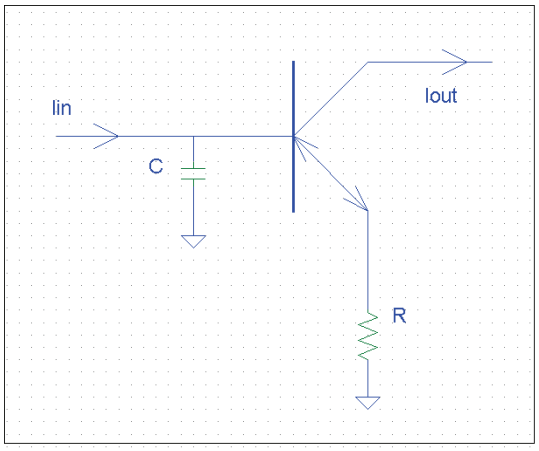
• It is more linear than discrete transistors

The basic blocks and the equations described here are all made in the current mode.

This first block represents a current amplifier set by external resistors R_1 and R_2.

Basic Gm Block

Current Integrator



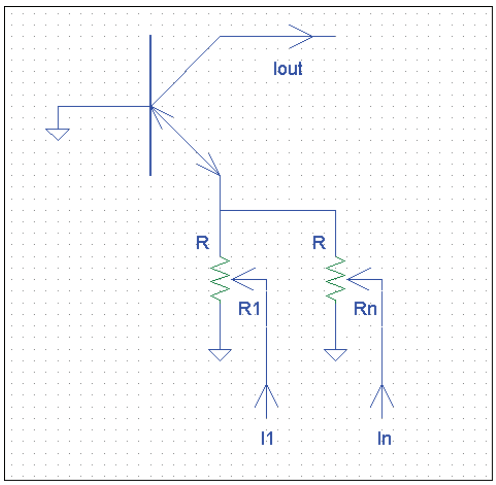
$$I_{Out} = \frac{1}{C \cdot R \cdot \int I_{In} dt}$$

A current integrator function can easily be realized as shown above.

A voltage integrator function will be used in the control-loop amplifier and is essential for state variable filters .

Basic Gm Block

◆ Weighted Current summer



$$I_{Out} = -\sum_{j=1}^{n} I_j \cdot \frac{R_j}{R}$$

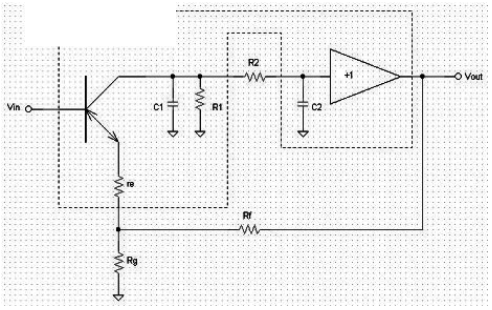
Current Summer where R=0

$$I_{Out} = -\sum_{j=1}^{n} I_j$$

A g_m stage in this configuration makes it really easy to add currents.

Adding resistors enables weighting each current input.

Current Feedback Amplifier



- Bandwidth adjustable through:
  - Iq
  - External C on the C-output.

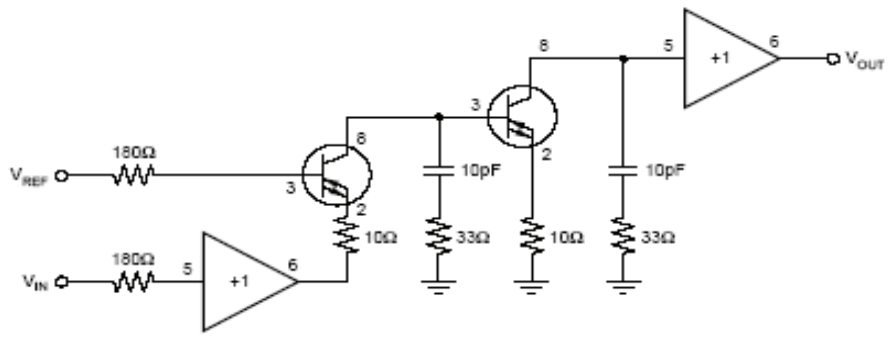
$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha \cdot \left(1 + \frac{R_F}{R_G}\right)}{1 + \left(1 + \frac{R_F}{R_G}\right) \cdot \frac{1}{g_m \cdot R_1} \cdot \left[1 + s\left(R_1C_1 + R_1C_2 + R_2C_2\right) + s^2 R_1 R_2 C_1 C_2\right]}$$

Going on to more advanced use of the OTA in combination with a buffer.

A combination of Buffer with OTA is offered in the OPA660 device.

This schematic is showing both parasitic capacitance and output impedance for E-input, C-Output and Buffer.

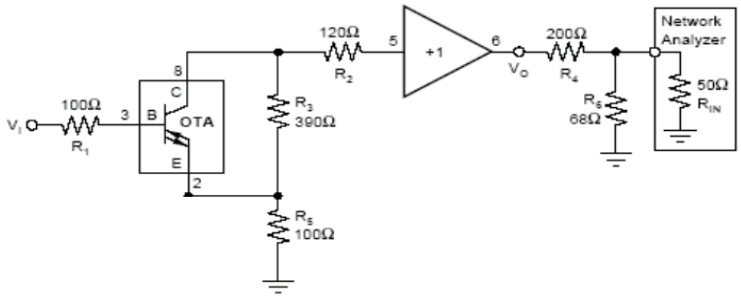
Control-Loop Amplifier



Using the basic g_m blocks shown earlier, it is possible to design other types of amplifiers that can fit your own requirement.

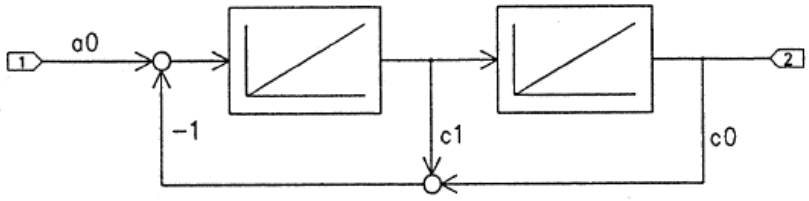
The circuit shown uses 2 OPA660 and combines a differential input and 2 voltage integrators. The output is finally buffered to offer low output impedance.

Closed-Loop OTA



- Built with OPA660 offers 750MHz bandwidth
- Iq = 12mA
- Buffer Stage removes final load from gain equation

State Variable Filters

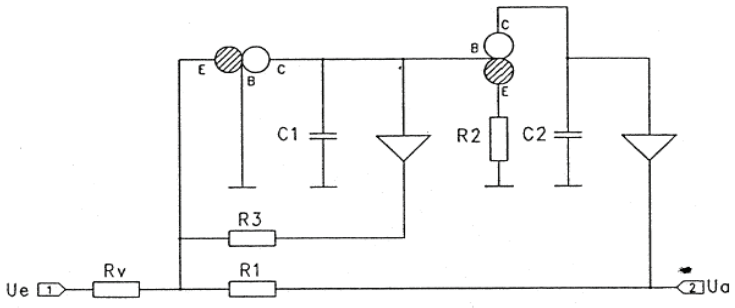


- Very flexible filter, good performance, low sensitivity
- Low-Pass Transfer Function shown

The state variable filter or KHN filter are extremely flexible, have good performance and low sensitivities. As transconductance amplifiers are ideal to drive capacitive load, this filter topology makes it a good combination.

A Low-Pass Filter is shown, High-Pass and Band-Pass filter also available from same configuration.

State Variable Filters



- Using both Buffer and OTA of OPA660
- Use of Buffers allows voltage mode
- Current mode also possible

This circuit is using 2 OPA660 comprising 2 OTAs stage and 2 Buffers. Each OTA is used as a voltage integrator and the buffer are placed in the feedback loop, allowing voltage-mode feedback. Current mode feedback can be implemented using OTA.

State Variable Filters

$$H(s) = \frac{a_0}{s^2 + c_1 s + c_0} = -\frac{R_1}{R_v} \frac{1}{1 + sC_2\frac{R_1 R_2}{R_3} + s^2 C_1 C_2 R_1 R_2}$$

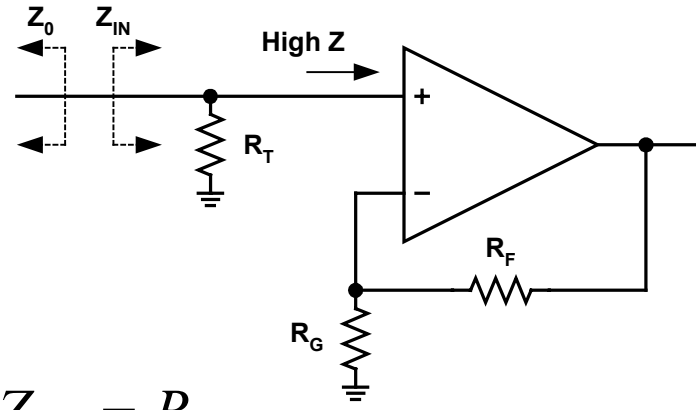
$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}$$

$$Q = \sqrt{\frac{C_1}{C_2}} \frac{R_3}{\sqrt{R_1 R_2}}$$

- 2nd order Low-Pass Filter equation shown for previous schematic

Back Matching Controlled Impedances

Non-Inverting Input Termination



$$Z_{IN} = R_T$$

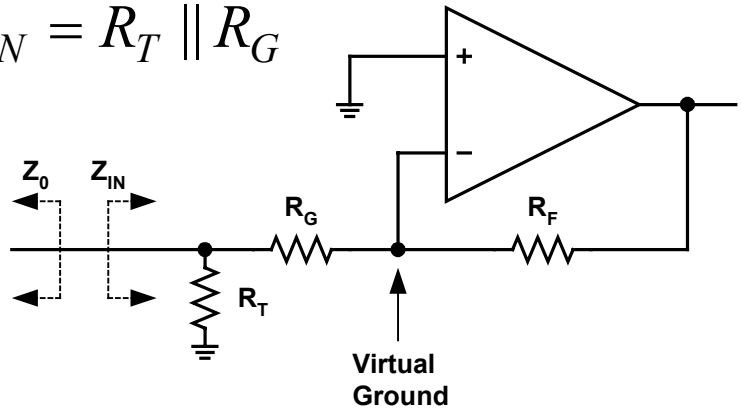
Double termination or back matching, where the source and load impedance match the characteristic impedance of the line (Z_0), is used to reduce line reflections. This is particularly important when transmitting pulses, square waves, or any signal with a fast transition.

The non-inverting op amp configuration is very simple to terminate. Normally the input impedance is very high, at least 10's of k ohms to meg ohm values, and can be ignored when compared to typical line impedance values of 50O to 100 O. In this case, R_T should be made equal to the Z_0.

Parasitic input capacitance is present at the input, and can become an issue at high frequencies. A small resistor (such as 25-50 ohms) in series with the input (after R_T) helps isolate the capacitance of the non-inverting input. This same technique is also used when cascading amplifiers, to prevent instability in the driving amplifier.

Inverting Input Termination

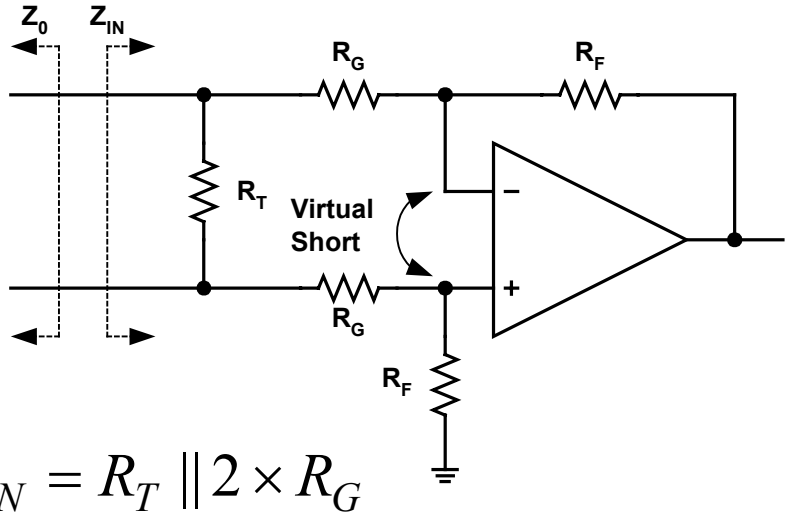
$$Z_{IN} = R_T \,||\, R_G$$



In the inverting op amp configuration, the action of the amplifier drives the negative input terminal to ground potential (virtual short to the grounded non-inverting input). In this case, the input impedance is seen as R_T || R_G.

At higher gains (i.e. G=-10V/V), R_G can be set to the value required for termination, and R_T can be eliminated. This is because R_F is large enough to not load the output stage of the amplifier (i.e. R_G = 50 ohms, and R_F =500 ohms when G=10V/V).

Differential Input Termination

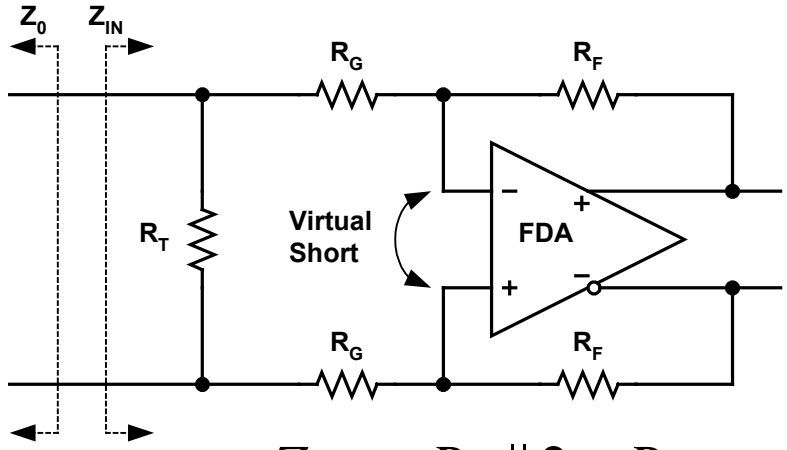


$$Z_{IN} = R_T \,||\, 2 \times R_G$$

Analysis of the differential op amp circuit is similar to the inverting op amp configuration. In negative feedback, the amplifier drives the voltage across its input terminals to zero. This is called a virtual short. In this case, the input impedance is seen as R_T || 2xR_G.

Remember to think differentially. It is important to view the system as differential and not try to analyze each input individually.

Differential FDA Input Termination

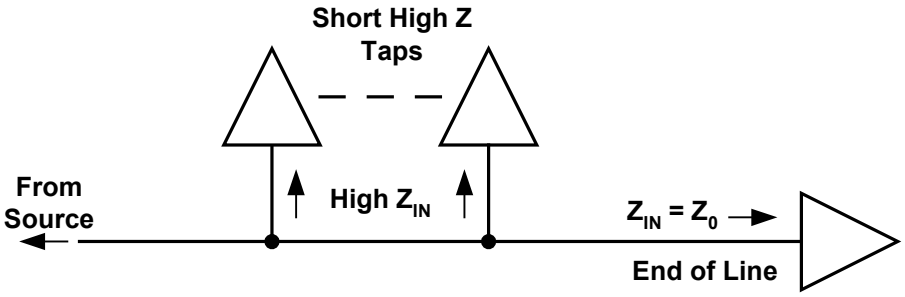


$$Z_{IN} = R_T \,||\, 2 \times R_G$$

The analysis of input Fully-Differential op amp (FDA) is the same as the differential op amp configuration with single-ended output. In negative feedback, the amplifier drives the voltage difference across its input terminals to zero (virtual short), and the differential input impedance is seen as R_T || 2xR_G.

At higher gains (i.e. G=-10V/V), 2 x R_G can be set to the value required for termination, and R_T can be eliminated. This is because R_F is large enough to not load the output stage of the amplifier (i.e. R_G = 50 ohms, and R_F =500 ohms when G=10V/V to terminate a 100 ohm line).

Multi-Drop Line Receivers

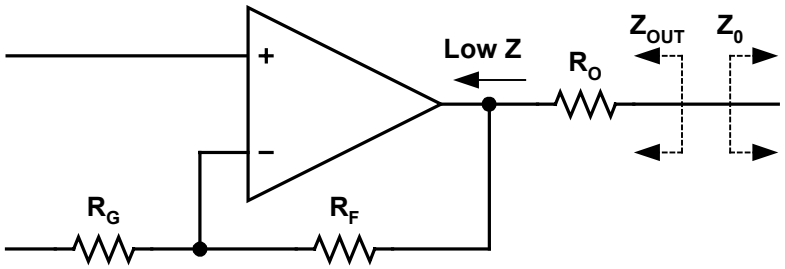


Terminate at the far-end of the line with the characteristic impedance of the line using short, high-impedance stubs for the intermediate drops

In applications where multiple receivers are placed on the line, the line should be terminated at the far-end of the line with the characteristic impedance of the line. Intermediate drops should be short high impedance stubs.

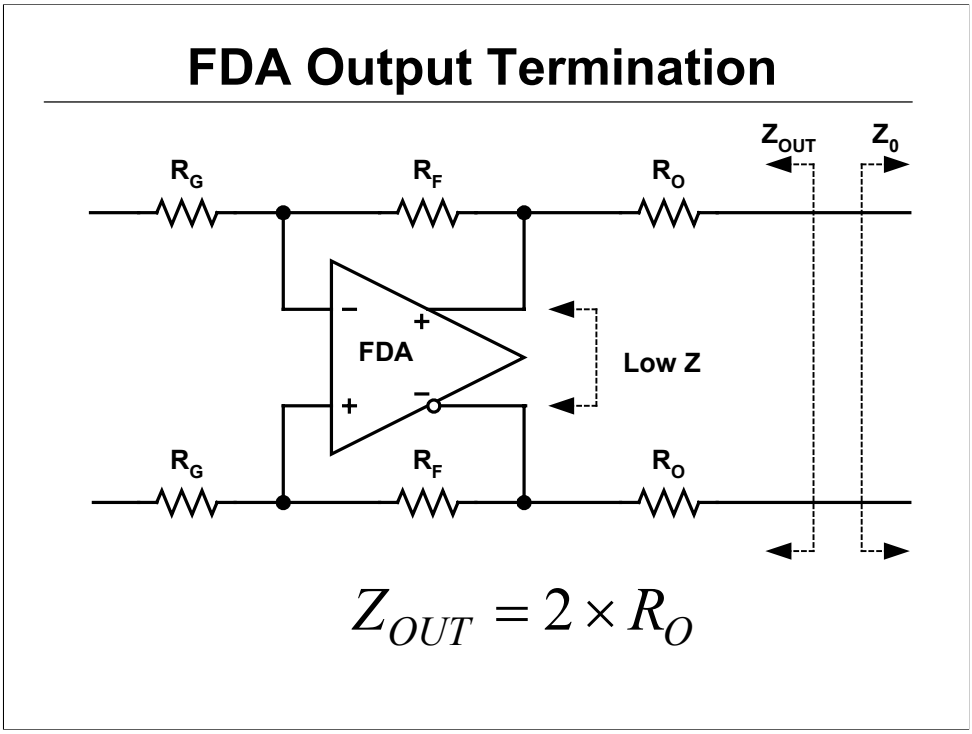
If the taps are op amps, then parasitic input capacitance is present at the input, and can become an issue at high frequencies. A small resistor (such as 25-50 ohms) in series with the input (after R_T) helps isolate the capacitance of the non-inverting input.

Single Ended Output Termination



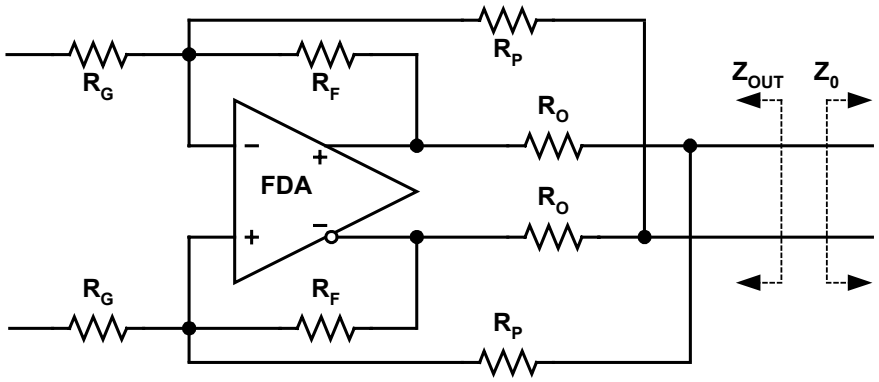
$$Z_{OUT} = R_O$$

Whether inverting, non-inverting, or differential, the output impedance of an op amp is very low while the amplifier is active. Output impedance is set by the value of R_O inserted in series with the output.



Fully-Differential op amps drive the line differentially requiring differential output termination. While the amplifier is active, the output impedance is set by the value of R_O inserted in series with each output.

FDA Active Output Termination



$$Z_{OUT} = \frac{2R_O R_P}{R_P - R_F + R_O}$$

Using positive feedback, the amplifier can be used to provide active termination. The positive feedback makes the output resistor appear to be a value larger than what it actually is when viewed from the line. Still, the voltage dropped across the resistor depends its actual value resulting in increased efficiency.

The output impedance of the circuit as seen from the line is given by the equation:

$$Z_{OUT} = \frac{2R_O R_P}{R_P - R_F + R_O},$$

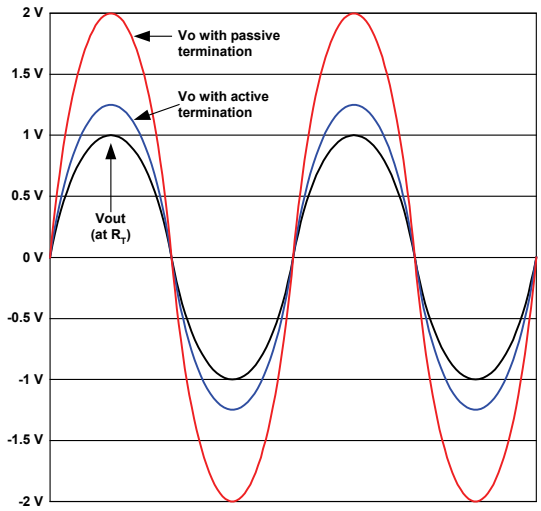
The gain to the load termination (R_T, not shown) is given by:

$$\frac{R_F}{R_G} \times \frac{1}{\frac{2R_O + R_T \| 2R_P}{R_T \| 2R_P} - \frac{R_F}{R_P}}$$

Design is easily accomplished by first choosing the value of R_F and R_O. Then calculate the required value of R_P to give the desired Z_0. Then calculate R_G for the required gain.

Reference AP Note number SLOA054 on Active Termination.

Example: Active Termination



Reduces Power Supply Requirements

Power Savings: 69%

Active Termination Example:

Given you want a gain of 1 to the far end of the cable load termination resistor (R_T), a 100Ω line, and you pick R_F = 1kΩ and R_O = 10Ω. The proper value for Z_0 and R_T is, of course, 100Ω.

Rearranging the equation to solve for R_P:

$$R_P = \frac{Z_O(R_F - R_O)}{Z_O - R_O} = \frac{50\Omega(1k\Omega - 10\Omega)}{50\Omega - 10\Omega} = 1237.5\Omega .$$

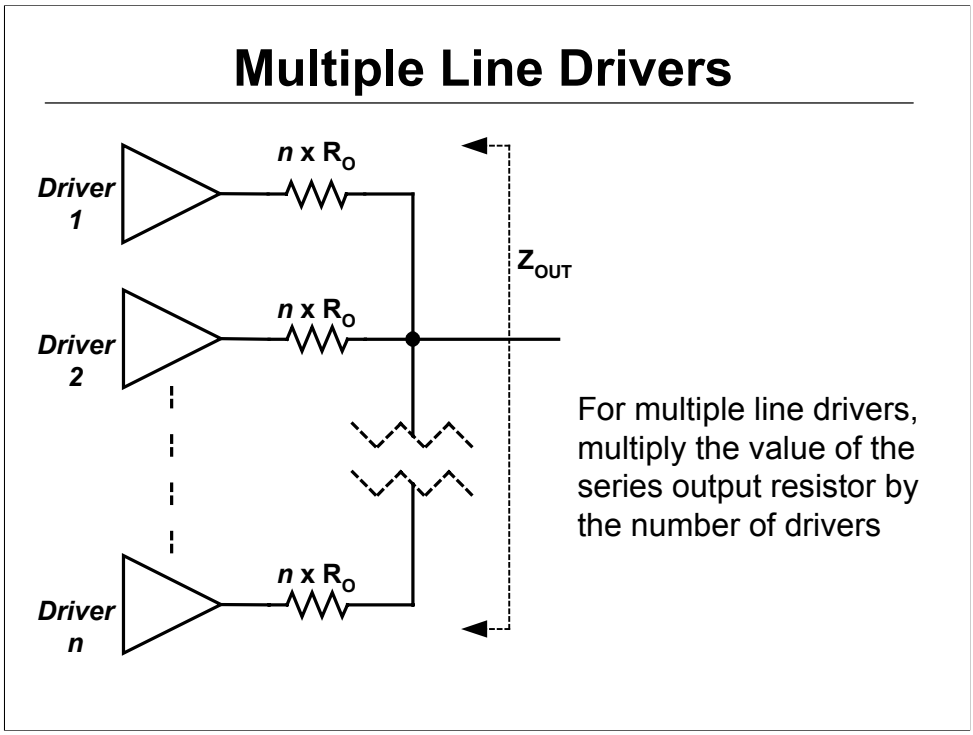
Then rearranging the gain equation:

$$R_G = \frac{R_F}{A} \times \frac{1}{\frac{2R_O + R_T \parallel 2R_P}{R_T \parallel 2R_P} - \frac{R_F}{R_P}} = \frac{1k\Omega}{\frac{20\Omega + 100\Omega \parallel 2475\Omega}{100\Omega \parallel 2475\Omega} - \frac{1k\Omega}{1237.5\Omega}} = 2500\Omega$$

The circuit is built and tested with the nearest standard values to those computed above: R_F = 1KΩ, R_P = 1.24kΩ, R_G = 2.49kΩ, R_T = 100Ω, and R_O = 10Ω. Compare the output voltage waveforms with active termination and passive termination. For passive termination: R_F = 1KΩ, R_P= open, R_G = 499Ω, R_T = 100Ω, and R_O = 50Ω.

With passive termination, 20mW of power is dissipated in the output resistors as opposed to 6.25mW with active termination. 69% less power is wasted with active termination.

Another feature about active termination that is very attractive, especially in low-voltage applications, is the effective increase in output voltage swing for a given supply voltage.



When using multiple amplifiers to drive the same line, the resistance seen looking in from the line is the parallel combination of the output resistors.

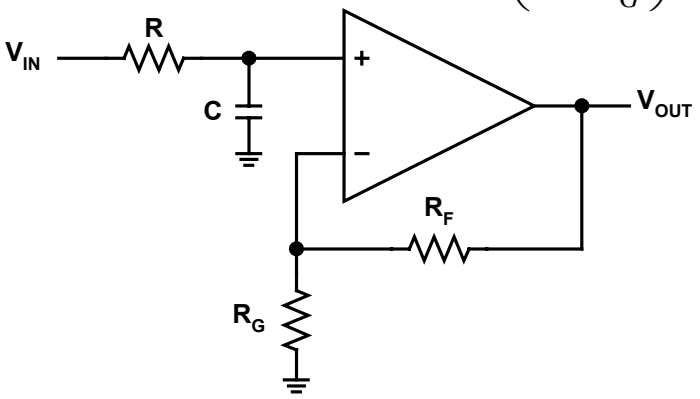
$Z_{out} = R_{Out0} \,||\, R_{Out1} \,||\, R_{Out2} \ldots R_{Outn}$

Note: Drivers should be co-located on the same board.

Low-Pass Topologies

Real Poles: RC at Input

$$H_{(f)} = \left(1 + \frac{R_F}{R_G}\right)\frac{1}{1 + j2\pi fRC}$$



Low-pass filtering is a mainstay of over-sampling ADC anti-aliasing filter design. Real and complex poles are simple to create with op amps.

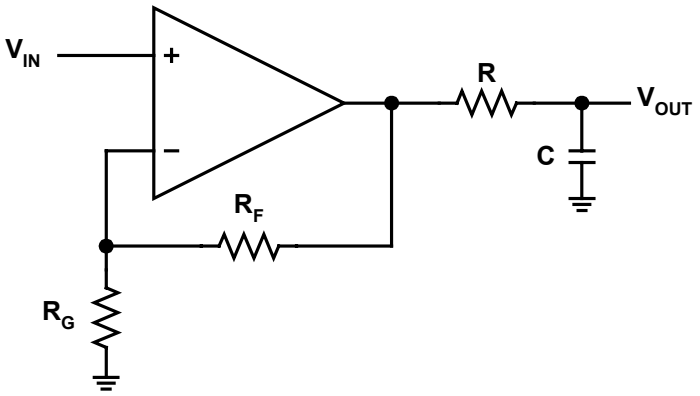
Real poles can be easily created in an op amp circuit by using resistors and capacitors (RC). Placing an RC on the input creates a passive low-pass filer. A real pole is created in the s-plane with cut-off, or -3dB, frequency equal to $\frac{1}{2\pi RC}$.

Note: bias current draw through R can cause DC offset. To limit this, R should be limited to small values (i.e. <1kohms).

Note: Capacitors values less than 10pF may need to be adjusted to account for stray capacitance in the circuit construction.

Real Poles: RC at Output

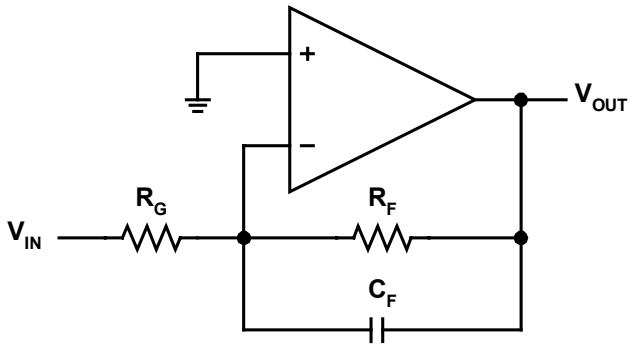
$$H_{(f)} = \left(1 + \frac{R_F}{R_G}\right)\frac{1}{1 + j2\pi fRC}$$



Placing an RC in the output creates a passive low-pass filer with a real pole located at $\frac{1}{2\pi RC}$.

Real Poles: RC in Feedback

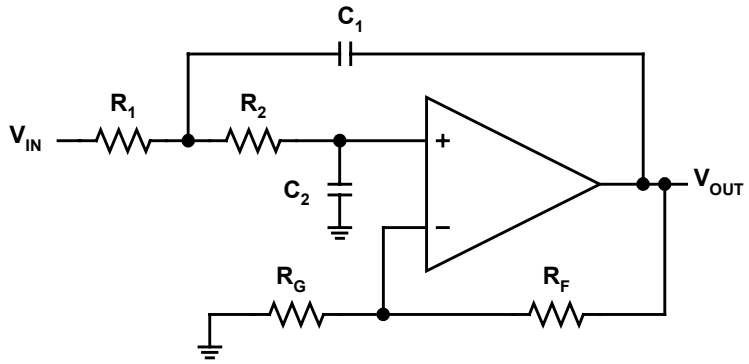
$$H_{(f)} = \left(\frac{R_F}{R_G}\right)\frac{1}{1 + j2\pi f R_F C_F}$$



Placing a capacitor across the op amp's feedback resistor creates an active low-pass filer. A real pole is created in the s-plane with cut-off, or -3dB, frequency equal to $\frac{1}{2\pi R_F C_F}$

The Sallen-Key and Multiple-Feedback (MFB) topologies are circuits used to create complex pole pairs, which are required for the classic filter types: Butterworth filters, Bessel filters, Chebyshev filters, and the like. Sallen-Key and MFB are discussed next.

Complex Poles: Sallen-Key



$$H_{(f)} = \frac{K}{-\left(\frac{f}{FSF \times f_C}\right)^2 + \frac{1}{Q}\left(\frac{jf}{FSF \times f_C}\right) + 1}$$

The circuit shown is the classic Sallen-Key topology and transfer function, where: $K = 1 + \frac{R_F}{R_G}$, $FSF \times f_C = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$, and $Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + R_1 C_2 (1-K)}$.

K sets the pass band gain, f_C is the cut-off frequency of the filter, *FSF* is a frequency scaling factor, and *Q* is the quality factor. $FSF = \sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}$, and

$$Q = \frac{\sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}}{2\,\mathrm{Re}}$$

where Re is the real part, and Im is the imaginary part of the complex pole pair.

Setting $R_1 = mR$, $R_2 = R$, $C_1 = C$, and $C_2 = nC$, results in: $FSF \times f_C = \frac{1}{2\pi RC\sqrt{mn}}$ and

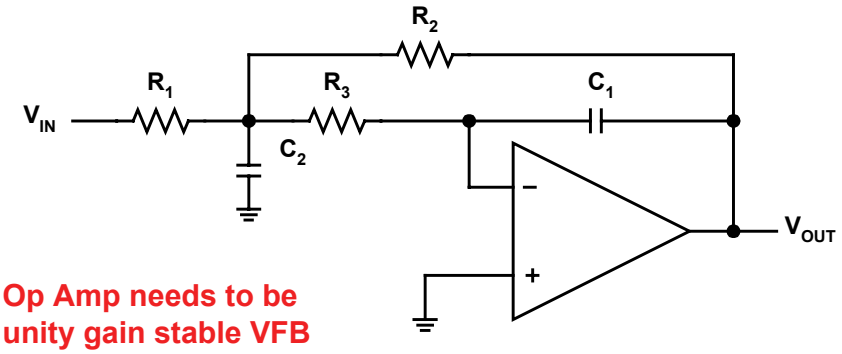
$$Q = \frac{\sqrt{mn}}{m + 1 + mn(1-K)}.$$

K and f_C are set by the pass band gain and the desired cut-off frequency of the application. *FSF* and *Q* are set by the type of filter being designed.

It is easiest to start the design by choosing standard capacitor values for C_1 and C_2. This gives a value for n. Then determine if there is a value for m that results in the required Q of the filter with the desired gain. If not, choose another capacitor combination and try again. Once a suitable combination of m and n are found, use the value for C to calculate R based on the desired f_C.It may take a few tries to give reasonable component values.

Alternately, you can solve the quadratic equation for Q, which makes it easier to find solutions for *m* & *n*.

Complex Poles: MFB



Op Amp needs to be unity gain stable VFB

$$H_{(f)} = \frac{K}{-\left(\frac{f}{FSF \times f_C}\right)^2 + \frac{1}{Q}\left(\frac{jf}{FSF \times f_C}\right) + 1}$$

The circuit shown is the classic Multiple-FeedBack (MFB) topology and transfer function, where: $K = -\left(\frac{R_2}{R_1}\right)$, $FSF \times f_C = \frac{1}{2\pi\sqrt{R_2 R_3 C_1 C_2}}$, and $Q = \frac{\sqrt{R_2 R_3 C_1 C_2}}{R_3 C_1 + R_2 C_1 + R_3 C_1 (-K)}$.

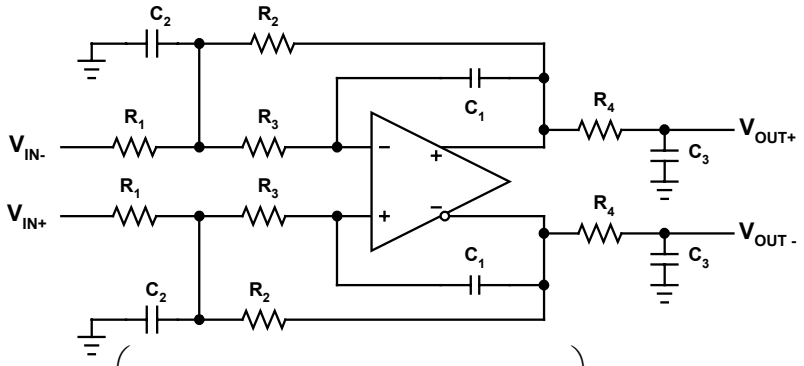
K sets the pass band gain, f_C is the cut-off frequency of the filter, *FSF* is a frequency scaling factor, and *Q* is the quality factor. $FSF = \sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}$, and $Q = \frac{\sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}}{2\,\mathrm{Re}}$ where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting $R_3=mR$, $R_2=R$, $C_1=C$, and $C_2=nC$, results in: $FSF \times f_C = \frac{1}{2\pi RC\sqrt{mn}}$ and. $Q = \frac{\sqrt{mn}}{1 + m(1-K)}$

Design is basically the same as for the Sallen-Key circuit. *K* and f_C are set by the pass band gain and the desired cut-off frequency of the application. *FSF* and *Q* are set by the type of filter being designed.

Start the design by choosing standard capacitor values for C_1 and C_2. This gives a value for n. Then determine if there is a value for m that results in the required Q of the filter with the desired gain. If not, choose another capacitor combination and try again. Once a suitable combination of m and n are found, use the value for C to calculate R based on the desired f_C.It may take a few tries to give reasonable component values.

Again, you can solve the quadratic equation for Q, which makes it easier to find solutions for *m* & *n*. This is left as exercise for the reader.

Complex Poles: MFB FDA



$$H_{(f)} = \left(\frac{K}{-\left(\frac{f}{FSF \times fc} \right)^2 + \frac{1}{Q} \frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{1}{1 + j2\pi f \times R_4 C_3} \right)$$

Shown is a fully-differential amplifier (FDA) utilizing the MFB architecture with a 3rd real pole added by the RC on the output along with the transfer function, where $K = \frac{R_2}{R_1}$,

$FSF \times f_C = \frac{1}{2\pi\sqrt{R_2 R_3 C_1 C_2}}$, and $Q = \frac{\sqrt{R_2 R_3 C_1 C_2}}{R_3 C_1 + R_2 C_1 + K R_3 C_1}$.

K sets the pass band gain, fc is the cut-off frequency of the filter, FSF is a frequency scaling factor, and Q is the quality factor. $FSF = \sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}$, and $Q = \frac{\sqrt{\mathrm{Re}^2 + |\mathrm{Im}|^2}}{2\,\mathrm{Re}}$, where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R_2 = R, R_3 = mR, C_1 = C, and C_2 = nC, results in: $FSF \times f_C = \frac{1}{2\pi RC\sqrt{n \times m}}$ and $Q = \frac{\sqrt{mn}}{1 + m(1+K)}$.

Design of the MFB is the same as before. *K* and f_C are set by the pass band gain and the desired cut-off frequency of the application. *FSF* and *Q* are set by the type of filter being designed.

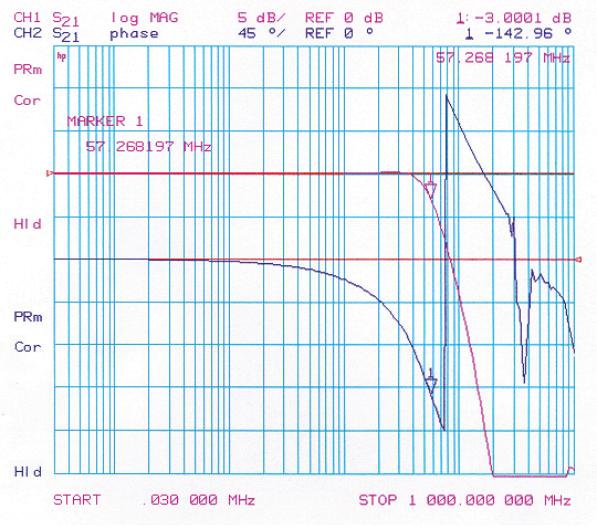
It is easiest to start the design by choosing standard capacitor values for C_1 and C_2. This gives a value for n. Then determine if there is a value for m that results in the required Q of the filter with the desired gain. If not try another capacitor combination and try again. Once a suitable combination of m and n are found, use the value for C to calculate R based on the desired f_C. It may take a few tries to give reasonable component values.

Solving the quadratic equation for Q helps to select the proper capacitor ratio (n) so that a valid resistor ration is more easily attained: Set n equal to or slightly larger than $2Q^2(1+K)$.

For n = 2Q^2(1+K), only one real value is found for m.
For n >> 2Q^2(1+K), two real values are found for m, one large, and the other approaching zero.
For n < 2Q^2(1+K), m is complex and is not physically realizable with a resistor.

R_4 and C_3 are chosen to set the real pole in a 3rd order filter. Care should be exercised with setting this pole. If R_4 is a low value, at frequencies above the pole frequency the series combination with C_3 will load the amplifier.

MFB FDA: 3rd Order Low Pass



The figure shows the gain and phase response of a 3rd order low-pass filter using the FDA circuit shown on the previous slide . The components used are: R_1 = 374Ω, R_2 = 374Ω, R_3 = 261Ω, R_4 = 25Ω, C_1 = 3.3pF, C_2 = 15pF, C_3 = 68pF, and the THS4500 fully-differential op amp. The result is flat response to about 30MHz, -3dB at 57.3MHz, and significant attenuation after that.

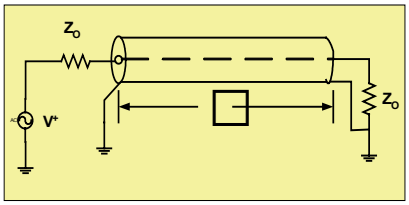
You may find FilterPro™ will make the design easier and faster for you. It is an active filter design utility that supports fully-differential op amps. It is available free via www.ti.com. Search for keyword filterpro.

http://focus.ti.com/docs/apps/catalog/resources/appnoteabstract.jhtml?abstractName=sbfa001a

Equalization Circuits

Frequency Equalization of Coaxial Cable

- **Cable Parameters**
  - **Frequency Dependent vs resistance parametric on length**
  - **Attenuation is linear up to skin effect than turns lossy at high frequencies**
  - **Characteristic Impedance is always matched for optimum performance and transfer, leaving the real loss of the cable**



$$V_O = V^+ e^{-\gamma l}$$

$$\gamma = (R + j\omega L)(G + j\omega C)$$

Normally R and G are assumed to be zero, but with true cables there is a loss term (and additional reactive term) due to the skin effect and the length of cable attenuation.

Understanding transmission lines is complicated by difficult math and theories. Reducing the math to simple terms allows one to show the cable loss in terms of a linear approximation that to design equalization curves with high-speed amps.

The important terms to separate are shown in the slide above and the next couple of slides.

Frequency Plot of Coaxial cable parametric on length

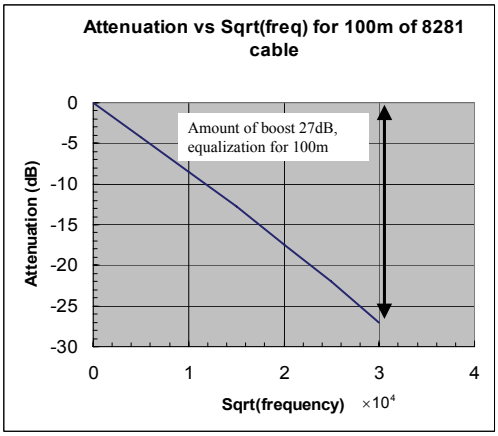
◆ Assuming no reflections and match termination a cable can be modeled as a function of frequency and length

$$Vo = V^{+} \cdot e^{-k'\sqrt{f}\ell} \cdot e^{-jk'\sqrt{f}\ell}$$

◆ Plot shows cable attenuation in log to log scale for Belden 8281 cable at a frequency of 300MHz and length of 100M

◆ At lower frequencies the length increases and the attenuation decreases.

◆ Equalization will match identically for a given length and frequency.



k'=1.02133? 10^{-6} and l=in meters

Developing the equation to describe for a lossy cable transfer function where we isolate the length of cable for a particular frequency is shown below.

Assuming no reflection at the load (matched termination for the characteristic impedance) the equation is $V_o = V^{+}e^{-\gamma\ell}$

Where γ2=(R+jωL)(G+jωC)

Normally R and G are assumed to be zero, but in this case there is a loss term (and an additional reactive term) due to the skin effect.

Assuming the skin depth is small compared with the radius of the inner conductor this term is then described by $Z_i = R_i + jR_i$

Where $R_i = \frac{1}{r}\sqrt{\frac{\mu}{4\pi\sigma}} \cdot f^{1/2} = k \cdot f^{1/2}$

$$Vo = V^{+} \cdot e^{-\frac{R_i}{2Z_o}\cdot\ell} \cdot e^{-j\frac{R_i}{2Z_o}\ell} \cdot e^{-j\omega\sqrt{LC}\cdot\ell}$$

The expression for Vo is $Vo = V^{+} \cdot e^{-k'\sqrt{f}\ell} \cdot e^{-jk'\sqrt{f}\ell}$

Where the last exponential term is a linear phase term representing the delay of the cable. Ignoring the last term and substituting kf1/2 for Ri results in

Where $k' = \frac{k}{2Z_o}$

Solving for k' by substituting the values found in a Belden cable tables

For Belden 8281 cable L approximately equal to 370nH/m therefore

$$k' = \frac{1}{2 \cdot Z_o \cdot r}\sqrt{\frac{\mu}{4\pi\sigma}} = \frac{1}{2 \cdot 75 \cdot \left(394 \cdot 10^{-06}\right)}\sqrt{\frac{4\pi \cdot 10^{-7}}{4\pi\left(5.8 \cdot 10^{7}\right)}}$$

$$\frac{R_i}{\omega L} = \frac{45.5}{\sqrt{f}}$$

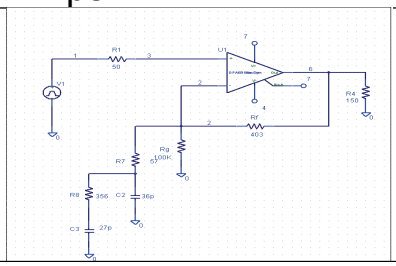
So for frequencies above 200Khz Ri/ωL is << 1 and the expression for gamma can be approximated.

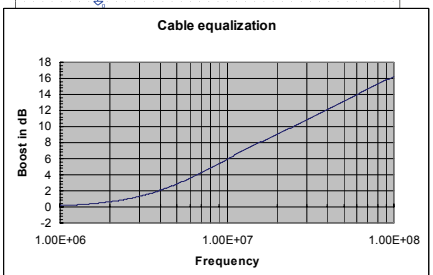
$$\gamma \cong j\omega\sqrt{LC} + \frac{jR_i}{2Z_o} + \frac{R_i}{2Z_o}$$

Cable Equalizer with High-Speed Current Feedback Amps

Equalizing Signals to match cables

- Match the cable roll-off for resistive loss over long length of cables results in taking the inverse of the previous plot.
- Can match the response for a given length cables at a specified frequency
- Limitation results from the amplifiers noise floor, dynamic range and frequency response.
- Caution layout parasitic components can alter the poles at high frequencies.
- Zero's are added by altering the gain of the non-inverting amplifier. This requires to match to a given length of cable.



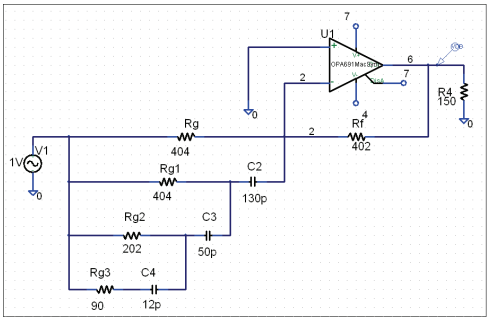


Device	BW-3db G=+2,(MHz)	SR (V/µs)	Iout (mA)	$V_{n\text{-}1MHz}$ (nV/√Hz)	Iib (uA)	V_{IO} (mV)	$I_{S/ch}$ (mA)	THD_{5MHz} (dB)	V_S (V)	Package	1k Suggested Single
OPAx691	**350**	**2100**	**190**	**2.5**	**15**	**0.5**	**5.1**	**71**	**+5 to ±5**	**D,DBV**	**$1.45**

Here each RC network is in parallel to a R resistance. This R sets the gain for the circuit and when the amplifier is a CFB the bandwidth stays constant over a limit range. At higher frequencies an additional zero is added causing increase the gain of the circuit. The plot shows a gain of 16dB is added with this circuit for a 100MHz. For higher frequencies and more boost add additional RC networks to match the required loss of the cable.

Inverting Equalizer Circuit

- Inverting configuration allow for slightly lower input referred noise
- Here each RC combination inserts a zero by shorting the previous resistor value to increase the gain.
- Limitations are the imput dynamic range.

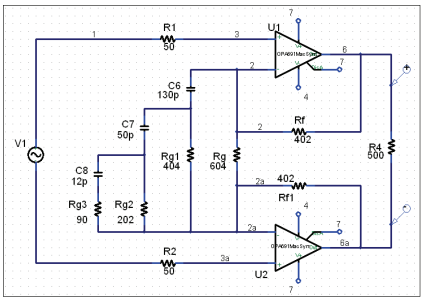


Device	BW-3db	SR	Iout	$V_{n\text{-}1MHz}$	Iib	V_{IO}	$I_{S/ch}$	$T\text{-}HD_{5MHz}$	V_S	Package	1k Suggested
	G=+1,(MHz)	(V/µs)	(mA)	(nV/√Hz)	(uA)	(mV)	(mA)	(dB)	(V)		Single
OPA695	**1700**	**4300**	**120**	**1.8**	**13**	**0.3**	**12.9**	**81**	**+5 to ±5**	**D,DBV,DBQ**	**$1.45**

Inverting stages provide lower noise. Each RC network is in parallel to a resistor which sets a zero in the response to give boost at the output. This circuit is intended for the terminating side of the cable.

Differential Cable Equalizer

- Differential amps provide twice the output swing and slightly lower noise specs for cable drivers.
- Current feedback used in the inverting mode supports a greater cable length and fix transmission frequency with lower noise.
- Discrete duals will have higher output current drive then differential amps



Here a dual with a common gain stage is used to set the output swing. Each RC network increases the gain by adding a zero in the response. Typically you can you use 2 to 3 RC networks for the boost, which is determined by the amount of cable roll-off.