PLL Fundamentals

Part 3: PLL Design

Dean Banerjee
Overview

• Frequency Planning
  – Number Theory Overview
  – Types of Frequency Plans
• Loop Filter Design
  – Choosing Loop Parameters
  – Tricks and Tips for Optimization
• Practical Things that Textbooks Won’t Tell You
  – Real World Component Values
  – Suggestions for Various Pins
  – PLL Debugging Tips
Less Known Divisibility Rules

- **Divisibility by 2, 4, & 8**
  - Even numbers are divisible by 2
  - Divisible by 4 if the last 2 digits are divisible by 4
  - Divisible by 8 if the last 3 digits are divisible by 8

- **Divisibility by 3 & 9**
  - A number is divisible by 3 if the sum of the digits is divisible by 3
  - A number is divisible by 9 if the sum of the digits is divisible by 9
  - 367218 is divisible by 9 since 3+6+7+2+1+8 is divisible by 9

- **Divisibility by 11**
  - A number is divisible by 11 if the sum of odd and even digits is divisible by 11
  - 12111 is divisible by 11 since 1-2+1-1+1 is divisible by 11
Least Common Multiple (LCM)

• This is the least number that is a multiple of a collection of two or more numbers
  – \( \text{LCM}(6,14) = 42 \)
  – \( \text{LCM}(A,B,C) = \text{LCM}( \text{LCM}(A,B) , C) \)
• This can be expanded to rational numbers
  – \( \text{LCM}(30.72 \text{ MHz} , 61.44 \text{ MHz}) = 61.44 \text{ MHz} \)
• A general technique for any fraction such as \( \text{LCM}( \frac{5}{3}, \frac{17}{12} ) \)
  • \( \frac{5}{3} \times A = \text{LCM}( \frac{5}{3} , \frac{17}{12} ) \)
  • \( \frac{17}{12} \times B = \text{LCM}( \frac{5}{3} , \frac{17}{12} ) \)
  • \( \frac{B}{A} = \frac{5/3}{17/12} = \frac{60}{51} = \frac{20}{17} \Rightarrow B = 20 \)
  • \( \text{LCM}( \frac{5}{3}, \frac{17}{12} ) = \frac{17}{12} \times 20 = \frac{85}{3} \)
Greatest Common Divisor (GCD)

- This is the greatest number that divides into two or more numbers
  - GCD(6,14) = 2
  - GCD(A,B,C) = GCD( GCD(A,B) , C)
- This can be expanded to rational numbers
  - LCM( 10 MHz , 21 MHz) = 1 MHz
- A general technique for any fraction such as GCD ( 5/3, 17/12 )
  - GCD( 5/3 , 17/12 ) x A = 5/3
  - GCD( 5/3 , 17/12 ) x B = 17/12
  - A/B = (5/3)/(17/12) = 60 / 51 = 20 / 17 => A = 20
  - GCD( 5/3, 17/12) = (5/3) / 20 = 1/12
Alternative Calculation Method

- Works for Non-Repeating Decimals
- Calculate LCM and GCD of 14.4 and 16.44
- LCM = $15 \times 64 \times 3 \times 2 \times 4 \times 4 \times 0.01 = 921.6$
  - $15 \times 14.4 = 921.6$
  - $64 \times 61.44 = 921.6$
- GCD = $0.01 \times 4 \times 4 \times 2 \times 3 = 0.96$
  - $14.4/15 = 0.96$
  - $61.44/64 = 0.96$

<table>
<thead>
<tr>
<th></th>
<th>14.4</th>
<th>61.44</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>1440</td>
<td>6144</td>
</tr>
<tr>
<td>4</td>
<td>360</td>
<td>1536</td>
</tr>
<tr>
<td>4</td>
<td>90</td>
<td>384</td>
</tr>
<tr>
<td>2</td>
<td>45</td>
<td>192</td>
</tr>
<tr>
<td>3</td>
<td>15</td>
<td>64</td>
</tr>
</tbody>
</table>
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## Types of Frequency Plans

<table>
<thead>
<tr>
<th></th>
<th>Fixed Frequencies</th>
<th>Variable Frequencies</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single Output</strong></td>
<td>Fixed Frequency Plan</td>
<td>Tunable Frequency Plan</td>
</tr>
<tr>
<td><strong>Multiple Outputs</strong></td>
<td>Simultaneous Frequency Plan</td>
<td>Not too Common</td>
</tr>
</tbody>
</table>
Traditional Tunable Frequency Method

- Phase Detector Frequency is fixed and the N divider changes
- Try to Optimize the Phase Detector frequency
  - Integer N PLL: Equal to the spacing, GCD(f₁, ..., fₖ)
  - Fractional N PLL: Can be made typically as large as f_{OSC} (i.e. Fden x GCD(f₁, ..., fₖ))
Other Tunable Frequency Method

- Each frequency can have its own phase detector frequency, VCO frequency, and channel divide value.
- Filter Optimization Tips …
  - Maximize phase detector frequency
    - Reduce fraction N/R to lowest terms
    - Equivalent to making $f_{PD} = \text{GCD}(f_{VCO1}, f_{VCO2}, f_{VCO3}, f_{OSC})$
  - Minimize variation of
    \[
    \frac{K\phi \cdot K_{vco}}{N}
    \]
  - Use Lower order Filters
Simultaneous Frequency Planning Techniques

- \( f_{VCO} = k \times \text{LCM}(f_1, f_2, f_3) \)
  - \( k = 1, 2, 3, \ldots \)
  - VCO Frequency may require that \( k > 1 \)
- \( f_{PD} = \frac{\text{GCD}(f_{VCO}, f_{OSC})}{c} \)
  - \( c = 1, 2, 3, \ldots \), where 1 is preferable
  - N counter and VCO Divider may require \( c > 1 \)
  - Fractional N can lower this value for \( c \)
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Loop Filter Design

- Need to solve for 3 Unknowns
  - T1
  - T2
  - C1+C2

\[ Z(s) = \frac{1 + C2 \cdot R2}{(Cl + C2) \cdot \left(1 + s \cdot \frac{Cl \cdot C2}{Cl + C2}\right)} = \frac{1 + T2}{(Cl + C2) \cdot (1 + s \cdot T1)} \]
Loop Bandwidth, Phase Margin, Gamma

Gain / Phase Margin

Closed Loop Gain

Phase Margin

Open Loop Gain
How Do I Pick Loop Bandwidth?

- Loop Bandwidth $\leq \frac{f_{PD}}{10}$
  - Violating this causes instability issues due to discrete sampling action of the phase detector
- Wider Loop Bandwidth $>$ Faster Lock Time, but Worse Spurs
- Choosing the loop bandwidth equal to the frequency where PLL noise and VCO noise are equal optimize the integrated phase noise (i.e. jitter, phase error, evm, …)
  - Actually, make about 25% wider to account for fact that loop filter is not a brick wall filter
  - This does not account for spurs
Minimum Integrated Phase Noise Bandwidth

Crossover = 50 kHz
Make BW = 50 kHz * 1.2

(Unshaped)
How Do I Pick Phase Margin?

• 70 – 80 degrees is for a very flat response and for minimum integrated phase noise
• 48 degrees (varies a little from design to design) is optimal for lock time
• Lower Phase Margin is good for slightly better spurs, especially for higher order filters
How do I Pick Gamma?

- Given a phase margin, Gamma can be estimated for optimal lock time, and typically this is best for spurs too.
- For some pathological cases involving partially integrated loop filters, gamma can be tweaked for a wider loop bandwidth

<table>
<thead>
<tr>
<th>Phase Margin</th>
<th>$\gamma$ for Fastest Lock Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>1.4</td>
</tr>
<tr>
<td>35</td>
<td>1.41</td>
</tr>
<tr>
<td>40</td>
<td>1.29</td>
</tr>
<tr>
<td>45</td>
<td>1.09</td>
</tr>
<tr>
<td>50</td>
<td>0.94</td>
</tr>
<tr>
<td>55</td>
<td>0.85</td>
</tr>
<tr>
<td>60</td>
<td>0.7</td>
</tr>
<tr>
<td>65</td>
<td>0.49</td>
</tr>
<tr>
<td>70</td>
<td>0.24</td>
</tr>
<tr>
<td>75</td>
<td>0.05</td>
</tr>
<tr>
<td>80</td>
<td>0.08</td>
</tr>
</tbody>
</table>
Apply the Constraints

- Apply Constraint that forward loop gain at loop bandwidth frequency is equal to 1

\[
\left| \frac{K_{PD} \cdot K_{VCO}}{N \cdot s} \cdot \frac{1 + T2}{s \cdot (C1 + C2) \cdot (1 + s \cdot T1)} \right|_{s = 2\pi \cdot BW} = 1
\]

- Set Phase Margin to Desired Value, \( \phi \)

\[
\phi = 180 + \tan^{-1}(2\pi \cdot BW \cdot T2) - \tan^{-1}(2\pi \cdot BW \cdot T2)
\]

- Apply Constraint that phase margin is maximized at loop bandwidth and define parameter, \( \gamma \)

\[
\gamma = \frac{1}{(2\pi \cdot BW)^2 \cdot T2 \cdot T1}
\]
What About Higher Order Filters?

• **3rd Order Filter**
  – Define T3/T1 Ratio as an additional constraint
  – Maximize value of C3 (closest to VCO)

• **4th Order Filter**
  – Define T3/T1 Ratio
  – Define T4/T3 Ratio
  – Choose C1 and C3 to maximize C4

• **Filter with C3, C4, R3, R4 Integrated**
  – No constraints to define
Possible Design Approach

Start with Minimum Jitter Design

Spurs too High?
1. Optimal Jitter Bandwidth
2. 2nd Order Filter
3. 70 Degrees Phase Margin

Lock Time too Slow?
1. Optimal Jitter Bandwidth
2. 2nd Order Filter
3. Make Phase Margin close to 48 degrees
4. Use Fastlock or Cycle Slip Reduction

Done

1. Reduce Loop Bandwidth
2. Increase Filter order
3. Increase Filter Attenuation
4. Decrease Phase Margin
More Common Approach

• Often times when presenting loop filter design, it gives an increased appreciation of the various design tools. National Semiconductor has excellent design and simulation tools at www.national.com

• For those seeking more details on the math, consult “PLL Performance, Simulation, and Design”, by Dean Banerjee
Active Filter Example

- Pole After op-amp reduces op-amp noise
- Voltage is centered at half charge pump supply for optimal spurs
LM6211 Op-Amp

- Allows Much Wider Tuning Voltage for VCOs
  - 5 to 24 volt operation
  - Goes to within about 100 mV of rail
- Minimal Added Noise
  - Voltage Noise = 5.5 nV/Sqrt(Hz)
  - Current Noise = 0.01 pA/Sqrt(Hz)
- Requires No Negative Supply
  - Input can go to 0 volts.
- Does not Cause Large Spurs
  - Input Bias Current = 10 nA max
- Small Package
  - SOT23-5
- Low Current
  - 1 mA
## Summary – Rules of Thumb

<table>
<thead>
<tr>
<th>PLL Functional Block</th>
<th>To minimize Noise contribution…</th>
<th>Why?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Detector/Charge Pump</td>
<td>Maximize charge pump gain ((K_\phi)) (up to a certain point)</td>
<td>The phase detector noise contribution is theoretically proportional to (1/(K_\phi)^2)</td>
</tr>
<tr>
<td>R-counter and N-counter divide ratios</td>
<td>Maximize phase detector comparison frequency → this minimizes N</td>
<td>The noise contribution of the R and N dividers is proportional to (N^2).</td>
</tr>
<tr>
<td>Reference oscillator</td>
<td>Use highest frequency practical and use R &gt; 1 if possible. If deciding between maximizing R and minimizing N, minimize N.</td>
<td>The noise contribution from the reference oscillator is proportional to ((N/R)^2)</td>
</tr>
</tbody>
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Real World Resistor

- For high resistance values and high frequencies, resistor might not look like its theoretical value
- $C \approx 0.2 \text{ pF}$
Real World Capacitor (ESR)

- Capacitors have an equivalent series Resistance (ESR)
  - ~ 0.05 ohms for ceramic caps
  - Bigger for larger caps
  - Several ohms for tantalum caps
  - Due to ESR, not always best to choose largest capacitor for power supply
- Self-Resonant Frequency
  - Above this frequency, cap looks like an inductor with a DC block
  - Sometimes good for high frequency input of PLL
- Dielectric Absorption
  - If a voltage is applied across a cap, then a short, a residual voltage can appear
  - Don’t see this effect as much for COG (NP0) and film capacitors
  - Can increase lock times (even up to 5X) if
    - Phase Detector frequency is lower ( < 1 MHz)
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TCXO Input Pin

- Some Parts are sensitive to the slew rate of the signal
  - Better Spurs for faster slew rate
  - Better phase noise for faster slew rate
- Other parts are really no that sensitive
- Often times, this is high impedance at these lower frequencies, so a 51 ohm resistor to ground often does work.
High Frequency Input Pin from VCO

• Input Impedance tends to be capacitive and is not always high impedance, especially at higher frequencies
• Smaller capacitors are good for higher frequencies, but don’t get carried away.
  – Keep the Reactance no more than about 1 ohm
  – Too low value allows harmonics to pass through easier
• Resistive splitter or pad is most reliable
• Sometimes, increasing this attenuation can improve spurs if they are outside the loop bandwidth
  – If you see that spurs get worse with higher charge pump current, even when filter is redesigned for the same loop bandwidth
  – If you see that fractional spurs of the same offset get worse with higher phase detector frequency, even when filter is redesigned for the same loop bandwidth
Power Supply Pins

• Integrated Regulator Output Pins
  – Sometimes sensitive to too low ESR for devices with integrated VCO

• Charge Pump Supplies can be sensitive
VCO Power Supply Noise Impact

- Influenced by Pushing of the VCO

\[ \beta = \frac{\text{Frequency Deviation}}{\text{Modulation Frequency}} = \frac{K_{\text{PUSH}} \cdot V_{\text{IN}}(f)}{f} \]

\[
\text{Sideband}(f) = 20 \cdot \log |J_1(\beta)| = 20 \cdot \log \left( \frac{\beta}{2} - \frac{\beta^3}{2^2 \cdot 4} + \frac{\beta^5}{2^4 \cdot 4^2 \cdot 6} + \ldots \right)
\]

\[ \approx 20 \cdot \log \left( \frac{\beta}{2} \right) \quad \text{for } \beta \ll 1 \]

- Dependent on Frequency
- PSRR is loop filter and frequency dependent
LMX2541 Power Supply Noise Example

Spur for a 25 mV stimulus

Offset (kHz)

Spur Level (dBc)

-80
-70
-60
-50
-40
-30
-20
-10
0
0.1 1 10 100

Theoretical PLL
Theoretical VCO
Actual Measurement
Impact of Resistance on Vreg Pins
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Quick PLL Debugging Tricks

• Step 1: Ensure Proper Communication
  – Typically, PLLs do not have register readack
  – Use the powerdown bit (not pin) and observe current change to ensure part is reading programming correctly

• Step 2: Observe Proper voltages and bias levels
  – VCO input pin typically is 1.6 V powered up, 0 V powered down
  – OSC input pin is typically Vcc/2 powered up, 0 V powered down
  – Internal regulators can also have their bias levels
  – Be aware ESD protection diodes on parts can sort of power up unconnected pins to make the part perform with strange symptoms

• Step 3: Check Loop Filter Issues
  – Flip the phase detector to see the VCO jump to ensure no open/short issues
  – Lower charge pump gain and phase detector frequency to check stability issues

• Step 4: Check the Counters
  – Check the counter outputs at the Ftest/LD pin to ensure they are correct
  – Touching your finger to the part can sometimes help debug impedance matching issues
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