Probing and Porting: Two DSP Activities Yield to New Solutions

Give me the days when men were men, women were women, and PCB-based embedded systems could be probed with ease. Never existed, you say? Could be those halcyon days are artifacts of the mind, false reminiscences that help us get through the daunting challenges of verifying today's SOC-based embedded systems. But back then, at least the processor, bus and peripherals were accessible; now, with almost useless probes in hand, designers face a single block of silicon. For the most part, observability and control have vanished. (As for men and women, let's stick to observability and forget about control; otherwise, I'm not touching that subject with a ten-foot probe.)

Put simply, verifying that an embedded system is market-ready is just plain hard to do. Complex SOCs used in mobile phone handsets and other products have opened a post-silicon verification chasm. First silicon rarely comes up as planned. Assumptions of things that "weren't supposed to happen" turn out to be too optimistic. Teams don't use the same design and verifications languages-or even the same text editor.

Take heart. Today's real men and women-in the form of firmware and middleware and various hardware teams-can join hands and leap the bring-up chasm before committing to silicon. So say the authors of our cover story, from Cadence Design Systems, who offer a solution in the form of an emerging unified verification methodology.

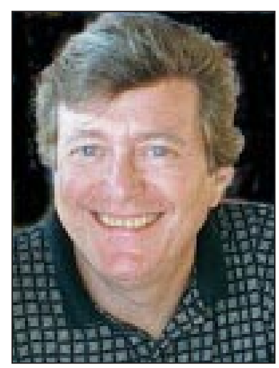
By sharing their collective talents to create three new design elements-an FVP (Functional Virtual Prototype), a transaction testbench, and API assertions-the hardware-dependent teams can shrink the pre-silicon process up to 50 percent. The three elements then become the tools the firmware and middleware teams need to close the chasm and speed products, like mobile phones, to market. Firmware and middleware engineers no longer must deal with unpredictable verification during post-silicon testing.

But while exploring the “good old days,” you may have noticed a bunch of algorithms sitting around that your company developed for PC use. Wouldn't it be nice, you think, if we could run those algorithms on the embedded system we just produced by so heroically leaping across the verification chasm. You can, according to Ketul Patel of eInfochips. Porting is just a question of optimizing the algorithms for faster execution and lower memory consumption.

Noting that the Texas Instruments' TMS320C6205 DSP provides sufficient horsepower to execute--in real-time--most computation intensive image processing algorithms, such as pattern recognition and display processing, eInfochip designers successfully optimized a PC-based algorithm and ported it over. The team there deployed various techniques--converting the code from C++ to C; and optimizing memory, logic and arithmetic calculations. The result is impressive: a 50 times blast in speed over recompiled code. The details are spelled out in our second article.

Before you speed through the details, check out a new feature embedded inside this issue. Noting the exploding demands of wireless applications, the piece, authored by Jean Hummel of Innovative Integration, points to software-defined radios (SDRs) as a key toward providing market-driven solutions.

In an SDR, the entire signal processing chain is digital, built up from reconfigurable firmware and software. A typical SDR will contain an analog interface to the RF stage and antenna, high-speed front-end signal processing, protocol-specific processing and data communications for interfacing with carrier networks and other purposes.



Among other things, Hummel explains why FPGAs are best for the front-end functions, whereas the complex algorithms found in protocol-specific algorithms are more suited to programmable digital signal processors.

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