Embedded Ogg Vorbis Decoder
An efficient implementation on the TMS320C6416 DSP processor
Ogg Vorbis

• Vorbis is an open source lossy audio compression codec.
  – Comparable to other formats used to store and play digital music, such as MP3, VQF, AAC, and other digital audio formats
  – Ogg is the general purpose media container format.
  – Founded by Xiph.org foundation.
Vorbis Source Code

- Xiph.org provides two reference decoder source codes;
  - libvorbis, a floating-point arithmetic decoder implementation
  - Tremor, fix-point arithmetic decoder implementation

- Targeted for embedded implementations of the Vorbis audio compression codec.
Project Outline

• Port Ogg Vorbis *Tremor* reference decoder to TMS320C6416DSK.
• Define the performance critical modules within the design.
• Optimize performance critical modules.
• Examined performance of the optimized Ogg Vorbis decoder.
# Tremor Code Branches

Code branch used for this project.

|                  | Default | Low Mem | No Byte *
|------------------|---------|---------|-----------
| Processor Requirement | Lower   | Higher  | Higher    |
| Memory Requirement   | Higher  | Lower   | Lower     |

* No byte branch is a version of the low-mem branch created for processors whose smallest unit is greater than 8 bits.
Tremor Low-Mem Branch

• Tremor default branch allocates memory dynamically without restriction.

• Tremor low-mem branch improves memory usage with a slight performance penalty although memory is still allocated dynamically without restriction.

• Tremor low-mem branch is better suited for memory restricted embedded environment.
Porting the Source Code

- “Fix” all typedefs for TMS320C6416
- Remove and replace alloca() statements
- Generate front-end C algorithm to interface with Tremor
- Configure DSP/BIOS to handle AIC23 Audio Codec
- Implement algorithm to transfer data between Tremor and AIC23 Audio Codec
Porting Steps

• Create type definitions to match the intended variable bit width with TMS320C6416 variable bit width.
  – typedef long long ogg_int64_t
  –typedef int ogg_int32_t
  – typedef unsigned int ogg_uint32_t
  – typedef short ogg_int16_t
Porting Steps Cont’

• Tremor source code provides a self check for bitwise operations used for decoding.
  – Verify all “assumed” bit width by the source code is consistent with the actual bit width used by TMS320C6416
Porting Steps Cont’

• Fix the known issues with the *Tremor* source code.
  – Add `free()` statement to appropriate locations to remove memory leaks.
  – Fix all compiler warnings.

• Replace `alloca()` statement with `malloc()` and `free()` statements.
Porting Steps Cont’

• Create a generic file system to store a Vorbis audio file.
  – Read a Vorbis audio file into on-board SDRAM in Main() during DSP/BIOS initialization.
  – Add file system functions to the Tremor low-mem source code to access and read Vorbis the audio file.

• Implement the setup and tear down steps required for Tremor source code.
Porting Steps Cont’

• Implement ping pong buffers to store decoded samples.

• Configure DSP/BIOS to output the decode samples using AIC23 audio codec interrupt (HW_INT11) while performing decoding in the background.
Design Block Diagram

- SDRAM
- void decode ()
- Vorbis Decoder
- Task
- Ping Pong Buffer
- void pcm_out ()
- Output PCM to AIC23
- ISR
- McBSPXINT HWI_SINT11
PIP Objects

- PIP Module (Pipe Manager) manages block I/O used for streams of program input and output.
- Data notification functions are used to synchronize data transfers.
PIP vs Ping Pong Buffer

• Ping Pong requires more user coding
  – Higher chances of mistake
  – May not be optimized

• PIP easier to implement and low overhead
  – PIP module management functions are available. Only requires few function calls to manage buffer.
  – Optimized for DSP/BIOS

PIP Module simplifies input and output data stream implementation.
Design Block Diagram with PIP

- SDRAM
- void decode ()
- Vorbis Decoder
- SWI_ISR
- PIP Module
- McBSPXINT
- HWI_SINT11
- IOM Driver
- Output PCM to AIC23
- HWI_ISR
Performance Results

### Ping Pong Buffer Implementation

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<th>Cycles</th>
<th>Percentage</th>
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<tr>
<td>IMDCT</td>
<td>75823572</td>
<td>44.40%</td>
</tr>
<tr>
<td>Residue Upack</td>
<td>51500363</td>
<td>30.00%</td>
</tr>
<tr>
<td>AIC23 Codec + Buffer Overhead</td>
<td>738718</td>
<td>0.40%</td>
</tr>
<tr>
<td>Other</td>
<td>42687551</td>
<td>25.20%</td>
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</tbody>
</table>

### PIP Module Implementation

<table>
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<tr>
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<th>Cycles</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
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<td>44.00%</td>
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<tr>
<td>Residue Upack</td>
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<td>30.00%</td>
</tr>
<tr>
<td>AIC23 Codec + PIP Overhead</td>
<td>695231</td>
<td>0.40%</td>
</tr>
<tr>
<td>Other</td>
<td>43564251</td>
<td>25.60%</td>
</tr>
</tbody>
</table>

Profiled by decoding ~5 second 128kps 44.1Hz stereo clip
Profiling the Results

- IMDCT and residue unpacking takes up the majority of the available clock cycles.
  - A better IMDCT algorithm can provide speed improvement without writing assembly.
- The difference between ping pong buffer and PIO module is minimal compared to the number of cycles taken by the Vorbis decoder.
DCT and DFT

- MDCT can be rewritten as an odd-time odd-frequency discrete Fourier transform. MDCT-IV is defined as shown below,

\[
DCT_{[K]}^{IV} : \quad C_k^{IV} = \sum_{r=0}^{K-1} x_r \cos \left( \frac{\pi}{4K} (2k + 1)(2r + 1) \right)
\]

and K-th coefficient number of odd time odd frequency DFT of length N is defined as shown below,

\[
O^2DFT_{[N]} \{u\} = U_k = \sum_{r=0}^{N-1} u_r e^{-j \frac{\pi}{N} (2k+1)(2r+1)}.
\]

Using zero padding,

\[
x'_r = \begin{cases} 
  x_r & \text{for } 0 \leq r \leq K - 1 \\
  0 & \text{for } K \leq r \leq 2K - 1 
\end{cases}
\]

The relationship between MDCT-IV and DFT is defined as the following,

\[
C_k^{IV} = \Re \{ O^2DFT_{(2K)} \{x'\} \}, \quad k \in \{0, \ldots, K - 1\}.
\]
New $O^2$ DFT Algorithm

- $O^2$ DFT can be calculated using one $n/4$ point FFT with pre-rotation and post-rotation.

   Taking advantage of built-in symmetry,

\[
\mathcal{P}_k = u_{2k} + j u_{N/2+2k} = 2 \sum_{r=0}^{N/4-1} \left( u_{2r} - j u_{N/2+2r} \right) e^{-j \frac{2\pi}{N} \left(2k + \frac{1}{2} \right) \left(2r + \frac{1}{2} \right)}
\]

\[
= 2 e^{-j \frac{2\pi}{N} \left( k + \frac{1}{2} \right)} \sum_{r=0}^{N/4-1} \left\{ \left( u'_r e^{-j \frac{2\pi}{N} \left(r + \frac{1}{2} \right)} \right) e^{-j \frac{2\pi}{N} r k} \right\},
\]

\[
\text{N/4 point FFT}
\]

\[
u'_r = \left( u_{2r} - j u_{N/2+2r} \right),
\]

\[
N = 4i; \ i \text{ integer}; \ r, k = 0, 1, \ldots, \frac{N}{4} - 1.
\]
New MDCT Algorithm

- MDCT is a special case of the new $O^2$ DFT algorithm.

$$u'_r = (x_{2r} + jx_{K-1-2r})$$

$$C_{2k}^{IV} = \frac{1}{2} \Re \{ P_k \}$$

- IMDCT is basically a scaled version of MDCT.
Performance Optimization

• New IMDCT implementation
  – The optimized IMDCT algorithm is performed as follows:
    1. Pre-processing
    2. N/4-point complex FFT
    3. Post-processing
  – Uses optimized DSP_fft32x32 function from with built-in bit reversal from C64X TI DSPLIB
Optimization Block Diagram

Pre-Processing

Pre-Arrange → Pre-Rotation

Post-Processing

Post-Arrange ← Post-Rotation

Complex FFT N/4
Pre-Processing

• Pre-Arrange and Pre-Rotation

```plaintext
for (i = 0; i < n/4; i++)
    X'[i] = X[2*i] * rotation factor[i]
    X'[i+1] = X[(n/2-1)-2*i] * rotation factor[i+1]
```
Complex FFT N/4

- Utilize the DSP_fft32x32 from the TI DSPLIB
  - Generate twiddle factor with “tw_fft32x32.exe” from DSPLIB
  - Include “dsp_fft32x32.h” header file
  - Call DSP_fft32x32 to perform FFT
Post-Processing

• Post-Arrange and Post-Rotation

for (i = 0; i < n/4; i++)
    x[i] = x'[i] * rotation factor[i]
## Performance Result after Optimization

<table>
<thead>
<tr>
<th></th>
<th>MIPS</th>
<th>Percent Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before IMDCT Optimization</td>
<td>~124</td>
<td>N/A</td>
</tr>
<tr>
<td>After IMDCT Optimization</td>
<td>~82</td>
<td>35.00%</td>
</tr>
</tbody>
</table>

Profiled by decoding ~75 second 128kps 44.1Hz stereo clip
Future Improvements

• Remove dynamic memory allocation from the Vorbis Decoder.
• Write pre- and post- processing section from the new IMDCT algorithm in assembly.
• Write the residue decoding portion in assembly.
• Make the code 100% RF3 compliant.
References


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An efficient implementation on the TMS320C6416 DSP Processor
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