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Minds in Motion

Tools For Debugging JTAG and Power Issues on DaVinci and OMAP devices

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Agenda

- JTAG Challenges for Multi-core Devices
- ICEPick Overview
- ICEPick CCS Support
- DBGJTAG Utility
- Demo
- Q&A

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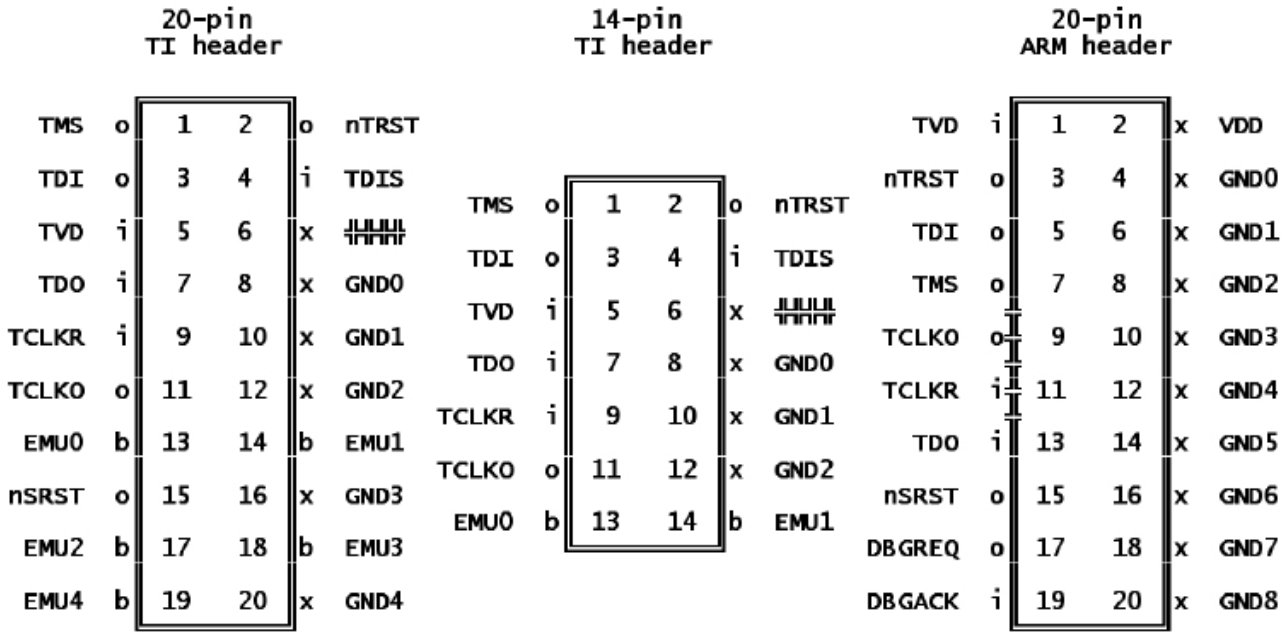
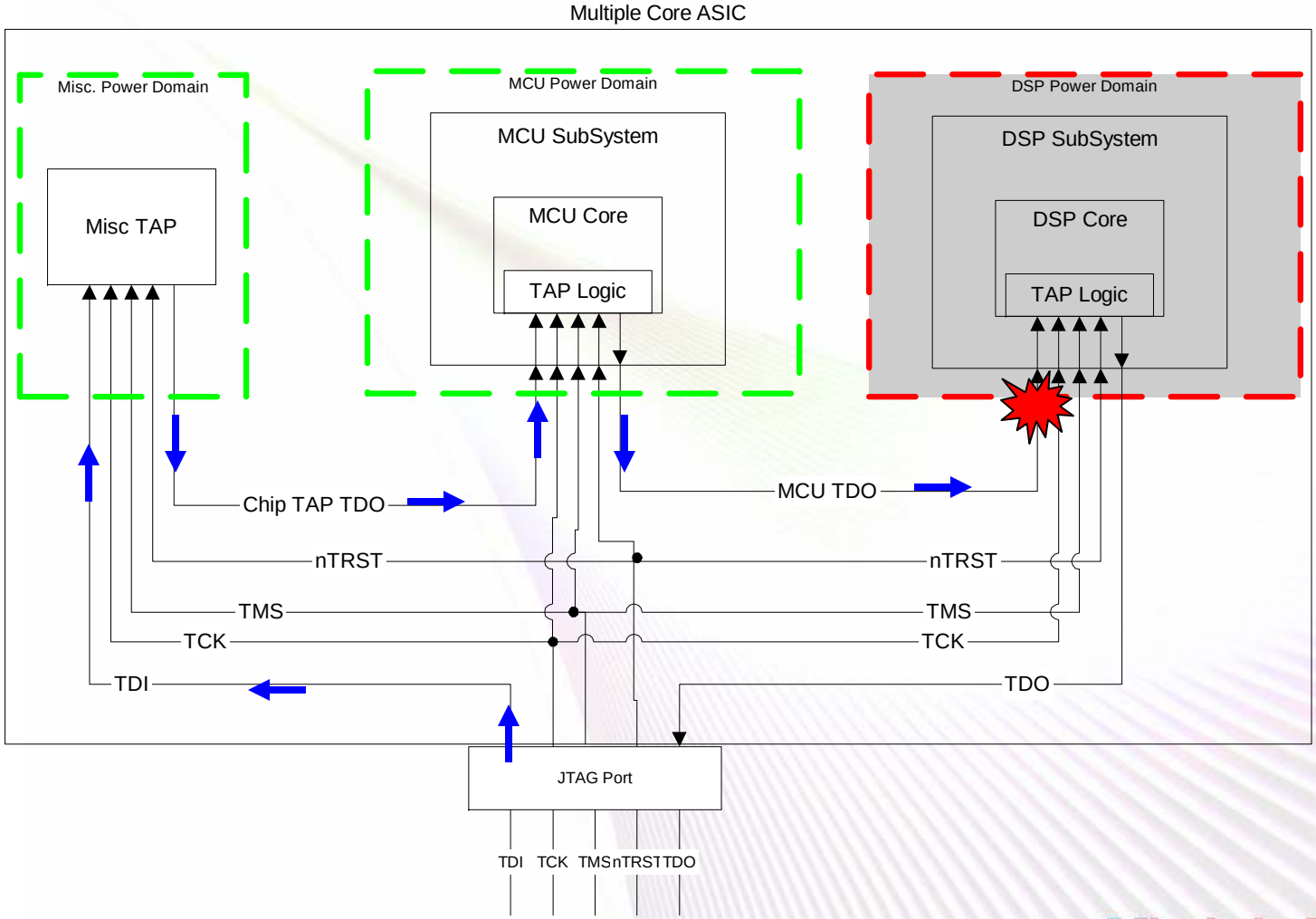
JTAG Overview



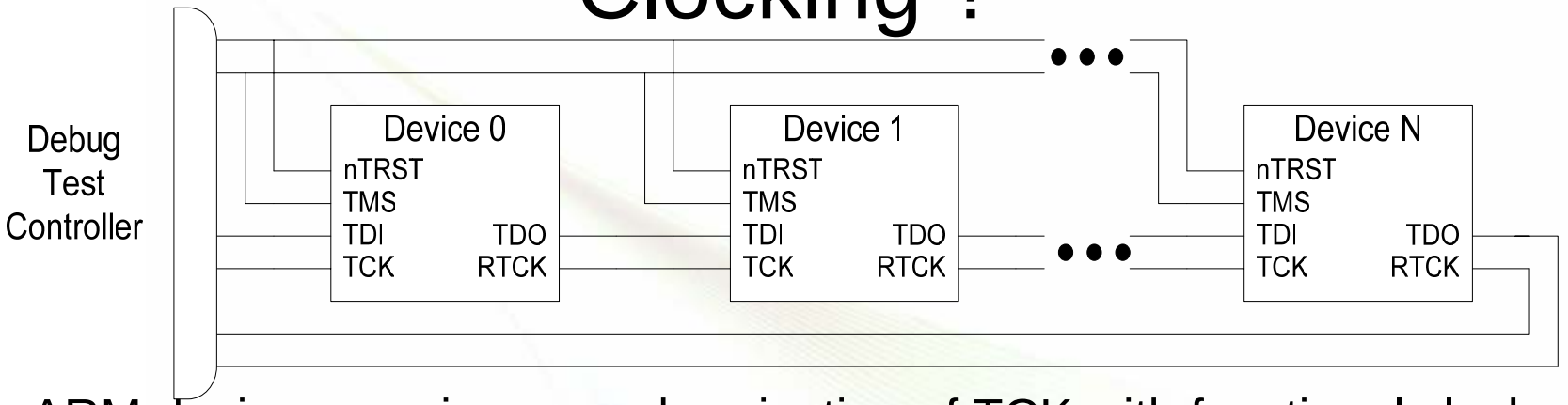
What is the Challenge – Power ?

- Power isolation
  - Portions of the chip are “powered down” when they are not being used
- Power isolation has serious impact on emulation
  - JTAG TAP logic is likely to be embedded inside an isolated domain
  - Current JTAG daisy chain topology is compromised when these discrete domains are powered down or sent to retention mode.

Domain Power Down Breaks JTAG Scan



What is the Challenge – Adaptive Clocking ?



- ARM devices require resynchronization of TCK with functional clock.
- This resynchronization creates an RTCK clock.
- The serialized daisy chaining of such devices imposes severe restrictions:
  - Does not work with a Rev.B xds560 pod or xds510 emulator unless the selected maximum TCK frequency is reduced to take account of both the slowest ARM clock in any device and the number of devices in the daisy chain.
  - Can only be used with an adaptive clocking emulator (e.g. TI Rev.D xds560 pod) with *severe* performance constraints.

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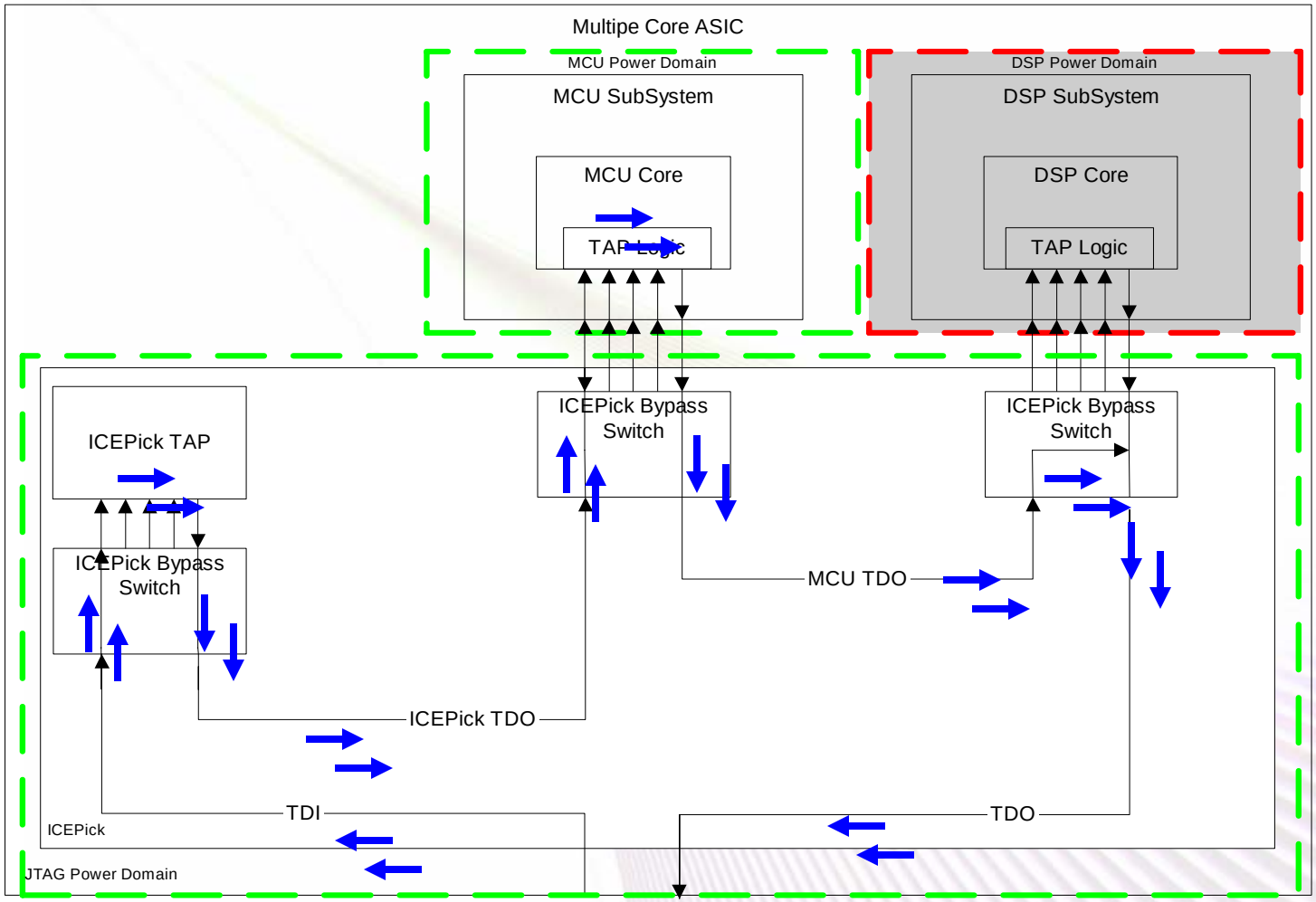
Introduction to ICEPick-C

- Dynamic scan chain management within the device
- Ability to interface multiple ARM cores with different RTCK frequencies
- Requires debugger support of dynamic scan chain management.

Power Domains With ICEPick



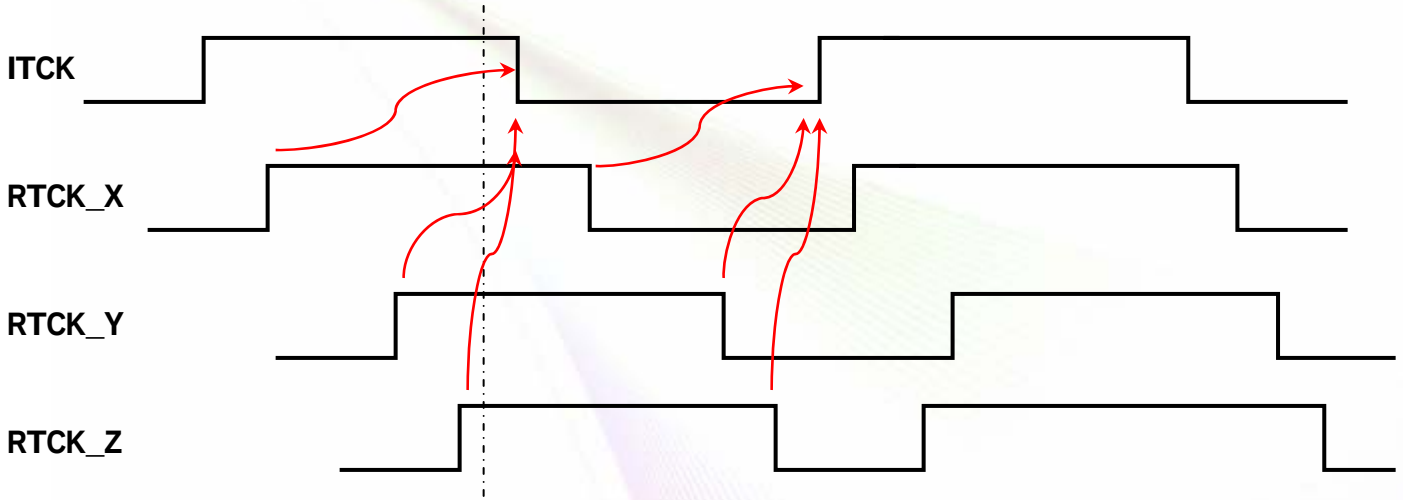
How does ICEPick solve the power problems?

- The primary JTAG interface is connected to ICEPick which is a chip level tap controller.
- ICEPick supports dynamic insertion and removal from the scan path of debug JTAG taps which are part of MCU or DSP cores
- Cores which are powered down do not affect the emulator JTAG connection because their taps are not in the scan chain.

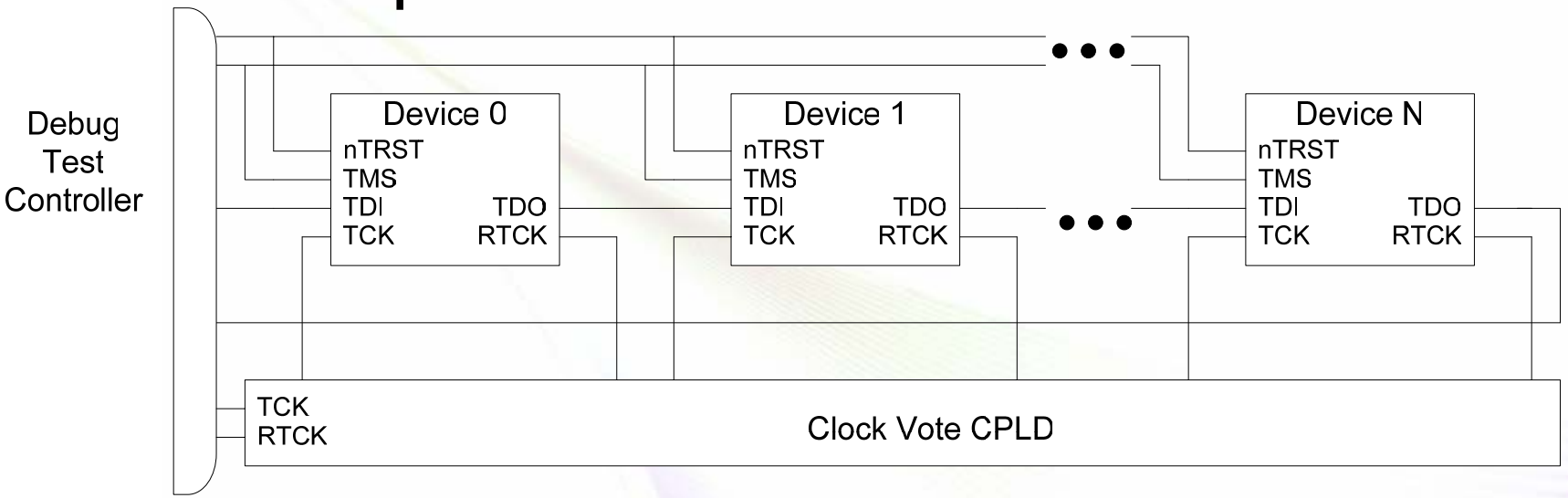
How to interface multiple ARM cores with ICEPick?

- Clock voting logic in ICEPick allows interfacing taps with multiple RTCK synchronisers.
- The TCK presented to each selected JTAG tap is based upon a consolidation of the RTCK from each selected tap.

Clock Voting (ICEPick-c)



How to use a single JTAG connection to multiple devices at board level?



- The suggested method involves using ICEPick-c clock voting logic in a CPLD.
- This method works provided that *all* devices are booted at the time debug is started.
- This method provides:-
  - Backward compatibility with Rev B xds560 and xds510 based pods
  - Allows for significantly better performance than daisy chaining the clocks using an adaptive clocking emulator (Rev D xds560 pod).
- Clock voting VHDL is available via softwaresupport@ti.com

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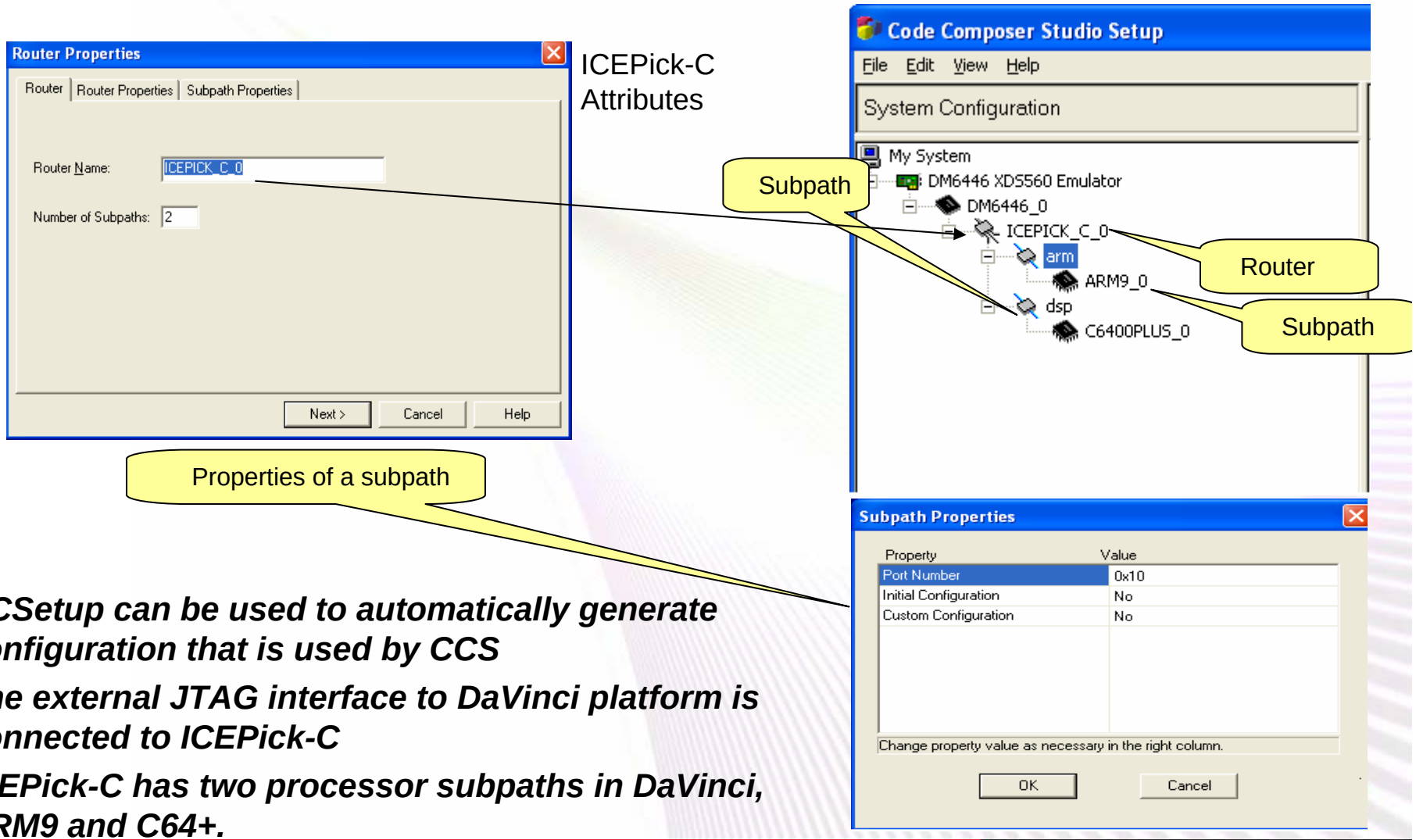
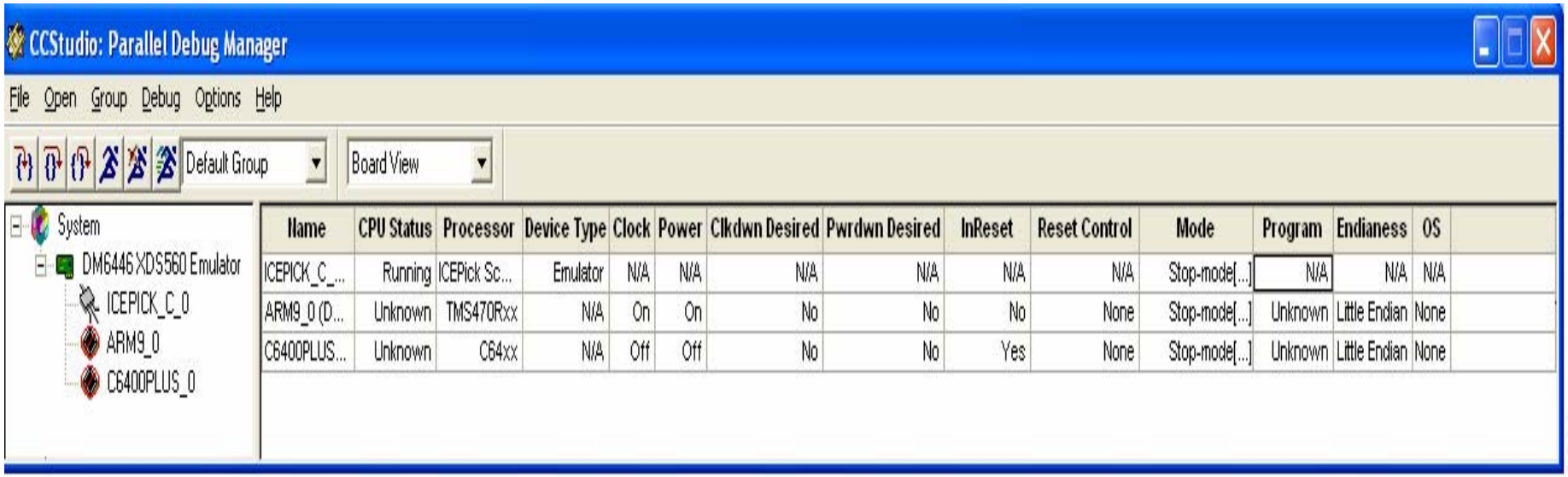
CCSetup - ICEPick Based Configurations



- ***CCSetup can be used to automatically generate configuration that is used by CCS***
- ***The external JTAG interface to DaVinci platform is connected to ICEPick-C***
- ***ICEPick-C has two processor subpaths in DaVinci, ARM9 and C64+.***

ICEPick Visualization - DaVinci



- ***Clock Status***
- ***Power Status (Domain Active/Inactive or Ret/Off)***
- ***ClockDownDesired Status (clock gating transition being inhibited or not)***
- ***Powerdowndesired status (power transition being inhibited or not)***
- ***InReset status (processor in warm reset or not)***
- ***Reset configuration (Wait-In-Reset mode active or not)***

Low Power Mode Tools Support for ICEPick

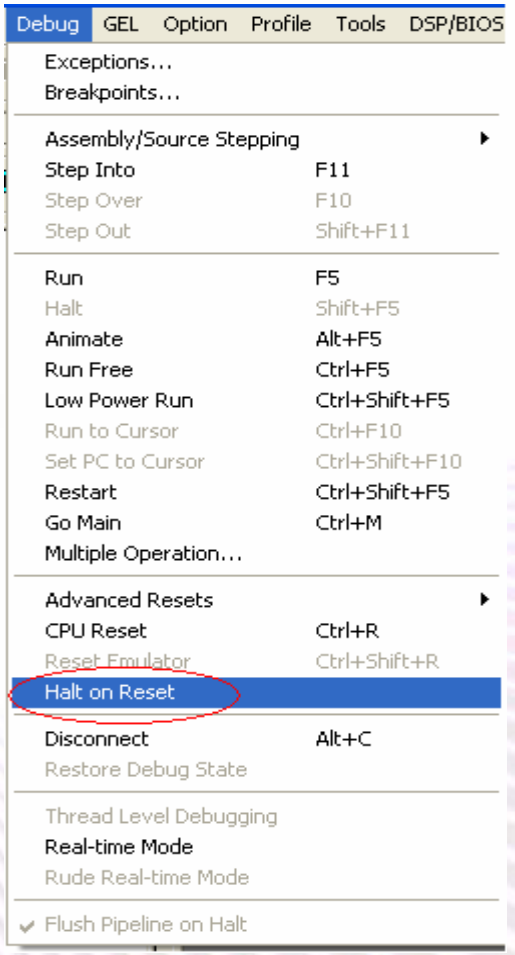
- New “Low Power Run” Feature introduced
  - Maintain debug connection on any CPU through low power states.
  - Allow HWBP and/or SWBP to survive between power sessions

Examples of Low Power Mode Usages

- OMAP3430
  - Cortex-a8
    - When using breakpoints (HWBP or SWBP) in conjunction with the MPU domain reaching OFF state then application must use debug context/save restore mechanisms.
  - C64+ (Mid-GEM 2.0)
    - Supports usage of SWBP across IVA OFF state.
    - Allows debug of DSP ISR servicing interrupt waking up the domain from a low power state.
    - If the same DSP ISR is being used for servicing a sleep request as well as a wakeup request then can set a HWBP qualified by a hardware implemented skip count feature to only halt the CPU after the skip count is reached. This works as long as the domain only reaches RETENTION mode.

Debug Code from Power Up

- Enable debug from device power up.
  - This is enabled using a particular hardware configuration of the EMU0 and EMU1 JTAG header pins.
  - This setup is supported when using the REV.D XDS560 pod.
- Enable debug from domain power up or boot of slave processor
  - Possible to debug boot code of slave device.
  - Possible to debug context restore code of CPU from reset vector when it comes out of logic OFF state.



Examples of Halt On Reset Usages

- DaVinci™/OMAP3430
  - C64+
    - Allow debug of DSP ROM code from reset vector after C64+ is first booted in ROM boot mode.
  - ARM9/Cortex-A8
    - Allow debug of ROM code from device boot.
    - Allow debug of customer Flash code from device boot.
- OMAP3430/C64+
    - Allow debug of DSP/BIOS code from reset vector after IVA domain wakes from OFF state.

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DBGJTAG Utility

- A diagnostic utility for TI and 3rd-party JTAG hardware
- Replaces the old XDSPROBE utility
- Hardware tests on emulators, cables and boards
- Scan and frequency tests on routers and devices

DBGJTAG Utility - basics

- Selecting emulators (-d)
- Resetting emulators (-r)
- Selecting board config' files (-f)

```
dbgjtag.exe -d xds560 -p0 –rv -f brddat\ccBrd0.dat
```

- Retrieving build-in help (-h)

```
dbgjtag.exe -h
```

```
dbgjtag.exe –S help
```

DBGJTAG Utility - scan

- Measuring IR/DR path-lengths (-S)

```
dbgjtag.exe -d xds560 -p0 –S pathlength
```

- JTAG test-patterns (-S)

```
dbgjtag.exe -d xds560 -p0 –S integrity
```

```
dbgjtag.exe -d xds560 -p0 –S givendata, literal=0x5533, repeat=200
```

- JTAG route operations (-R)

```
dbgjtag.exe -d xds560 -p0 -S pathlength -f brddat\ccBrd0.dat
-R routelist, subpaths=arm+dsp
```

DBGJTAG Utility - frequency

- Selecting a TCLK frequency(-F clock)

```
dbgjtag.exe -d xds560 -p0 –F clock, program=specific, frequency=10
```

- Measuring a JTAG frequency(-F inform)

```
dbgjtag.exe -d xds560 -p0 –F inform, logfile=yes
```

- Evaluating signal quality (-G range)

```
dbgjtag.exe -d xds560 -p0 –G range, lowest=2.5, highest=35
```

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Demo

- DBGJTAG on DaVinci™ platforms
- ICEPick demo on OMAP™ device

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Backup Slides

IR/DR Length Table

Device	IR	DR
ICEPick	6	1
ARM11	5	1
ARM9	4	1
ARM7	4	1
C64x+	38	1
C55x	38	1
ETB	4	1
DAP	4	1

DBGJTAG Utility - advanced

- Configuring cables (-Y emupins)

```
dbgjtag.exe -d xds560 -p0 –Y emupins, jtagboot=01, powerboot=10
```

```
dbgjtag.exe -d xds560 -p0 –Y jtagpins, jtagboot=01, powerboot=10
```

- Controlling System Reset (-Y reset)

```
dbgjtag.exe -d xds560 -p0 –Y system, signal=pulse
```

- Controlling JTAG state (-M jtag)

```
dbgjtag.exe -d xds560 -p0 –M jtag, goto=idle
```

Board Configuration File - Overview

- Configuration files used by JTAG scan controller software
- Contains both device and variable records
- Describes JTAG scan paths
- Generated by CCS_Setup and then used by CCS and DBGJTAG utility (ccBrd0.dat)
- Can be hand edited independently of CCS

Board Configure File - example

```
# config version=3.5
$ uscif
  # Select a TI PCI-bus XDS560 emulator
  ecom_drvr=xds560.out
  ecom_port=0x0
  # TCLK Setup to use 2 MHz
  tclk_program=SPECIFIC
  tclk_frequency=2
  tdoedge=RISE
$ /
@ icepick_c_0 family=icepick_c subpaths=2
  & dsp address=18 default=no custom=no
    @ c6400plus_0 family=tms320c64plus
  & arm address=16 default=no custom=no
    @ arm9_0 family=arm9xx
  & /
# /
```

- Label
- Comment
- Variable
- Device
- Family
- Sub-path