Data Converter Basics
How to Use and Test Data-Acquisition Products

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Workshop Agenda

• Data Converter Fundamentals
  – Key concerns when choosing a data converter
  – Data converter and analog design tools

• Design Considerations
  – Input drive considerations
  – Cost and performance tradeoffs
  – PCB layout

• Putting the Pieces Together…
  – Software tool demos
  – Hardware tool demos
Data Acquisition Components
Types of Input Signals

+5V

5kΩ

-5V

5kΩ

DAQ System

Minds in Motion

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Simultaneous Sampling

• Why do simultaneous sampling?
• Applications for simultaneous sampling converters
Why Sample Simultaneously?

• Preservation of Phase Relationship
  – Speed/position sensors
  – Vibration analysis

• Relative Signals for Various Equations
  – Power
  – Torque, etc.
Simultaneous Sampling Applications

- ADC
- OPA350
- TLV3501
- OC
- F28xx
- REF32xx
- TMP122
- AC/DC Inverter

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Simultaneous Sampling ADCs

• 2x2 SAR: 2 ADCs with 2 S/H
  – ADS7861, ADS8361
  – ADS7862
• 3x2 SAR: 2 ADCs with 3 S/H
  – ADS7864
• 1x6 SAR: 6 ADCs with 1 S/H
  – ADS8364, ADS8365
• Pipeline
  – THS12xx
2x2 SAR

Serial Interface

SAR

COMP

CDAC

SHA

CONVST

RD

BUSY

CS

CLOCK

A0

M1

M0

SERIAL DATA B

SERIAL DATA A

REFOUT

REFIN

CH A0+ CH A0D

CH A1+ CH A1D

CH B0+ CH B0D

CH B1+ CH B1D

Internal 2.5V Reference

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1x6 SAR
4X1 Pipeline

- **Logic and Control**
- **12 Bit Pipeline ADC**
- **FIFO 16:12**
- **Buffers**

**Power Supplies:**
- AVDD
- DVDD
- 3.5 V
- 1.5 V
- 1.225 V

**Grounds:**
- AGND
- DGND

**Analog Inputs:**
- REFP
- REFM
- AINP
- AINM
- BINP
- BINM

**Digital Inputs:**
- CONV_CLK (CONVST)
- CS0
- CS1
- RD
- WR (R/W)

**Digital Outputs:**
- D0 - D11/RA1
- D10/RA0
- BVDD

**RefERENCE:**
- VREFP
- VREFM

**Reference Inputs:**
- REFOUT

**Control Register**

**Note:** This diagram illustrates the connections and components of a 4X1 pipeline ADC. Please refer to the manufacturer's datasheet for detailed specifications and usage instructions.
Multiplexed Sampling

- Are there advantages?
- What about using multiple ADCs?
- Applications for multiplexed inputs
Multiplexed Advantages

- Fewer converters needed per channel – often only one needed.
- Often lower power
- Often lower cost
Multiplexed vs. Multi-Chip

- Reference distribution issues
- Input signal issues: One channel has very different input needs from others.
  - Use a single channel device, MUX the others.
- Multiplexing implies time delays between channels – system issues? Simultaneous sampling better?
- Can the processor easily support multiple ADCs?
Reference Distribution

- REF
- Buffer/Filter
- Buffer/Filter
- Buffer/Filter
- ADC
- ADC
- ADC
Multiplexing Basics
Multiplexed Applications

- Temperature monitoring
- Multi-point weigh scales
- Pressure monitoring
- Control surface transducer readings (e.g., audio mixer control surface)
- General purpose low-speed sensor data acquisition
Multiplexing Application Tips

• If converter is available with internal MUX, use it!
  – Available on both SAR and delta-sigma.
• Internal MUXes are tailored to match the ADC performance.
• Don't have to guess about switching and settling time.
Multiplexing SARs vs. $\Delta\Sigma$s

- SAR-based systems often require low-pass filters on each channel, increasing power and cost.
- $\Delta\Sigma$ systems generally offer greater accuracy and lower noise floor.
- SAR designs with a post-multiplexer filter result in a system with settling-time issues almost identical to the $\Delta\Sigma$ design, but with higher noise.
Multiplexing with SARs
Multiplexing with Delta-Sigmas
The Delta-Sigma Architecture

Analog Input \xrightarrow{\sim} \text{Delta-Sigma Modulator} \rightarrow \text{Decimator} \rightarrow \text{Digital Decimating Filter} (usually implemented as a single unit) \rightarrow \text{Digital Output}
SAR vs. Delta-Sigma Conversions

- SAR conversions have Start Conversion Signal.
- Delta-Sigma is always sampling/converting.
Settling Time

For a delta-sigma, these are normally combined.
Settling Time: SAR vs. ΔΣ

SARs can convert any time, so can be made to resume conversion at just the right moment.

Delta-sigma with 2-cycle settling time.
Effects of Settling Time

MULTIPLEXING

LOW-PASS FILTERING

FILTER SETTLING – MEASUREMENT INVALID
Aliasing will occur at these frequencies.

50-dB, alias-free range is insufficient for 16 bits.
Improved Anti-Aliasing Filter

An 8-pole filter increases dynamic range to 98 dB!
8th Order Filter Example

\[ V_{\text{AIN}} \]

\[ \text{OPA4227UA} \]

\[ \text{U1A} \]

\[ \text{U1B} \]

\[ \text{U1C} \]

\[ \text{U1D} \]

\[ \text{MUX IN} \]
Filter Pro™

- A filter synthesis tool for designing multi-section, low-pass and high-pass active filters.
- Supports 2\textsuperscript{nd} to 10\textsuperscript{th} order, multiple-feedback (MFB) and Sallen-Key filter topologies.
The Filter Pro Worksheet

Filter topology
Pass band
No. of poles
Ripple (Chebychev)
Cutoff freq.
Response freq.
Gain

Topology info
Response plot
Filter schematic with component values
Section Info: G, f_n, “Q”

The Multiple Feedback (MFB) or Infinite Gain topology places two feedback paths around an op amp. This filter type is less sensitive to component values than the Sallen-Key topology.
Filter Pro Topologies

Multiple Feedback (MFB)
- Inverted stage
- No common-mode error
- Low component sensitivity

Sallen-Key
- Non-inverting stage
- Common-mode input C adds to C3
- G = +1V/V, reduces to follower
- High “Q” sensitivity
Response Characteristics

Frequency Response

Time Domain

T100uS impulse
Bessel
Butterworth
Chebychev

12dB Gaussian

1kHz, 4-pole Low-pass Filters
Impulse response

Gain (dB)

Frequency (Hz)

Voltage (V)

Time (s)

1kHz, 4-pole Low-pass Filters
Amplitude response

Technology for Innovators™
TINA-TI™ is an easy-to-use, but powerful, circuit simulation program based on a SPICE engine. TINA-TI™ is a fully functional version of TINA, loaded with a library of TI macromodels plus passive and active models. TINA-TI is limited to circuits with two ICs and up to 20 additional nodes.
Test and Measurement
OPA355 single-supply video amplifier, $G = 4V/V$

Virtual Instruments

Virtual Instruments
For More on TINA-TI

Where to get TINA-TI:
http://focus.ti.com/docs/toolsw/folders/print/tina-ti.html

Or simply go to www.ti.com and enter TINA-TI in the keyword search box.
In Summary

• Know Your Input Signals
  – Speed, bandwidth
  – Time relationships to each other

• Choose the Right Scheme
  – Multiplexing
  – Simultaneous sampling
  – Multiple ADCs

• Choose the Right Converter Architecture
  – SAR
    • Input buffering and drive requirements
  – Delta Sigma
    • Settling time of filters
Design Considerations

• ADC Input Drive
• Cost and Performance Tradeoffs
  – Improving embedded ADC performance.
• PCB Layout Considerations
  – Analog and auto routers don’t mix.
Input Drive Circuitry

• Input Types
  – Single ended
  – Pseudo-differential
  – Differential

• Buffer Op Amp
  – Rail-to-rail considerations

• RC Circuit
  – Establishing starting criteria

• Modeling the ADC Input Interface
Single-Ended Inputs

ADC

+V

-V (optional)
Single-Ended Inputs

- A single input pin for a particular channel.
- Input signals are referred to ground.

Note: input is referred to GROUND!
True Bipolar Inputs

Devices with up to +/-10VDC inputs

• ADS78xx and ADS85xx Series
• TLC257x and TLC357x Series
Pseudo Differential Inputs

- More like a single-ended input than differential, but with some advantages.
- IN- pin can move, but in a limited range.
- Good for removing common-mode voltages, offsets, etc.
- Provides a “clean” signal reference point.
Pseudo Differential Example

- Example: 0V to 2V sine wave; 1V common mode voltage.
- ADC sees the difference between the two inputs ("differential").
- Output code may be unipolar or bipolar (bipolar shown here).
Differential Inputs

- Sometimes called “fully differential.”
- ADC sees AINP-AINN as input.
- Both inputs can swing from 0V to the full scale – but NOT below ground (in most cases).
- Typically move in a “balanced” fashion.

Example: ADS1271
Differential Input Example

Common Mode Voltage (CMV)

\[(\text{VIN}+) - (\text{VIN}-) = +\text{VREF}\]

\[(\text{VIN}+) - (\text{VIN}-) = -\text{VREF}\]

\[|\text{VREF}|\]
Driving SAR Inputs

\[ V_{IN} \]

\[ S \]

\[ C \]

Data Output Register

SAR

N-bit Search DAC
**Op Amp**
CMV range, $V_{OS}$ vs CMV
RR out-swing to the rail
Slew rate, Signal BW,
Load transient, Settling time,
Output impedance

**Filter**
Charge bucket
Filtering,
$C_{load}$ isolation,

**A/D**
Acquisition time
Input circuit parameters
Initial voltage on $C_{SH}$

---

**Interface Circuit**

- **Operational Amplifier (Op Amp)**
- **Filter**
- **A/D Converter**

**Component Values**
- $R_{flt}$
- $R_{sw}$
- $C_{SH}$ (20pF to 50pF)
- $V_{int}$ ($V_{CC}$, 0.5$V_{CC}$, or GND)

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Design Checklist Items

- Op Amp Common Mode Voltage
- Op Amp Output Swing to Rail
- Op Amp Settling Time
- Filter Capacitor Type
- Filter Component Values
- Op Amp Specifications
Amplifier Input Concerns

Rail-to-Rail Input
Drive Stage Concerns

Rail-to-Rail Output
Rail-to-Rail Limitations

Example: OPA350
• Since op amp can only swing 4.8Vp-p.
• Set ADS FSR to 4.8V by reducing Refin to 2.4V.
Why the R/C Filter?

![Diagram of R/C filter circuit]

- \( R_{\text{flt}} \)
- \( C_{\text{flt}} \)
- \( R_{\text{sw}} \)
- \( C_{\text{SH}} \) (20pF to 50pF)
- \( V_{\text{int}} \) (\( V_{\text{cc}} \), 0.5\( V_{\text{cc}} \), or GND)
- \( \text{SW}_{\text{samp}} \)
- \( \text{SW}_{\text{conv}} \)
Charge Transients

Tek stop 10.0MS/s  8 Acqs

△: 20.0 V
@: -3.4 V

2 Sep 2003 16:17:52
R/C Component Selection

• Pick $C_{flt} = 20 \times C_{SH}$
• $R_{flt}$ Calculation
  $t_{flt\_settle} = t_{ACQ} = 12 \tau_{FLT}$
  Theoretical Minimum

Practical Results:

– Use $t = 18 \tau_{FLT}$ margin for:
  • Op amp output load transient
  • Op amp output small signal settling time
– $R_{flt} = t_{ACQ}/18 \times C_{flt}$
## Settling Time vs. Resolution

<table>
<thead>
<tr>
<th>Number of bits</th>
<th>0.5LSB</th>
<th>Time Constants</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>0.0488281%</td>
<td>8</td>
</tr>
<tr>
<td>12</td>
<td>0.0122070%</td>
<td>9</td>
</tr>
<tr>
<td>14</td>
<td>0.0030518%</td>
<td>11</td>
</tr>
<tr>
<td>16</td>
<td>0.0007629%</td>
<td>12</td>
</tr>
<tr>
<td>18</td>
<td>0.0001907%</td>
<td>13</td>
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<tr>
<td>20</td>
<td>0.0000477%</td>
<td>15</td>
</tr>
<tr>
<td>22</td>
<td>0.0000119%</td>
<td>17</td>
</tr>
<tr>
<td>24</td>
<td>0.0000030%</td>
<td>18</td>
</tr>
</tbody>
</table>
In Summary

• Choose the right ADC for your system input requirements
  – Single-ended
  – Pseudo-differential
  – Differential

• Buffer op amp
  – Rail-to-Rail considerations
  – Settling times and drive capability

• RC circuit
  – Use the starting criteria established here.
  – Experiment to optimize.
Balancing Cost and Performance

• What does the system really need?
• But I already have an on-board ADC…
• How to improve performance of an embedded converter.
System Input Requirements

- Component selection: choice does matter!
- What performance level are you looking for?
- Does the embedded ADC give the required accuracy?
- Does the on-board reference support the required accuracy?
Capacitor Choice Is Important!

\[ R_{\text{fit}} \quad C_{\text{fit}} \quad R_{\text{sw}} \quad C_{\text{SH}}(20\text{pF to } 50\text{pF}) \quad \text{SW}_{\text{samp}} \quad V_{\text{int}}(V_{\text{cc}}, 0.5V_{\text{cc}}, \text{or GND}) \]

\[ \text{SW}_{\text{conv}} \]
THD+N vs. Frequency

- Sweep | Trace | Color | Line Style | Thick | Data                     | Axis | Comment
- 1     | 1     | Yellow | Solid     | 1     | Anlr.THDC+N Ratio        | Left | C = 0
- 2     | 1     | Red    | Solid     | 1     | Anlr.THDC+N Ratio        | Left | C1
- 3     | 1     | Blue   | Solid     | 1     | Anlr.THDC+N Ratio        | Left | C2
- 4     | 1     | Cyan   | Solid     | 1     | Anlr.THDC+N Ratio        | Left | C3
- 5     | 1     | Green  | Solid     | 1     | Anlr.THDC+N Ratio        | Left | C4

R = 100 ohm, C = 3.3 nF, Vp-p = 5V f(-3dB) = 482 kHz
THD+N vs. Voltage

<table>
<thead>
<tr>
<th>Sweep</th>
<th>Trace</th>
<th>Color</th>
<th>Line Style</th>
<th>Thick</th>
<th>Data</th>
<th>Axis</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>Yellow</td>
<td>Solid</td>
<td>1</td>
<td>Anlr.THD+N Ratio</td>
<td>Left</td>
<td>C = 0</td>
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<tr>
<td>2</td>
<td>1</td>
<td>Red</td>
<td>Solid</td>
<td>1</td>
<td>Anlr.THD+N Ratio</td>
<td>Left</td>
<td>C1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>Blue</td>
<td>Solid</td>
<td>1</td>
<td>Anlr.THD+N Ratio</td>
<td>Left</td>
<td>C2</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>Cyan</td>
<td>Solid</td>
<td>1</td>
<td>Anlr.THD+N Ratio</td>
<td>Left</td>
<td>C3</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>Green</td>
<td>Solid</td>
<td>1</td>
<td>Anlr.THD+N Ratio</td>
<td>Left</td>
<td>C4</td>
</tr>
</tbody>
</table>

R = 100 ohm, C = 3.3 nF, f = 10 kHz, f(-3dB) = 482 kHz
What ‘C’ Type Should I Use?

• Best performance:
  – Silver Mica or C0G(NPO)

• Avoid others.

• Others may cost less and be smaller but can distort the input signal.
Embedded Processor ADCs

• Performance vs. cost
• Process issues
  – Digital process, analog application…
• How to improve on-board converter accuracy
  – Try an external precision reference!
DAQ Signal Chain

- Temp
- Pressure
- Speed
- Humidity
- Position
- Flow
- Light
Specifications to Watch for

- Speed: How fast is the converter?
- Resolution: What is the ENOB?
- INL: Integral non-linearity
- DNL: Differential non-linearity
- Offset: Error (in LSBs) regarding offset
- Gain: Error (in %FSR) regarding gain
## Important Parameters

<table>
<thead>
<tr>
<th></th>
<th>ADS7829</th>
<th></th>
<th>ADS7866</th>
<th></th>
<th>ADS7886</th>
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<th>56F807</th>
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<tr>
<td></td>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
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<tr>
<td><strong>Speed</strong></td>
<td>kSPS</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>Resolution</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>INL (@12bit)</strong></td>
<td>LSB</td>
<td>±0.4</td>
<td>±1.25</td>
<td>±1</td>
<td>±1.5</td>
<td>±0.6</td>
<td>±0.9</td>
<td>±4</td>
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<tr>
<td><strong>DNL</strong></td>
<td>LSB</td>
<td>±0.4</td>
<td>+1.25/-1</td>
<td>±0.8</td>
<td>+1.5/-0.9</td>
<td>±0.75</td>
<td>+1.5/-0.9</td>
<td>±0.9</td>
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<tr>
<td><strong>Offset</strong></td>
<td>mV</td>
<td>±0.18</td>
<td>±1.83</td>
<td>±0.5</td>
<td>±0.87</td>
<td>±0.31</td>
<td>±0.92</td>
<td>±0.87</td>
</tr>
<tr>
<td><strong>Gain</strong></td>
<td>%</td>
<td>±0.007</td>
<td>±0.05</td>
<td>±0.007</td>
<td>±0.05</td>
<td>±0.012</td>
<td>±0.04</td>
<td>±0.012</td>
</tr>
</tbody>
</table>

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at -40°C to 85°C, AVDD = 5V, BVDD = 3V, VREF = internal +2.5V, fCLK = 10MHz, and tSAMPLE = 500 kSPS, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>ADS8361</th>
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<tbody>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
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<tr>
<td>Full-Scale Range (FSR)</td>
<td>+IN – (-IN)</td>
<td>2.2</td>
</tr>
<tr>
<td>Operating Common-Mode Signal</td>
<td>-IN = VREF</td>
<td>±VREF</td>
</tr>
<tr>
<td>Input Switch Resistance</td>
<td>-IN = VREF</td>
<td>2.8</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>-IN = VREF</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>+IN = VREF</td>
<td>25</td>
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<tr>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>pF</td>
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</table>
# Datasheet Specs...

## ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at -40°C to 85°C, AV_{DD} = 5V, BV_{DD} = 3V, V_{REF} = internal +2.5V, f_{CLK} = 10MHz, and f_{SAMPLE} = 500 kSPS, unless otherwise noted.

### ADC’s performance over temperature at specified speed

### Ensured values based on tests in production

### Clear test conditions for specified parameters

### No hidden and unclear limitations

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>ADS8361</th>
</tr>
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<tr>
<td>ANALOG INPUT</td>
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<td></td>
</tr>
<tr>
<td>Full-Range (FSR)</td>
<td>+IN – (–IN)</td>
<td>2.2</td>
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<td>Operating Common-Mode Signal</td>
<td>–IN = V_{REF}</td>
<td>26</td>
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<tr>
<td>Input Switch Resistance</td>
<td>–IN = V_{REF}</td>
<td>±1</td>
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<td>Input Capacitance</td>
<td>–IN = V_{REF}</td>
<td>40</td>
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<tr>
<td>Input Leakage Current</td>
<td>–IN = V_{REF}</td>
<td>16</td>
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<tr>
<td>Differential Switch Resistance</td>
<td>–IN = V_{REF}</td>
<td>84</td>
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<tr>
<td>Differential Capacitance</td>
<td>–IN = V_{REF}</td>
<td>80</td>
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<tr>
<td>Common-Mode Range (CMRR)</td>
<td>At DC</td>
<td></td>
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<tr>
<td>ADC’s performance over temperature at specified speed</td>
<td></td>
<td></td>
</tr>
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</table>

### DC ACCURACY

| RESOLUTION | (NMC) | 16 | 14 | Bits |
| INTEGRAL LINEARITY ERROR | (INL) | 3.4 | ±0.5 | Bits |
| DIFFERENTIAL NONLINEARITY | (DNL) | 16 | ±2 | LSB |
| BIPOLAR OFFSET ERROR | (V_{OS}) | 1.0 | ±2 | LSB |
| BIPOLAR OFFSET ERROR MATCH | 4 | 1 | μV |
| BIPOLAR OFFSET ERROR DRIFT | (ΔV_{OS}) | 0.05 | 0.5 | ppm/°C |
| GAIN ERROR | (G_{ERR}) | 0.05 | 0.5 | % |
| GAIN ERROR MATCH | | 20 | | ppm/°C |
| GAIN ERROR DRIFT | (ΔG_{ERR}) | 50 | | dB |
| NOISE | | | | dB |
| POWER-SUPPLY RANGE | (PSRR) | | | |
| SAMPLING DYNAMICS | | | | |
| CONVERSION TIME | | | | |
| Acquisition Time | | | | |
| 100kHz ≤ f_{CLK} ≤ 10MHz | | 1.6 | 150 | μs |
| 400 | 100kHz ≤ f_{CLK} ≤ 10MHz | 400 | | ns |
| 500 | 100kHz ≤ f_{CLK} ≤ 10MHz | 500 | | ns |

### NOTES:
1. All Values are at T_{A} = 25°C. (2) Ideal input span; does not include gain or offset error. (3) LSB means Least Significant Bit, with V_{REF} equal to +2.5V; 1LSB = 76μV. (4) Specified for 14-bit no missing code. (5) Specified for 15-bit no missing code. (6) Measured relative to an ideal, full-scale input (+IN – (–IN)) of 4.9999V. Thus, gain error does not include the error of the internal voltage reference.
Table 35. ADC Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $V_{REF} = V_{DDA} - 0.3$ V, $ADCIV = 4, 9, or 14$, (for optimal performance), $ADC$ clock $= 4$ MHz, $3.0–3.6$ V, $T_A = -40^\circ$ to $+85^\circ$ C, $C_L \leq 50$ pF, $f_{OP} = 80$ MHz

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td>ADC input voltages</td>
<td>$V_{ADCIN}$</td>
<td>0$^4$</td>
<td>—</td>
<td>$V_{REF}$</td>
<td>V</td>
</tr>
<tr>
<td>Resolution</td>
<td>$R_E$</td>
<td>2</td>
<td>—</td>
<td>12</td>
<td>Bits</td>
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<td>Integral Non-Linearity</td>
<td>$INL$</td>
<td>—</td>
<td>+/- 2.5</td>
<td>+/- 4</td>
<td>LSB$^4$</td>
</tr>
<tr>
<td>Differential Non-Linearity</td>
<td>$DNL$</td>
<td>—</td>
<td>+/- 0.9</td>
<td>+/- 1</td>
<td>LSB$^4$</td>
</tr>
<tr>
<td>Monotonicity</td>
<td>GUARANTEED</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>ADC internal clock</td>
<td>$f_{ADC}$</td>
<td>0.5</td>
<td>—</td>
<td>5</td>
<td>MHz</td>
</tr>
<tr>
<td>Conversion range</td>
<td>$R_{AD}$</td>
<td>$V_{SSA}$</td>
<td>—</td>
<td>$V_{DDA}$</td>
<td>V</td>
</tr>
<tr>
<td>Conversion time</td>
<td>$t_{ADC}$</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>$t_{ADC}$ cycles$^6$</td>
</tr>
<tr>
<td>Sample time</td>
<td>$t_{ADS}$</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>$t_{ADC}$ cycles$^6$</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>$C_{ADI}$</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>pF$^6$</td>
</tr>
<tr>
<td>Gain Error (transfer gain)</td>
<td>$f_{Gain}$</td>
<td>0.93</td>
<td>1.00</td>
<td>1.08</td>
<td>—</td>
</tr>
</tbody>
</table>

1. For optimum ADC performance, keep the minimum $V_{ADCIN}$ value $\geq 25$ mV. Inputs less than 25 mV may convert to a digital output code of 0.
2. $V_{REF}$ must be equal to or less than $V_{DDA}$ and must be greater than 2.7 V. For optimal ADC performance, set $V_{REF}$ to $V_{DDA} - 0.3$ V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
Reference Voltage Accuracy

- Initial accuracy: ±0.2%
- Temp. coefficient: 60ppm/°C
- Range of interest: 60°C
- Insured accuracy: ±0.56%

0.2% + (60*60)ppm =
0.2% + 3.6% = 0.56%
<table>
<thead>
<tr>
<th>Device</th>
<th>Initial Accuracy (%)</th>
<th>Tmp.Coeff. (ppm/°C)</th>
<th>Total Accuracy (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>MSP430F167</td>
<td>±4</td>
<td>_</td>
<td>±100*</td>
</tr>
<tr>
<td>56F807</td>
<td>_</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>F2808</td>
<td>_</td>
<td>±50</td>
<td>_</td>
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<tr>
<td>ADS7829</td>
<td>_</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>ADS7866</td>
<td>±2</td>
<td>±20</td>
<td>_</td>
</tr>
<tr>
<td>ADS1203</td>
<td>±1</td>
<td>±20</td>
<td>_</td>
</tr>
<tr>
<td>ADS8361</td>
<td>_</td>
<td>_</td>
<td>_</td>
</tr>
<tr>
<td>REF29xx</td>
<td>±2</td>
<td>±35</td>
<td>±100</td>
</tr>
<tr>
<td>REF30xx</td>
<td>±0.2</td>
<td>±20</td>
<td>±50</td>
</tr>
<tr>
<td>REF31xx</td>
<td>±0.2</td>
<td>±5</td>
<td>±15</td>
</tr>
<tr>
<td>REF32xx</td>
<td>±0.2</td>
<td>±4</td>
<td>±7</td>
</tr>
</tbody>
</table>
PCB Layout Issues

- LSB size
  - Affects your layout decisions.
- Basic PCB Design Principles
  - Care must be exercised for high resolution!
- PCB Layout Reviews
  - Learn from others! Ask your co-workers what worked and what did not. Better yet: Ask us!
LSB Size

Signal range is critical

- ±10V is a FSR of 20V
  - 16 bits: \(20V/65,536 = 305\mu V\) per LSB
  - 24 bits: \(20V/16,777,216 = 1,192nV\) per LSB

- ±2.5V is a FSR of 5V
  - 16 bits: \(5V/65,536 = 76.3\mu V\) per LSB
  - 24 bits: \(5V/16,777,216 = 298nV\) per LSB

- ±0.020V is a FSR of 0.040V
  - 16 bits: \(0.040V/65,536 = 0.610\mu V\) per LSB
  - 24 bits: \(0.040V/16,777,216 = 2nV\) per LSB
• 1 inch (7 mil) trace of 1/2 oz copper with 10μA of current => voltage drop of 1.3μV.
• This is 4 LSBs at 24 bits!
AC Performance vs. Layout
With Short Traces

SNR [dB]
59.8467
H2 = -72.612 dB

SINAD (dB)
59.4855
H3 = -79.740 dB

THD (dB)
-70.4646
H4 = -107.288 dB

SFDR (dB)
72.6115
H5 = -90.596 dB

ENOB (SINAD)
9.58895
H6 = -96.973 dB

Signal power (dB)
-0.275766
H7 = -103.440 dB

H8 = -109.115 dB

H9 = -109.715 dB
Basic Layout Issues

- Separate analog and digital signals
- AGND and DGND connected at ADC/DAC
- Provide good ground return paths
- High-frequency bypassing
- Minimize inductance
- Differential signal measurements
  - Route in pairs
Avoid ‘Auto Routing’

- Auto routers do not handle analog signals very well!
- Route critical signals by hand for best performance – this is imperative.
- Route “like” channels in similar fashion.
- Remember to tie grounds locally at the most critical circuit – usually the ADC.
Ground Current from U3 affects ground for C1 & C2 which affects Crystal Y1
Ground Signal

Destroying Ground Effectiveness with traces on Ground Layer
PCB Layout

Be Careful With Ground Plane and Narrow Current Flow

Good Analog Separation and GND connection

Minds in Motion

Technology for Innovators™
Demo Time!

• Software Tools
  – ADC Pro
  – Code Composer Studio™, Embedded Workbench™

• Hardware Tools
  – Analog EVMs
  – DSP starter kits

• Where to get more
  – App notes
  – Code examples
ADC Pro

Multichannel Scope

Channel 1
Max code: 32767
Min code: -32768
Frequency: 44100
Max V: 15
Min V: -15
Waveform: Sine
Rin: 16

Channel 2
Max code: 32757
Min code: -32768
Frequency: 44100
Max V: 15
Min V: -15
Waveform: Triangle
Rin: 16

Channel 3
Max code: 32757
Min code: -32768
Frequency: 44100
Max V: 15
Min V: -15
Waveform: Square
Rin: 16

Plot Legend
- CH1
- CH2
- CH3

Block size: 512

Vertical Scale
- Range
  - FSR
  - Auto
- Units
  - Codes
  - Volts
Writing Application Code

• Code Composer Studio IDE
  – Application design, code and build, debug
  – TMS320 and TMS470

• Code Composer Essentials
  – C compiler, assembler and linker
  – MSP430 ultra-low-power controllers

• IAR Embedded Workbench
  – IDE for embedded applications
  – MSP430 and TMS470
Code-Generation Tools

• Data converter “plug-in” tool for CCS
• Supports:
  – ADCs
  – DACs
  – CODECks
  – AMC
  – PCM
TMS320C6713 Hardware
TMS470R1B1M Hardware
MSP430F449 Hardware
Evaluating Circuit Sensitivity in Analog Filters

Session ID: S284574
Wednesday at 4:10 p.m.

Mark Fortunato
Texas Instruments, Inc.
Real World Analog Solutions for Your Processor Applications

Session ID: S283976
Thursday at 4:10 p.m.

Bonnie Baker
Texas Instruments, Inc.
Data Converter Basics
How to Use and Test Data-Acquisition Products

Tom Hendrick
t-hendrick@ti.com