Texas Instruments’ TMS320C6670 System-on-Chip (SoC) is well suited for high-performance programmable applications in areas such as radar, software defined radio (SDR) and emerging broadband. These markets all have similar needs for high-performance, high-speed peripherals and power efficiency. The C6670 SoC is based on TI’s KeyStone multicore architecture and integrates four C66x DSP cores to offer real-time performance that helps customers realize R&D savings while getting to market faster.

- **Performance** – fastest fixed- and floating-point DSP core
  - Four cores at 1 GHz and 1.2 GHz
  - 153.8 GMACs / 76.8 GFLOPs for 1.2 GHz
- **Architecture**
  - KeyStone architecture
  - Multicore Navigator
  - TeraNet – On-chip switch fabric
- **Coprocessor accelerators**
  - FFTC x3 – Fast Fourier Transform
  - TCP3d x3 – Turbo Decoder
  - TCP3e x1 – Turbo Encoder
  - VCP2 x4 – Viterbi
  - BCP x1 – Bit rate coprocessor
  - RAC x2 – Receive accelerator processor
  - TAC – Transmit accelerator processor
  - RSA – Rake search accelerator
  - Packet accelerator
  - Security engine
- **High-speed input/output (I/O)**
  - PCI Express Gen II single & double lanes
  - Serial RapidIO® V2.1 x4
  - OBSAI / CPRI x6
  - DDR3 – 1600 Mhz (64b)
  - Hyperlink – chip-to-chip interconnect
- **Memory**
  - 2 MB shared L2
  - 1 MB Cache L2 per core
- **Power**
  - Dynamic power monitoring
  - SmartReflex™ technology
- **Industrial/extended temperature range**
  - -40°C to 100°C
- **Peripherals**
  - Ethernet ports SGMII x2
  - UART, PC, SPI, GPIO

**Radar** – The C6670 can be used in a variety of radar applications ranging from military to commercial. Radar (radio detection and ranging) is a demanding application that works by emitting radio frequency (RF) signals at particular frequencies and then listening for the return signals from the “target”. It involves processing data that is acquired using arrays of sensor elements to provide information relevant to the location and tracking of the target. Radar requires not only high performance, but also large on-chip memory to improve real time response. The performance integration of the C6670, combined with the large dedicated memory makes it a perfect choice for radar.

In addition, the array of data from the sensors must be processed as a set of linear equations to extract the desired information. Solution methods require math functions such as matrix inverse, factorization, adaptive filtering, etc. The greater precision of output required, along with the need for a larger dynamic range, make these functions perform significantly better on a 1.2 GHz floating-point engine like the C6670. Additionally, the SIMD enhancements and the 1.2 GHz 32 MAC/cycle fixed-point capability of the C6670, give designers tremendous flexibility in finding the right fixed- and floating-point combination to suit their applications.
of commercial and custom waveforms. The device natively supports various broadband standards such as LTE, WiMAX, WCDMA and CDMA2000, as well as multichannel solutions of narrowband waveforms such as GSM, APCO, CDMA2000, as well as multichannel solutions. The C6670 device also contains 2,048 KB of Multicore Shared Memory (MSM) that can be used as a shared L2 SRAM. A Multicore Shared Memory Controller (MSMC) prevents memory contention between the cores and arbitrates access to the shared memory between the cores and other IP blocks.

**KeyStone multicore architecture**

TI's KeyStone multicore architecture implemented in the C6670 device maximizes the throughput of on-chip data flows to eliminate the most remote possibility of bottlenecks, ensuring that the vast processing...
power of the device’s C66x DSP cores can be utilized to the maximum. Central to this architecture is TeraNet, a packet-based fabric of high-speed non-blocking channels that delivers as much as 2 terabits per second of on-chip throughput. With TeraNet and an extensive two-layer memory structure, data flows freely and effectively through the C6670 device.

Although it provides direct chip-to-chip connectivity for local devices, Hyperlink is also integral to the internal processing architecture of the C6670 device. Hyperlink is a fast and efficient interface with low protocol overhead and high throughput, running at an aggregate speed of 50 Gbps (four lanes at 12.5 Gbps full duplex). Working in conjunction with Multicore Navigator, Hyperlink transparently dispatches tasks to other local devices where they are executed as if they were being processed on local resources.

In the KeyStone architecture, CorePac is defined as the main processing element in a multicore DSP. The CorePac includes the infrastructure that supports the DSP cores, including shared memory and memory controllers. There are three levels of memory in the KeyStone architecture. Each C66x CorePac has its own level-1 program (L1P) and level-1 data (L1D) memory. Additionally, each CorePac has a local level-2 unified memory (L2). Each of the local memories can be independently configured as memory-mapped SRAM, cache or a combination of the two.

In addition, the KeyStone architecture includes a shared memory subsystem, comprising internal and external memory connected through the Multicore Shared Memory Controller (MSMC). The MSMC allows the CorePacs to dynamically share the internal and external memories for both program and data. The MSMC internal RAM offers flexibility to programmers by allowing portions to be configured as shared level-2 RAM (SL2) or shared level-3 RAM (SL3). SL2 RAM is cacheable only within the local L1P and L1D caches, while SL3 is additionally cacheable in the local L2 cache.

External memory is connected through the same memory controller as the internal shared memory, rather than to chip system interconnect as has been traditionally been done on embedded processor architectures, providing a fast path for software execution. External memory is always treated as SL3 memory and cacheable in L1 and L2.

The C6670 device also features several innovative coprocessing accelerators that offload processing tasks from the DSP engines, thereby enabling sustained high application processing rates. A packet accelerator, for example, speeds the data flow through the core by transferring data to peripheral interfaces such as the Ethernet ports or Serial RapidIO without the involvement of any core’s DSP processor. In addition, the packet accelerator works in tandem with another new coprocessor, the Security Accelerator, which provides security processing for a number of popular encryption modes and algorithms, including IPSec, SCTP, SRTP, 3GPP, SSL/TLS and several others.

**Multicore Navigator**

A breakthrough feature of the C6670 device is TI’s innovative Multicore Navigator which brings single-core simplicity to multicore devices. Multicore Navigator is designed to support hardware-assisted functional acceleration that utilizes an innovative packet based hardware subsystem in KeyStone devices. With an extensive series of over 8,000 queues and a packet-aware DMA controller, it optimizes the packet-based communications of the on-chip cores by practically eliminating all copy operations. The extreme efficiency made possible by the Multicore Navigator results in a 100x performance gain in terms of the number of packets communicated per second over previous generation cores.

The low latencies and zero interrupts ensured by Multicore Navigator as well as its transparent operations enable new and more effective programming models such as task dispatchers. Moreover, software development cycles are shortened significantly by several features inherent in Multicore Navigator, including dynamic software partitioning. With Multicore Navigator’s ‘fire & forget’ software tasking, developers save significant time and effort by defining repetitive tasks only once, and thereafter accessing and running these tasks automatically without additional coding efforts.

**Faster coprocessors for optimized wireless designs**

Since 2001 TI has delivered various coprocessing functions, consisting of configurable IP blocks to offload processing demands as well as increase overall device performance. TI’s coprocessors also reduce power requirements and dissipation as well as board complexity, making new products easier to design, build and debug.

As various industry standards evolve and related implementations become standard-
ized, each evolution of the TI DSP devices has included more and more acceleration/coprocessing and as such provides a compelling roadmap to lower power and costs while delivering higher performing solutions for our customers. TI’s strategy of integrating DSP cores along with coprocessors and accelerators has proven to be the simplest and most economical approach to communications, wireless and other high performance applications and continues to be the market leading solution today.

TI is now offering its third generation of communications coprocessors that deliver the equivalent processing power of over 250 DSP cores. Hundreds of customers that have come to rely on TI’s DSPs and software solutions, have realized that TI’s DSP platforms are easier to design with and deliver the processing power and reliability needed. TI’s accelerators and coprocessors eliminate external FPGAs and ASICs as well as additional DSPs that were previously needed to deliver the performance needed, lowering the system cost and design complexity.

The C6670 has fifteen high-performance embedded coprocessors to help offload DSP processing demands while increasing overall device performance – four enhanced Viterbi decoder coprocessors (VCP2), three third-generation turbo decoder coprocessor (TCP3d), turbo encoder coprocessor (TCP3e) and three fast Fourier transform coprocessors (FFTC). There is also a bit rate coprocessor (BCP) that significantly speeds up channel encoding/decoding operations on-chip, dual receive accelerator coprocessors (RAC) used for WCDMA processing and transmit acceleration coprocessor (TAC) also used in WCDMA.

Finally, the C6670 also has rake search accelerators (RSA) that are tightly coupled to the C66x core.

The four Viterbi decoders (VCP3) support more than 38 Mbps at 40 bit block size. The three Turbo decoder coprocessors (TCP3d) support WCDMA/HSPA/HSPA+/TD-SCDMA, LTE and WiMAX. The TCP3d supports 548 Mbps for LTE and up to 353 Mbps for WCDMA. The single turbo encoder coprocessor (TCP3e) is targeted for LTE with 643 Mbps and WCDMA with 746 Mbps. With three fast Fourier transform coprocessor (FFTC), the C6670 supports 2048 point FFT in 4.8us. Finally the bit rate coprocessor (BCP) is targeted for uplink / downlink bit rate processing in LTE (914 Mbps), WCDMA/TD-SCDMA (405 Mbps) and WiMAX. The RAC supports up to 256 WCDMA users at eight fingers without measurement. Finally, the TAC supports up to 256 WCDMA users with two radio links and diversity.

**Lowest power consumption for the performance**

TI has a legacy of providing the lowest power, high performance DSPs on the market. TI is able to achieve its ultimate low power through the combination of its process technology, including SmartReflex technology, and the proactive use of power management techniques, such as adaptive voltage scaling, to keep active power at a minimum. In addition, TI has leveraged its extensive knowledge in the high performance applications market to establish multiple, dynamic power modes for the TMS320C6670 device, allowing customers a programmable strategy for optimizing power usage based on operation and use models for a particular market.

TI's power efficient architecture also enables designers to develop smaller, power efficient portable devices for markets such as mid to small form factor RADAR and scalable software defined radios. The C6670 enables multiple processors in previous designs to be consolidated down due to its better power profile coupled with higher performance than competitive products. With more processing performance in the same power envelope as previous generations of products, the C6670 gives designers more freedom and processing room to develop even higher performance applications.

**Complete tools and support**

The C6670 device provides a full suite of best-in-class Eclipse-based development and debug tools, including: a new C compiler, an assembly optimizer to simplify programming and scheduling and a Windows® debugger interface for visibility into source code execution. TI’s compiler generates highly efficient code that is “first pass efficient” so there is less need to optimize it. TI’s debug tools help developers to visualize problems and resolve them quickly, helping designers get products to the field faster while saving development resources. In addition, TI offers a TMS320C6670 evaluation module (EVM) that helps customers to quickly evaluate the C6670’s high performance.

**For more information**

To learn more about the TMS320C6670 SoC please visit [www.ti.com/c6670](http://www.ti.com/c6670). Discover how the C6670 can add performance to your next high-performance, computation-intensive application design.

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