

# TMS320TCI6636 SoC

## High-performance SoC for ultra high capacity small cells and green power macro cells



Texas Instruments continues to lead and innovate in the communications infrastructure market through analysis of the market's inflection points and technology drivers. TI also has an eye on operator challenges and managing the data deluge is one of the most significant challenges operators face today. As wireless data rates increase with high-speed 3G and even faster 4G services, the ability to efficiently handle the large volume of data flowing through the chip infrastructure becomes critically important. With the right silicon technology and design, small and macro cells can work together to manage the immense network traffic users are generating. Operators are moving to heterogeneous networks that intermix macro and small cell solutions to deliver enhanced user experiences. Operators must also field solutions that support a mix of 2G, 3G and 4G subscribers. TI's TMS320TCI6636 combines ARM® RISC cores, DSP cores and AccelerationPacs providing the ideal mix of processing element for ultra high capacity small cell and green power macro cell infrastructure. This enables developers to deliver the data bandwidth and performance that operators and subscribers demand.

The TCI6636 SoC is the first wireless infrastructure system-on-chip (SoC) based on TI's new KeyStone II architecture. The TCI6636 SoC is ideally suited to the data-centric performance that wireless network operators are demanding today for 4G small cell base stations and provides the power to help the operator migrate to future standards. The eight TMS320C66x DSP cores provide programmable performance while expanded AccelerationPacs focus on packet, symbol and bit-rate processing to allow base station manufacturers to support a mix of WCDMA and

### Key Features

- Based on new KeyStone II architecture for greater scalability and portability from macro to small cells reducing product development expense
- First infrastructure device with quad ARM® Cortex™-A15 RISC cores
- Eight 1.2-GHz TMS320C66x DSP core subsystems combine floating and fixed point on the same core, delivering floating-point performance at fixed-point speeds
- In addition to on-core memory for ARM RISC and DSP cores, TCI6636 SoC includes KeyStone II's Multicore Shared Memory Controller (MSMC) with 6-MB SRAM memory shared by processing cores to minimize latency with zero utilization of TeraNet's central network-on-chip
- KeyStone II's network and security coprocessors and Multicore Navigator combine to provide Layer 2, 3 and transport acceleration for all wireless base station standards, minimizing latency and increasing system performance
- Multicore Navigator affords single-core simplicity to multicore SoCs
- Best power/performance ratio, coupled with unique power-saving hibernation modes, delivers the lowest power for green base stations
- Enhanced AccelerationPacs support a mix of WCDMA and LTE users to help operators manage transition from 3G to 4G
- First LTE-A ready SoC with the processing power and memory to support future standards
- Enables new use cases for base stations such as macro cell controller and green power base stations
- Leverages high-performance 28-nm process technology

LTE users, easing the transition from 3G to 4G. The TCI6636 SoC is the first SoC to integrate four ARM Cortex-A15 RISC cores, providing high-performance RISC processing at ultra-low power consumption levels.

The integration of four ARM Cortex-A15 RISC cores greatly reduces system cost. The ARM Cortex-A15 RISC cores enable developers to design low-power, high-performance solutions supporting more users on data-centric applications and bringing a new level of power efficiency and integration to infrastructure developers. The Cortex-A15 core coupled with the incorporation of packet and security processors eliminate the need for an external

network processor and all its associated memory, clock and power-management support chips.

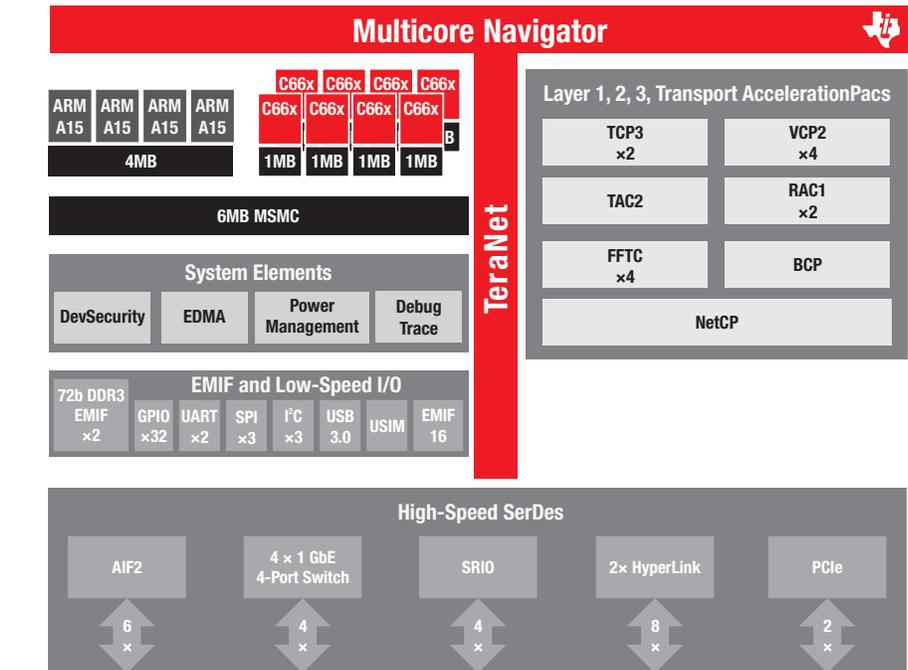
With both fixed- and floating-point processing on each DSP core, the TCI6636 SoC enables base station designers to take advantage of rapid algorithm prototyping and quick software redesigns, reducing costs and development time. Because the C66x cores are so powerful, significantly fewer cores are needed to provide four times the processing power of previous generations of DSPs. Designers enjoy simplified programming with fewer cores, along with increased performance.

KeyStone II leverages advanced 28-nm technology for improved cost efficiency through integration of multiple RISC cores and DSP cores and lower system power consumption. The TCI6636 SoC features an ideal mix of processing elements including radio accelerators, network and security coprocessors, eight fixed- and floating-point capable digital signal processor (DSP) cores and four ARM® RISC cores, providing the ideal processing element for all aspects of ultra high capacity small cell base stations. An enhanced Multicore Navigator featuring 16K queues, 1M descriptors and eight built-in uRISC cores facilitates data movement among different system end point without CPU intervention. In addition, KeyStone II offers Navigator Runtime software that is a thin layer of software on top of Navigator. Navigator Runtime enables dynamic scheduling and load balancing, accelerates application software development, gives designers the ability to easily add differentiating, value-added features and maximizes multicore performance with reduced cost.

Designers stand to benefit from the TCI6636 SoC's software compatibility with TI's previously announced TCI6612, TCI6614, TCI6616 and TCI6618 wireless base station SoCs to design multimode base stations that support all 2G, 3G and 4G standards. OEMs can simplify the migration to 4G and beyond with this flexibility, and it allows base station OEMs to develop a wider portfolio of solutions at a lower cost and in a shorter time than with competing solutions. Manufacturers can jumpstart LTE-A development with the TCI6636 SoC. It is an ideal platform for trialing capabilities beyond LTE and supports carrier aggregation to 40 MHz as well as a 600 Mbps downlink and 150 Mbps uplink.

### TCI6636 high-performance solution for ultra high capacity small cells

Designed specifically for ultra high capacity small cell and green power macro cell wireless infrastructure baseband applications, the TCI6636 SoC enables baseband solutions for WCDMA/HSPA/HSPA+, TD-SCDMA, WiMAX, GSM, FDD-LTE and TDD-LTE applications as well as providing the bandwidth and performance for future standards such as LTE-A. To make the transition easier, the TCI6636 SoC is code compatible with TMS320C6000™ DSP software, allowing



▲ TCI6636 SoC block diagram

software reuse and maintaining value-added designs and IP. In addition, TI's TCI6636 SoC leverages the KeyStone II architecture for scalability to meet the need of all infrastructure equipment, from single-sector small cells to multi-sector macro cells. With one software base driving a variety of products, developers will realize the highest R&D efficiency possible as well as optimized product costs.

### TCI6636 SoC for green power macro cells

The TCI6636 SoC enables new-use cases of macro cells, including the macro cell controller – a new level of integration for macro base stations. The macro cell controller completely replaces the expensive and power-hungry network processor with a full-featured wireless SoC. With the help of a network coprocessor, the TCI6636 SoC can perform all of the transport network termination and packet and security processing of a traditional network processor as well as all operations and management functions. It also acts as an onboard controller for baseband processors, for example, a pair of TCI6618 SoCs in a macro configuration. There is additional Bill of Material (BOM) savings by utilizing the integrated Ethernet switch on the TCI6636 SoC, eliminating the need for an external interconnect switch that can cost upwards of U.S. \$200. In periods of low load, such as during the night, the TCI6636 SoC can assume all of the baseband processing and shut

down the TCI6618 SoC pair. The result is an impressive power savings with full performance delivered to the active subscribers.

### Providing the ideal mix of performance and peripherals

The TCI6636 SoC is based on 28-nm process technology and delivers up to 10 GHz of raw DSP processing power, as well as performance of up to 307 16-bit GMACs per second, making it a very cost-effective solution for high-performance DSP programming challenges. Due to its floating-point capability, the TCI6636 SoC offers performance of up to 153 billion floating-point operations per second (GFLOPs), making this SoC one of the industry's most powerful floating- and fixed-point SoCs. Because the TCI6636 SoC incorporates both fixed- and floating-point capabilities on the same core, it can perform up to five times faster than a traditional floating-point implementation alone. In addition, the development and debugging cycle time for complex algorithms is significantly reduced from a multiple-month cycle to just a few days. The TCI6636 SoC integrates eight C66x DSP cores and includes 90 instructions targeted for floating-point and vector-math-oriented processing.

The TCI6636 SoC integrates large on-chip memory organized as a two-level memory system that minimizes latency and increases system performance. Each C66x DSP has 1MB private L2 memory, the quad-ARM

Cortex™ - A15 cluster has 4MB shared L2, and, in addition, there is 6MB shared L3 memory across DSP and ARM® cores, resulting total of 18MB total programmable on chip memory. The Shared Memory Controller (MSMC) is directly connected to DDR3 which bypasses TeraNet, thereby reducing external memory access latencies. The large on-chip memory enables the lowest latency memory access with highest performance. 6MB shared memory across heterogeneous cores facilitates multicore programming, ease multicore programming challenges and enables highly efficient multicore software.

The TCI6636 SoC has a high-performance peripheral set with everything needed to develop robust base stations of varying coverage and capacity, including:

- Three I<sup>2</sup>C, three SPI, one USB 3.0, one USIM and two UART
- PCI Express port with two lanes supporting GEN1 and GEN2 up to 5 GBaud
- Twenty 64-bit general-purpose timers (also configurable as forty 32-bit timers)
- 32-pin general-purpose input/output (GPIO) port with programmable interrupt/event generation mode
- Multicore Navigator enables hardware-assisted software programming paradigm
- Four lanes of Serial RapidIO® (SRIO), compliant with RapidIO 2.1 spec for up to 5-Gbps operation per lane
- Five Enhanced Direct Memory Access (EDMA) modules
- Two 72-bit DDR3 interfaces for up to 1,600 MHz speed
- 16-bit external memory interface (EMIF) for connecting to flash memory (NAND and NOR) and asynchronous SRAM
- Second-generation SerDes-based antenna interface (AIF2) capable of up to 6.144 Gbps operation per link with six high-speed serial links, compliant to OBSAI RP3 and CPRI standards
- Two Hyperlinks supporting a combined total of up to 100 GBaud interconnection with other KeyStone architecture devices to provide resource scalability

For efficient communications between the device and the network, the TCI6636 SoC includes a network coprocessor that consists of:

- Five 10/100/1000 Ethernet media access controllers (EMACs), which provide an efficient interface between the SoC and the core network
- Management data input/output (MDIO) module (also part of the EMAC) that continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system
- Packet accelerator that provides L2-to-L4 classification functionalities and the processing power of up to 5 Gbps wire rate switching
- Security accelerator block capable of 6.4-Gbps Ethernet traffic on IPSec, SRTP and SSL/TLS security protocols and 3 Gbps traffic on 3GPP and WiMAX air interface
- Embedded Ethernet switch that allows multiple devices to be connected through four SGMII ports, eliminating the need for a board level Ethernet switch

The TCI6636 SoC includes many wireless base station AccelerationPacs to offload the bulk of the processing demands of layer 1 and 2 base station processing. This offloading frees the cores for receiver algorithms and other differentiating functions. The SoC contains multiple copies of key coprocessors such as the FFTC and TCP3 enabling designers to develop the fastest, most efficient infrastructure possible.

### **Bit-rate coprocessor for increased spectral efficiency**

The bit-rate coprocessor (BCP) is a multi-standard AccelerationPac that offloads all bit-rate processing in the wireless signal chain without the need to involve the DSP or RISC cores at any step once the BCP is engaged. The BCP contains the modulator, demodulator, interleaver/de-interleaver, turbo and convolution encoding, rate matcher/rate de-matcher, correlator for block code decoding, and CRC engine. The BCP enables turbo interference cancellation for MIMO equalization and enables high-performance PUCCH format 2 decoding. It offloads approximately 15 GHz of CPU MIPS. These techniques, coupled with the powerful MIMO processing capabilities of TI's new DSP C66x cores, yield an SoC that delivers on the promise of 4G for operators and users alike and supports more than 1.5 Gbps for LTE and 780 Mbps for WCDMA/TD-SCDMA.

### **Faster coprocessors for optimized infrastructure designs**

Since 2001, TI has delivered radio coprocessing functions as AccelerationPacs that consist of configurable hardware accelerators to offload processing demands as well as increase overall system performance. TI's coprocessors also reduce base station power requirements and dissipation as well as board complexity, making new products easier to design, build and deploy.

As wireless radio standards evolve and related implementations become standardized, each evolution of TI's wireless SoCs includes additional coprocessing, providing a compelling path to lower power and costs while enabling higher-performing base station and infrastructure solutions from our customers. TI's SoC strategy of integrating DSP and ARM RISC cores with AccelerationPacs is the most efficient and most economical approach to wireless base station SoC design and continues to be the market-leading solution. TI's AccelerationPacs eliminate external FPGAs and ASICs that were previously needed to meet the performance demanded of 3G and 4G base stations.

The TCI6636 SoC has multiple, dedicated high-performance embedded coprocessors to perform intensive signal-processing functions common to wireless base station applications. The coprocessors are:

- Four Viterbi decoder coprocessors supporting more than 50 Mbps at a 40-bit block size
- Two enhanced turbo decoder coprocessors supporting up to 282 Mbps for LTE and WCDMA at eight iterations
- Two WCDMA receive acceleration coprocessors supporting 8192 correlators
- WCDMA transmit acceleration coprocessor supporting 2,304 spreaders
- Four fast Fourier transform coprocessors (2,400 MCPS at 1,024 FFT size)
- Bit-rate coprocessor accelerates the entire bit-rate processing

Together, these coprocessors significantly accelerate channel encoding/decoding operations. Also included in the SoC are 16 tightly coupled rake/search accelerators (RSAs) for code-division-multiple-access (CDMA) assistance with chip-rate processing for WCDMA release 99, HSDPA and HSDPA+.

## Delivering full multicore entitlement

The TCI6636 SoC is the first SoC based on TI's KeyStone II multicore architecture. KeyStone II continues to set the standard by providing full multicore entitlement. This provides non-blocking access to all processing cores, peripherals, coprocessors and I/Os. Innovations that unleash full multicore entitlement are Multicore Navigator, TeraNet, Multicore Shared Memory Controller (MSMC) and HyperLink.

**Multicore Navigator** – TI's Multicore Navigator is an innovative packet-based manager that controls and abstracts the connections between the various subsystems on the SoCs. With a unified interface for communication, data transfer and job management, Multicore Navigator enables higher system performance with fewer interrupts and reduced software complexity with a "fire and forget" paradigm. Benefits of Multicore Navigator include:

- Dynamic resource/load sharing
- Offloading CPU overhead/delay related to inter-subsystem communications
- Hardware-based task prioritization
- Dynamic load balancing
- Common communication methodology for all IP blocks (software, I/O and accelerators)

**TeraNet** – TeraNet is a hierarchical switch fabric that combines to deliver more than two terabits of bandwidth for data transfer within the SoC. This virtually guarantees that the cores or coprocessors are never starved for data and can deliver the entitled processing horsepower. Because the switch fabric is hierarchical instead of a flat crossbar, overall power consumption is much lower in idle states and systems latency is minimized. Low latency is a key requirement of next-generation base stations.

**Multicore Shared Memory Controller (MSMC)** – TI's TCI6636 SoC includes a unique improved memory architecture for enhanced performance. TI's Multicore Shared Memory Controller (MSMC) allows the cores to directly access shared memory without having to use any TeraNet bandwidth. The MSMC arbitrates access to shared memory between the cores and other IP blocks, eliminating memory

contention. Shared memory access for code is nearly identical in latency to local L2 access, with highly effective pre-fetch mechanisms for code and data.

The DDR3 external memory interface in the TCI6636 SoC includes two 1,600-MHz, 72-bit busses with 8 GB of addressable memory space. Tied directly to the MSMC, the DDR3 EMIF reduces latency associated with external memory fetches and provides the speed increase and support needed for larger applications that operate on large amounts of data, which is essential for advanced 3G and 4G base stations.

**HyperLink** – Two HyperLink interfaces supporting up to 100Gbps provide a proprietary high-speed interconnect that allows low protocol and high-speed communication and connectivity to other KeyStone devices providing OEMs a seamless path to scalable solutions. The HyperLink on the TCI6636 SoC works in conjunction with the Multicore Navigator to dispatch tasks to multiple devices transparently, so they execute as if they are running on local resources.

## TCI6636 SoC as Layer 2, 3 and transport processing engine

The TCI6636 SoC combines unmatched PHY processing capabilities with dedicated coprocessors for Layer 2, 3 and transport layer processing. This enables designers to create base stations without a separate network processor thereby reducing board complexity and cost without compromising performance.

The network coprocessor enables fast-path processing in the transport network layer and deep into the Layer 2 and 3 of the radio network. Within the SoC's network coprocessor, the Packet Accelerator and the Security Accelerator perform fully-accelerated autonomous packet-to-packet processing. They leverage the Multicore Navigator, which uses a zero-copy method to optimize data processing at all layers. The network coprocessor supports classification and ordering, multicore-accessible storage, memory management, segmentations and reassembly and delivery across multiple cores and devices. Layer 2 data-plane and transport plane overhead can be reduced by 10–15 times due to the fast-path and zero-copy processing.

## Lowest power consumption for performance

TI has a history of providing the lowest-power wireless base station and infrastructure SoCs on the market. TI is able to achieve its ultimate low power through the combination of its process technology, SmartReflex™ technology, and the proactive use of power-management techniques (such as dynamic voltage and frequency scaling, memory retention until access, power and clock gating to name a few) in every wireless infrastructure semiconductor device to keep active power to a minimum. When network loading drops at night, the TCI6636 SoC, acting as a macro cell controller, can power down companion TCI6618 base-band chips to entirely eliminate their energy consumption. KeyStone II technology makes restarting shutdown elements fast and easy.

## Complete tools and support

TI provides a full suite of best-in-class Eclipse-based development and debugging tools with the TCI6636 SoC, as part of TI's well known Code Composer Studio™ (CCStudio) Integrated Development Environment. These include a C compiler, an assembly optimizer to simplify programming and scheduling and a Windows® debugger interface for visibility into source-code execution. TI's compiler generates highly efficient code that is "first-pass efficient" so there is less need to optimize it. TI's debugging tools help developers visualize problems and resolve them quickly, so designers can get products to the field faster while saving development resources. In addition, TI will offer an evaluation module (EVM) to help customers prototype quickly. All of these tools integrate the ARM® RISC processor as well, enabling designers to quickly and efficiently develop code for all subsystems of the SoCs, within a single platform.

## For more information

To learn more about the TCI6636 SoC visit [www.ti.com/multicore](http://www.ti.com/multicore). Discover how the TCI6636 SoC can add performance to your next ultra high capacity small cell or green power macro cell infrastructure design and carry that design into the future.

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